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EE 102-03

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Lab 3 Combinational Logic Circuit

1) Purpose

Aim of this lab is to learn how to construct combinational logic circuits using integrated circuits (such as 74HC163 four bit counter, 74HC32N 2 inp OR gates, 74HC08 2 inp AND gates) and other components (such as resistors, LED's) on breadboard. We learned how to use integrated circuits like 74HC163 4 bit counter and how to read their datasheet. We also used oscilloscopes and LED's to monitor the signals in the circuit we constructed. We used 4 bit counter 74HC163 for testing all combinations of inputs and their results.

2) Methodology

In this lab basically 74HC163, 74HC32N, 74HC08, 5 resistors (1K ohm), 5 LED'S, a 5v power supply, a signal generator producing 1HZ square wave, a breadboard and jumpers are used.

A) 74HC163

This is basically a 4 bit counter integrated circuit. It generates 4 output signals with 0 phase difference and periods of 1t, 2t, 4t, 8t. Resulting in a 4 bit counter. To explain, the output signal with 1t period takes values 0 and 1 and after that output signal with 2t period turns from 0 to 1 and for 4 different outputs it generates all the combinations of 16. In order 74HC163 to be operate its Vcc port should be connected to a 5v power supply and GND port to ground then pins cep, cet, pe and mr should be connected to 5v line to make it count mode. Then a square wave signal by a signal generator should be connected to its cp pin. The circuit and its output signals periods are synchronized according to this signal. This 4 bit counter is used for testing all the combinations of inputs for the implemented design.

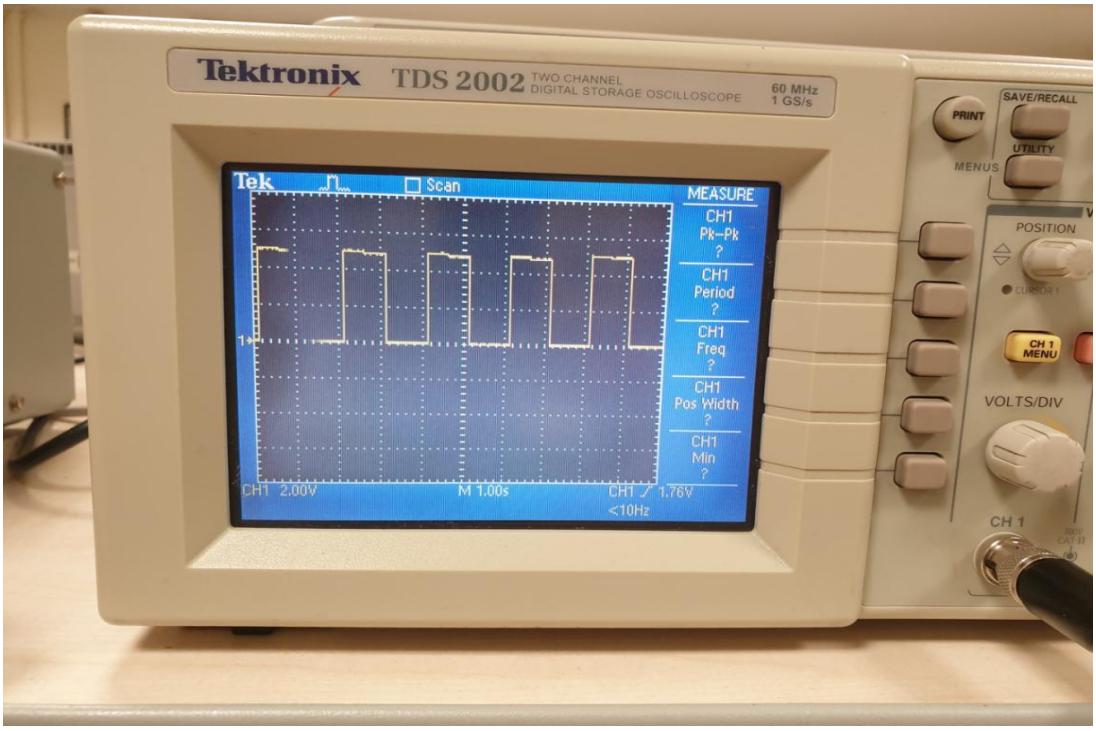

Figure 2.1 output signal representing least significant digit and period with 1t of the 74HC163 counter.

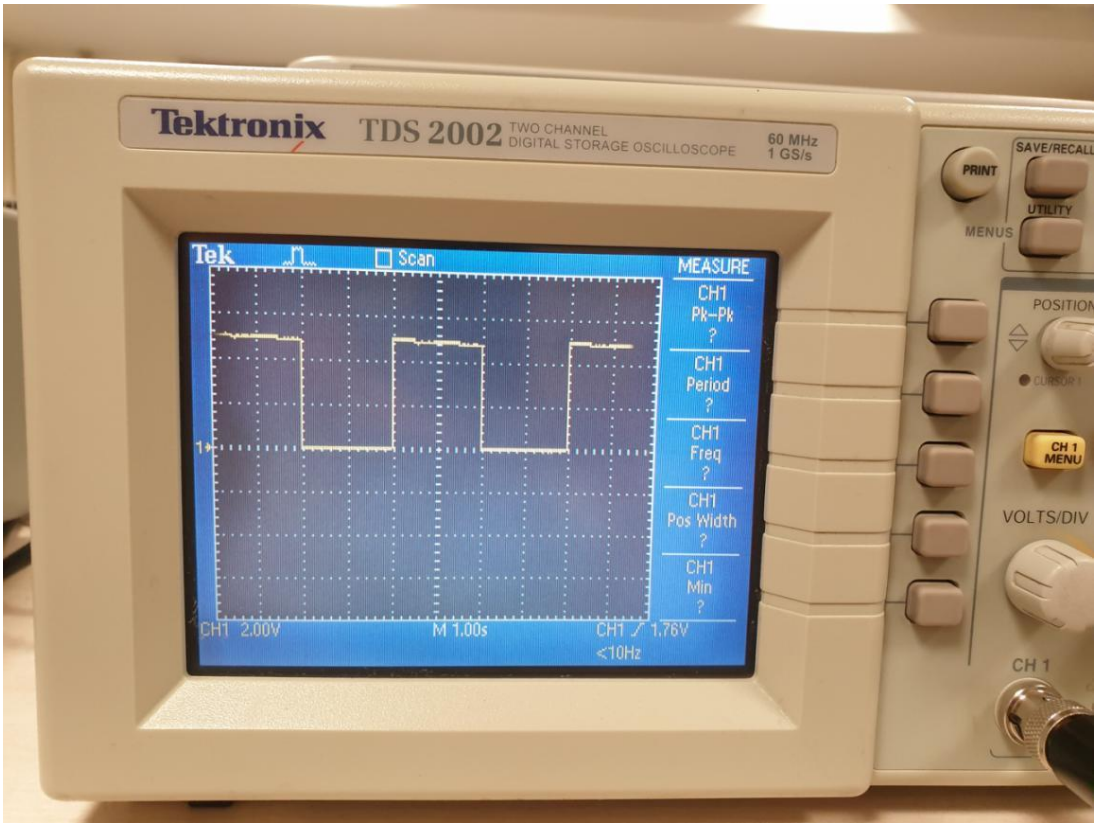

Figure 2.2 output signal period with 2t of the 74HC163 counter.

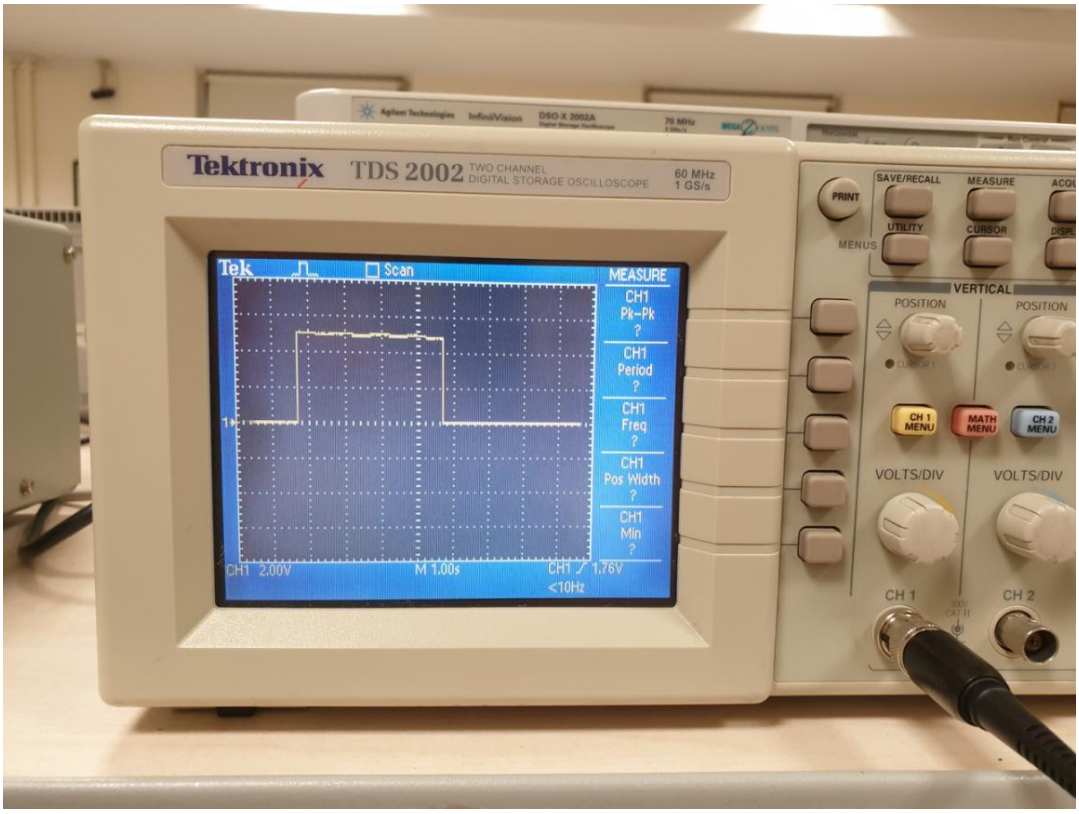

Figure 2.3 output signal period with 4t of the 74HC163 counter.

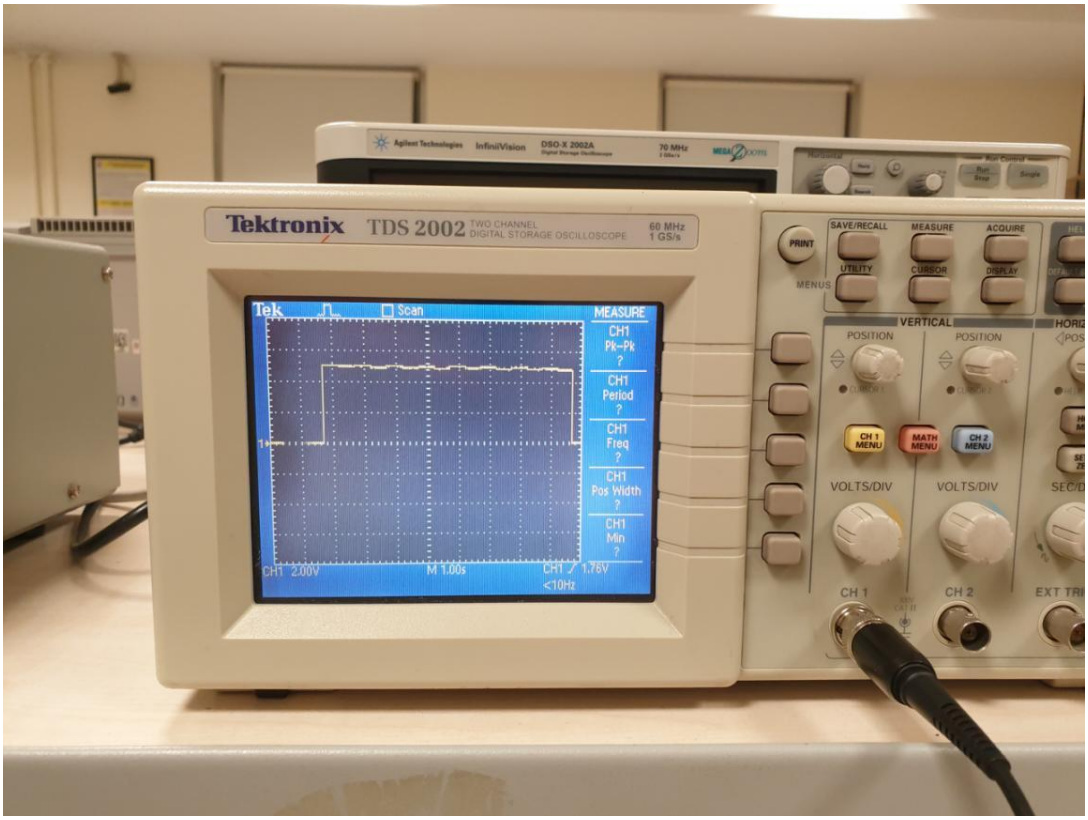

Figure 2.4 output signal representing most significant digit and period with 8t of the

74HC163 counter.

B) 74HC32N

This integrated circuits needs to be connected to 5v power supply by Vcc port and GND port to ground. It includes 4 two input OR gates. It is used to implement the OR gates in the implemented design.

C) 74HC08

This integrated circuits needs to be connected to 5v power supply by Vcc port and GND port to ground. It includes 4 two input AND gates. It is used to implement the AND gates in the implemented design.

D) Designed combinational circuit

Code1 (A)	Code2 (B)	Check1 (C)	Check2 (D)	Success (F)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Figure 2.5 truth table of the design.

The same design in the lab2 is implemented using integrated circuits and to test it a counter is used. It can be expressed as F = ((C AND D) AND (A OR B)) OR (A AND B).

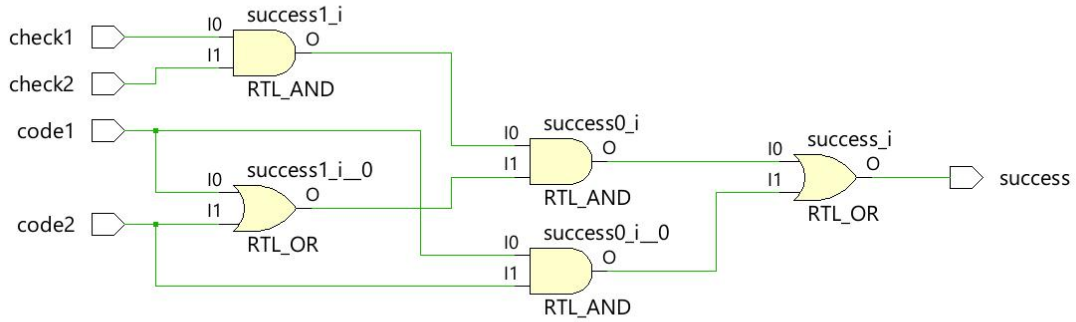

Figure 2.6 schematic representation of the combinational circuit design.

4 inputs generated by counter 74HC163, 3 AND gates implemented using 74HC08 integrated circuit, 2 OR gates implemented using 74HC32N integrated circuit. Inputs tracked by connecting them with parallel to green LED circuits and after input signals processed by the integrated circuits output signal is traced by the red LED.

3) Results

Resulting circuit outputs with regard to inputs produced by 74HC163 counter are shown figures below. Additionally, the resulting circuit's wave form is monitored using an oscilloscope and compared with the test bench simulation result of the VHDL with the same design and test bench's input signals connected in the same order than observed that the wave forms are the same.

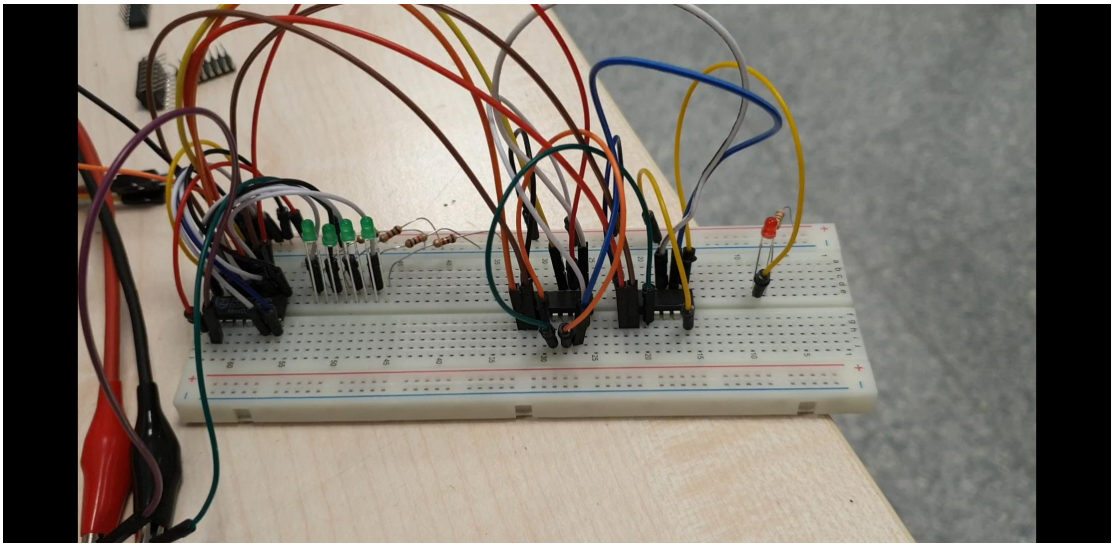

Figure 3.0 representing C=0, D=0, A=0, B=0 inputs and F=0 output.

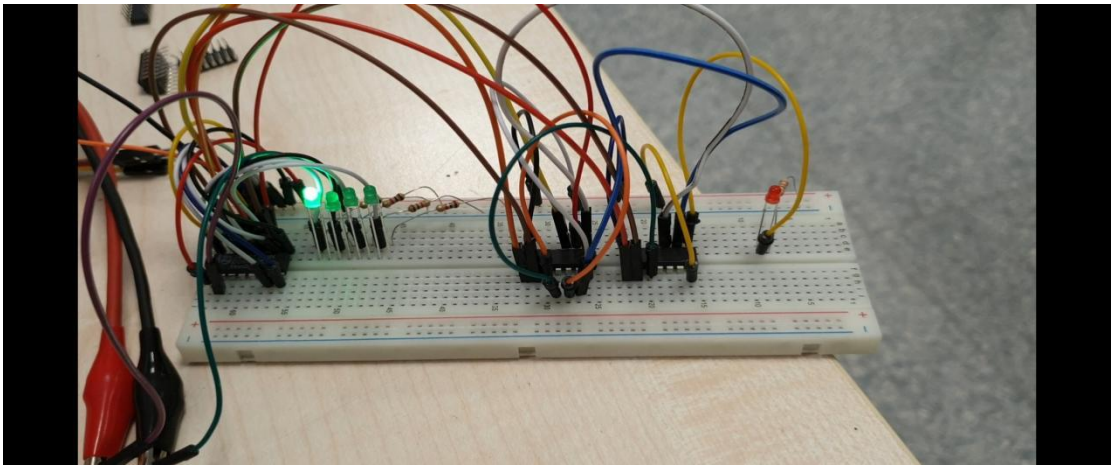

Figure 3.1 representing C=1, D=0, A=0, B=0 inputs and F=0 output.

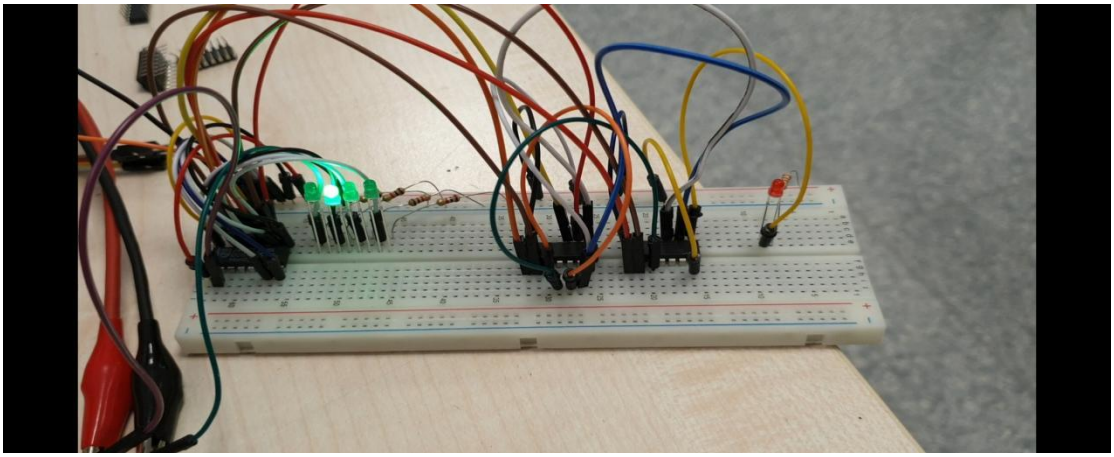

Figure 3.2 representing C=0, D=1, A=0, B=0 inputs and F=0 output.

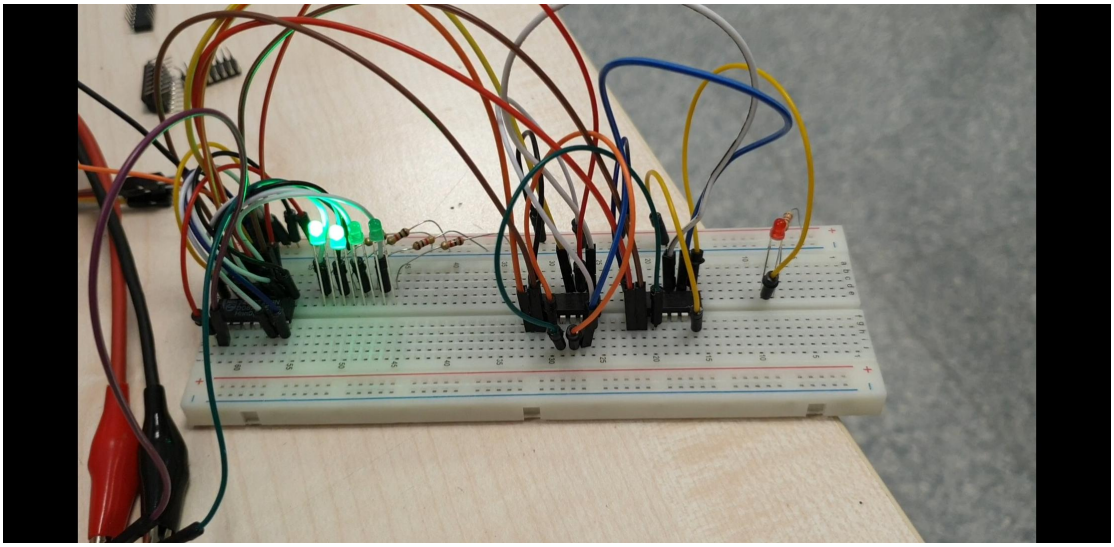

Figure 3.3 representing C=1, D=1, A=0, B=0 inputs and F=0 output.

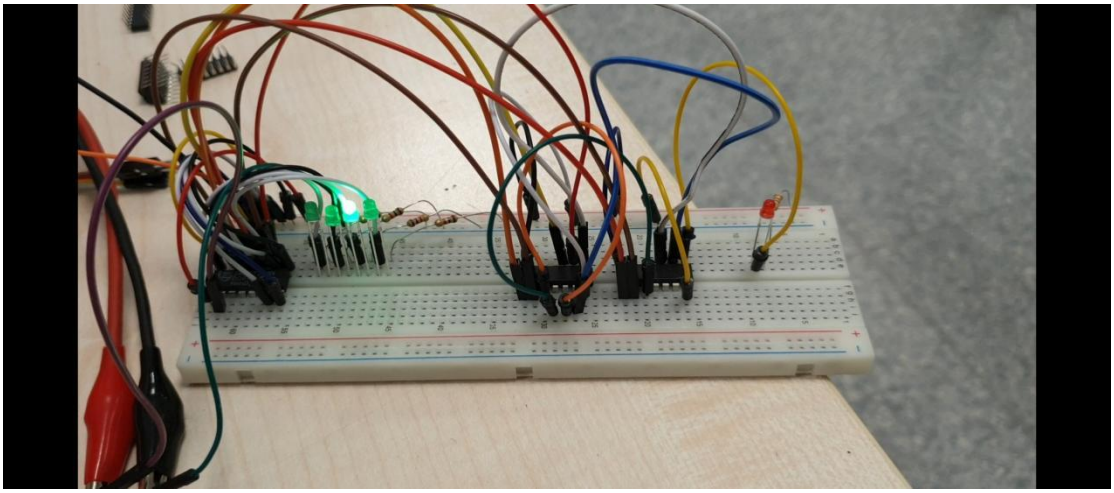

Figure 3.4 representing C=0, D=1, A=1, B=0 inputs and F=0 output.

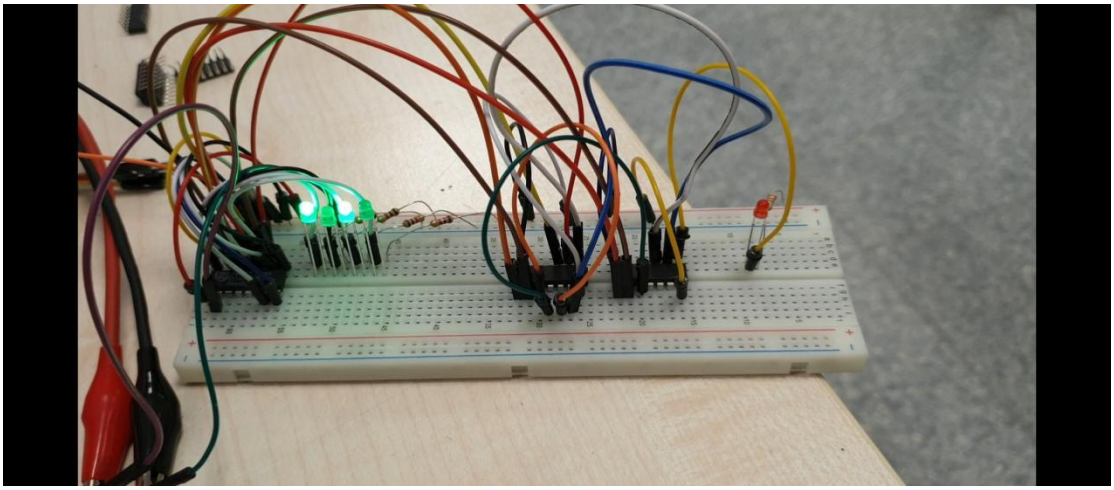

Figure 3.5 representing C=1, D=0, A=1, B=0 inputs and F=0 output.

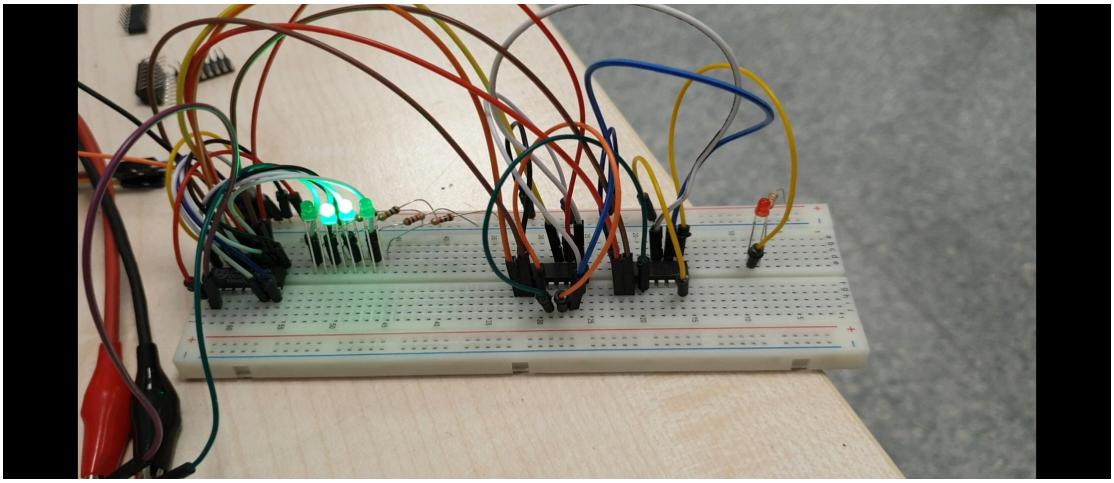

Figure 3.6 representing C=0, D=1, A=1, B=0 inputs and F=0 output.

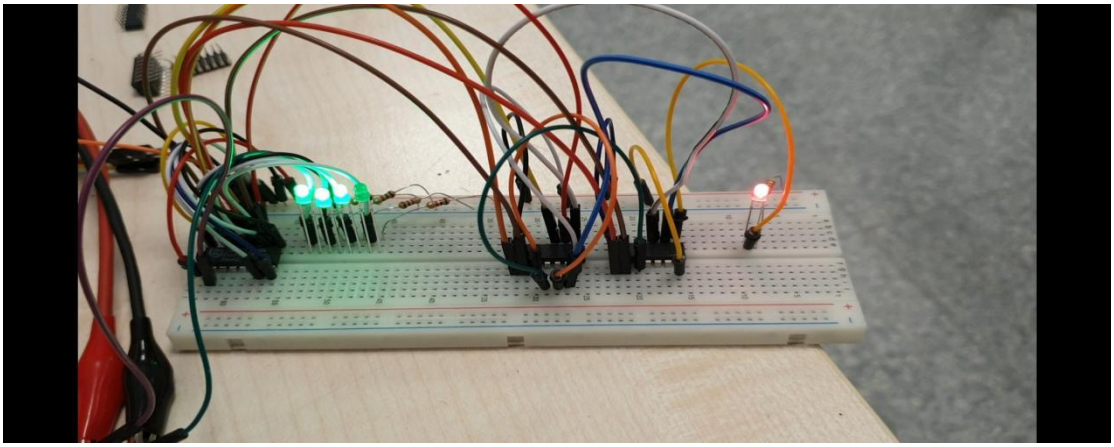

Figure 3.7 representing C=1, D=1, A=1, B=0 inputs and F=1 output.

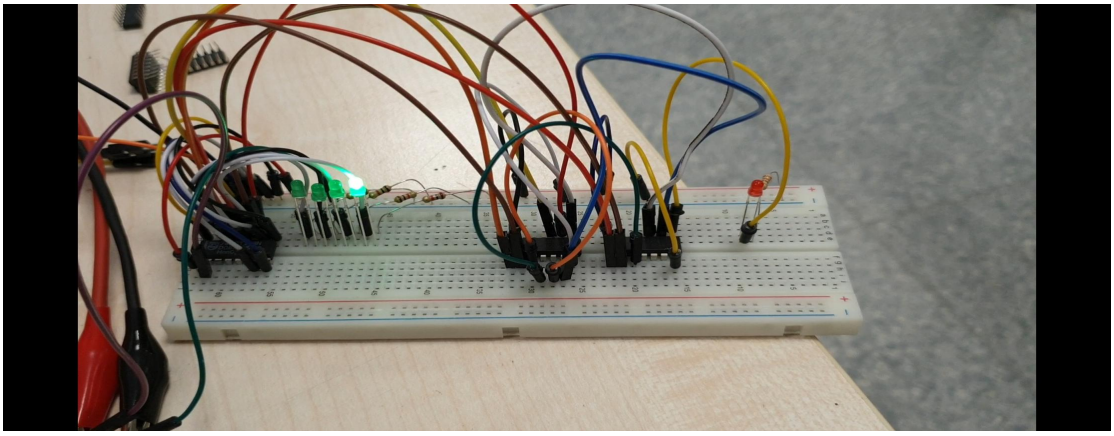

Figure 3.8 representing C=0, D=0, A=0, B=1 inputs and F=0 output.

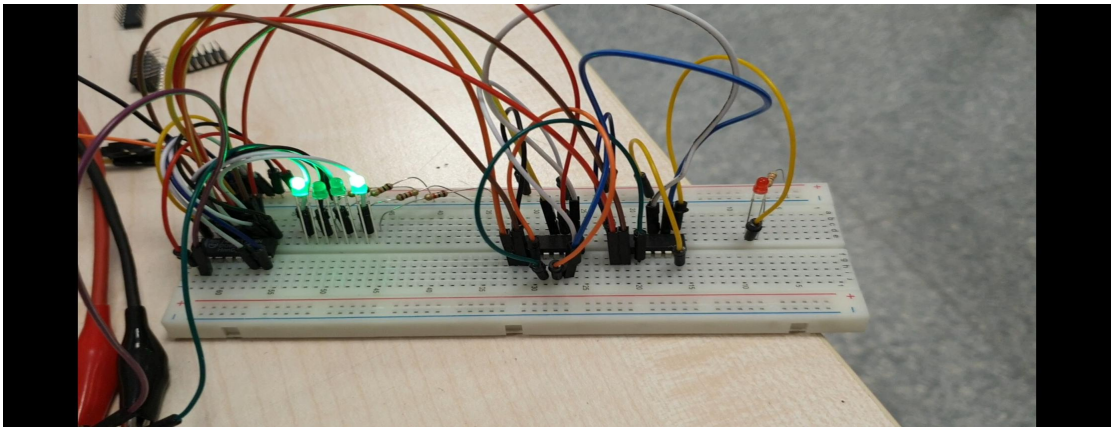

Figure 3.9 representing C=1, D=0, A=0, B=1 inputs and F=0 output.

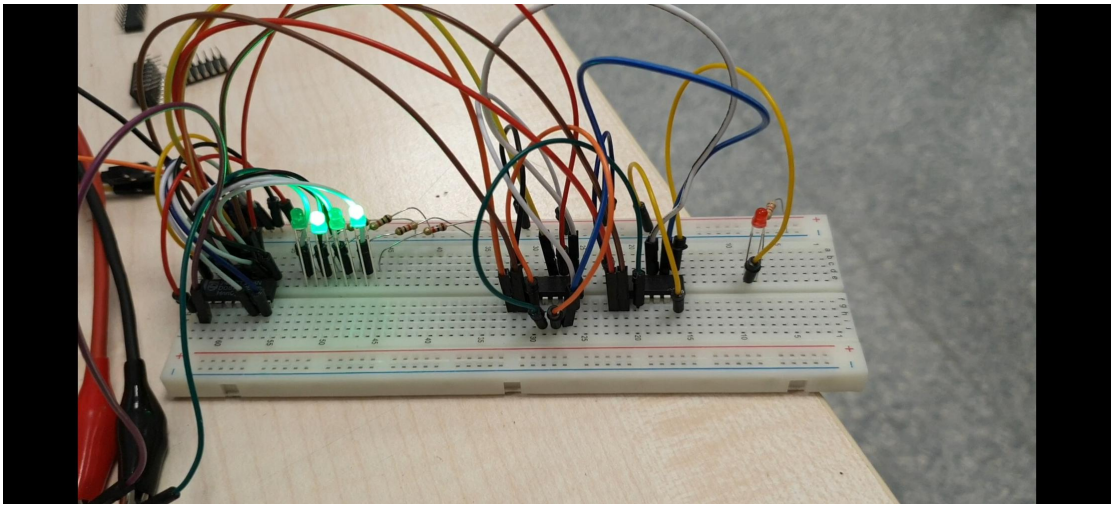

Figure 3.10 representing C=0, D=1, A=0, B=1 inputs and F=0 output.

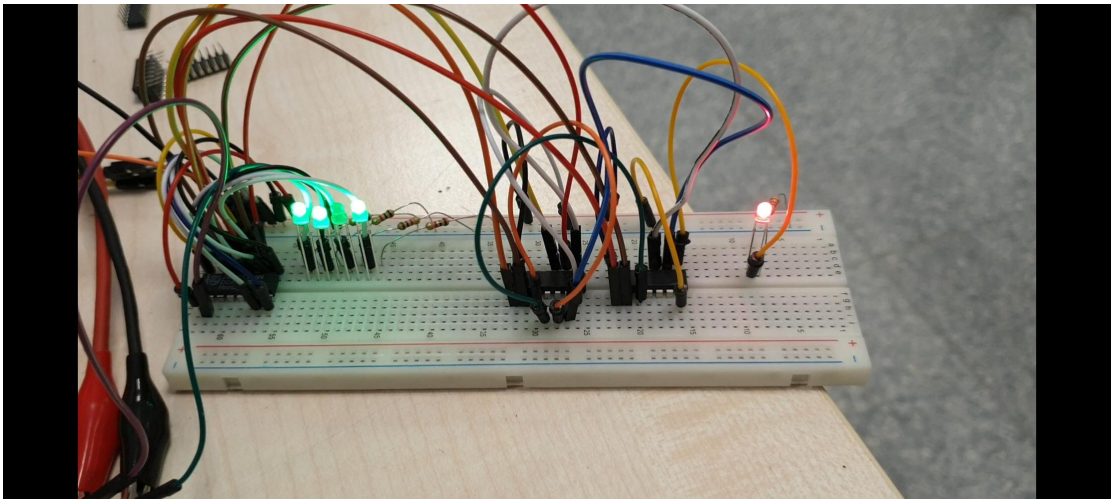

Figure 3.11 representing C=1, D=1, A=0, B=1 inputs and F=1 output.

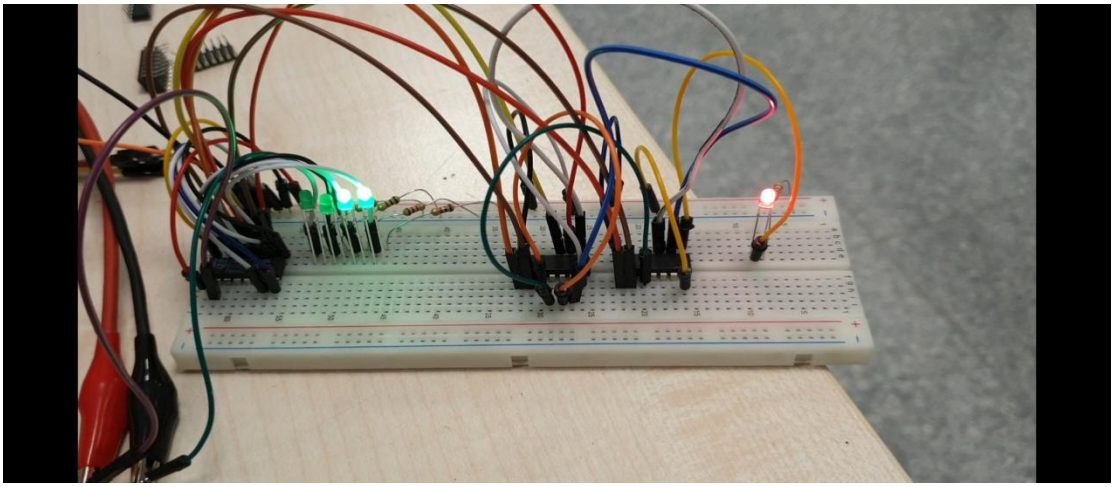

Figure 3.12 representing C=0, D=0, A=1, B=1 inputs and F=1 output.

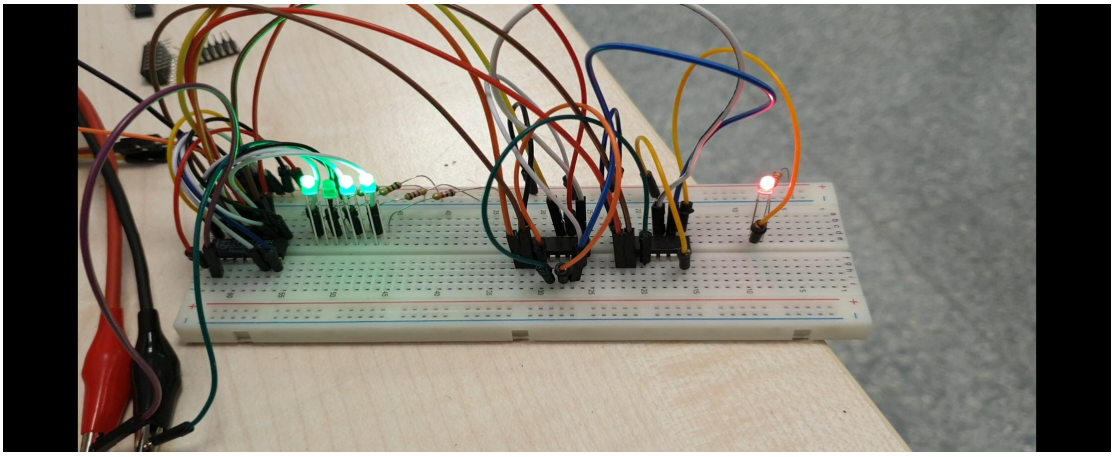

Figure 3.13 representing C=1, D=0, A=1, B=1 inputs and F=1 output.

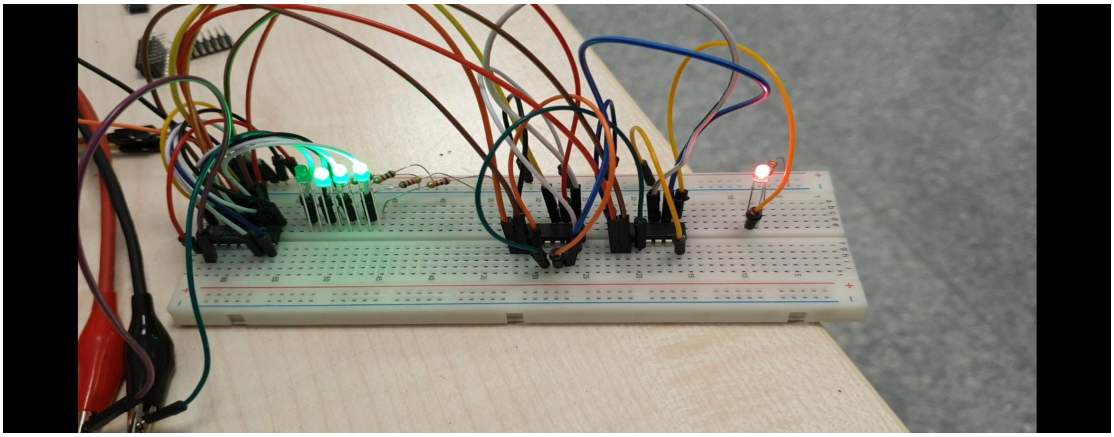

Figure 3.14 representing C=0, D=1, A=1, B=1 inputs and F=1 output.

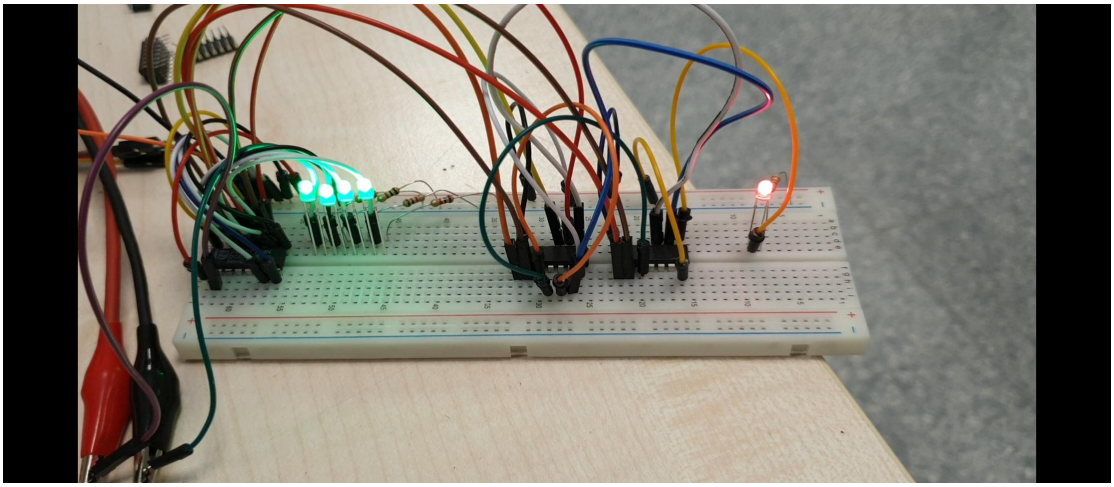

Figure 3.15 representing C=1, D=1, A=1, B=1 inputs and F=1 output.

Wave forms of the output compared with the VHDL test bench's function output signal (Figure 3.16) and the circuit constructed using IC's output signal monitored using oscilloscope (Figure 3.17) reveals that the designs are identical.

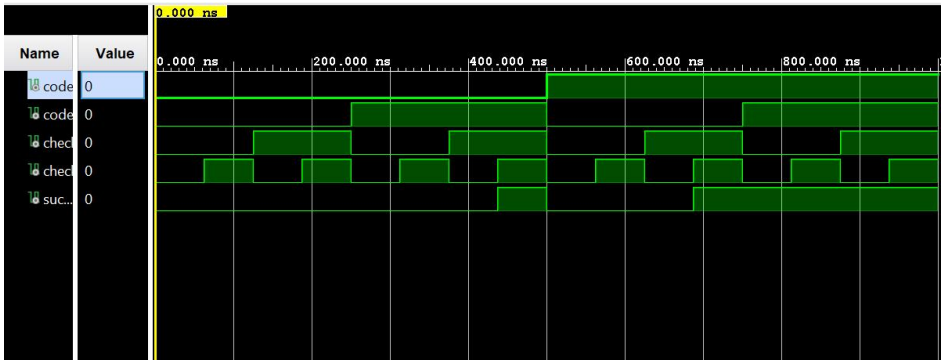

Figure 3.16 at the bottom the signal represents the output behaviour of the circuit

Figure 3.17 constructed circuit's output signal observed on the oscilloscope

4) Conclusion

We learned hoe to implement digital circuits using basic elements such as integrated circuits and counters. However, contrary to the implementation using FPGA this implementation required more testing and debugging especially counter did not work properly during the experiment and in several times it is needed to be changed. In conclusion we learned implementing combinational circuits using IC’s and monitoring their signals using oscilloscopes and LED’s.