DUKE UNIVERSITY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ECE 529
ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS

Spring Semester 2020.

FINAL PROJECT.

Assigned: April 15, 2020.
Due: at 12:00 Noon, April 28, 2020.

DESIGN PROBLEM 2:

Design of SRAM Cell and Read/Write Circuitry in 180 nm Technology

Hodges, Jackson, and Saleh,
Analysis and Design of Digital Integrated Circuits, 3rd Edition.
Pages 397 and 398.

- Note that, even though the statement of Design Problem 2 indicates that it is part 2 of Design Problem 1, the requirements of Design Problem 1 can be separated from those of Design Problem 2.
- In the errata file regarding Design Problem 1, in the third paragraph replace 5 fF with 10 fF and delete the sentence "You can assume that the clock period is 24 FO4 delays."
- In your 256×256 SRAM array, assume that each column has 256 rows and one sense amplifier.
- You are required to submit a report which includes your design, calculations, programs, simulation results (plots), and HSPICE input code. You must include circuit diagrams with clearly number-labeled nodes that correspond to your HSPICE input files.
- Simulate the waveforms on the bitlines and the internal node q and $\overline{q}$ for writing a '0' and writing a '1'.
- Simulate the waveforms on the bitlines and the internal node q and $\overline{q}$ for reading a '0' and reading a '1'.
- Upload all HSPICE input files and other computer code to your drop box on Sakai.