a)

Based on calculation

M2 = M1 = 3lambda is doable, so M1=M2 = 3lambda = 270nm M5=M6 = 2lambda = 180nm

M3=M4=4lambda = 360nm

Based on simulation

M1 M2 sizes are too small to hold Vq below VTN, therefore increases M1 M2 sizes to 4 lambda = 360nm = M3=M4

Figures:

c) If we assume the bitline is always acting like a supply voltage at Vdd, and initially, Vq = 0V, Vq\_bar = Vdd, then the current would flow through M3 and M1 during read operation. M3 would always be in saturation since Vbit = Vword = Vdd.

At t = 0, Vq = 0V, I = Id\_M3 = 4.01e^-4 A

At steady state, Vq = Vtn = 0.5V, I = Id\_M3 = 1.9e^-4 A

I\_ave = 2.968e^-4 A

(Calculation done in MATLAB)

d) C\_bit = C\_s/d + C\_wire + C\_contact = row\_number\*uC\_s/d\*W\_access + uC\_wirerow\_number\*W\_cell + uC\_contact\*row\_number/2 = 358.4 fF

(Calculation done in MATLAB)