a)

Based on calculation

M2 = M1 = 3lambda is doable, so M1=M2 = 3lambda = 270nm M5=M6 = 2lambda = 180nm

M3=M4=4lambda = 360nm

Based on simulation

M1 M2 sizes are too small to hold Vq below VTN, therefore increases M1 M2 sizes to 4 lambda = 360nm = M3=M4

Figures:

c) If we assume the bitline is always acting like a supply voltage at Vdd, and initially, Vq = 0V, Vq\_bar = Vdd, then the current would flow through M3 and M1 during read operation. M3 would always be in saturation since Vbit = Vword = Vdd.

At t = 0, the cell is turned off, ignoring subthreshold current, I = 0A

At steady state, Vq = Vtn = 0.5V, I = Id\_M3 = 190uA, compared with SPICE output I = 172.7uA

I\_ave = 9.6178^-5 A = 96.178uA, compared with SPICE output calculated average I\_ave = 86.35uA

(Calculation done in ‘ECE529\_FinalProject\_cd.m’)

(SPICE simulation done in ‘bit\_current.sp’)

d) Since there is also pull-up transistors on the bitline, we need to take into consideration their drain/source capacitance.

C\_bit = C\_s/d + C\_wire + C\_contact = row\_number\*uC\_s/d\*W\_access + 2\*uC\_s/d\*W\_pullup + uC\_wirerow\_number\*W\_cell + uC\_contact\*row\_number/2 = 362.9 fF

(Calculation done in ‘ECE529\_FinalProject\_cd.m’)

e) t\_disc = C\_bit \* delta\_V / I\_ave = 2.1737e-10 seconds = 0.679 ns

(Calculation done in MATLAB; used C\_bit and I\_ave from problem C and D)

f) t\_disc\_amp = C\_amp \* delta\_V\_amp / I\_bias = 1.5e-10 seconds = 0.15 ns

(Calculation done in MATLAB)

g) Take t\_read into account,