The George Washington University
School of Engineering & Applied Science
Electrical & Computer Engineering Department

Instructor: Prof. Louri
Semester: Fall 2022
Course: Computer Architecture & Design ECE 6005 / ECE 4535

Lab Assignment 2

Due Date: October 12

Instructions:

Submit **one report** (preferably pdf format) and **separate codes in plain text files**, please do not compress them to a zip file. In the report, include source code with comments to explain the key steps, figures of your analysis. Make sure your source codes in plain text files are executable. Your codes will be downloaded and executed on simulator for functional testing.

Problem 1 (60)

You are given three trace files and are asked to find optimal cache design for these applications. You can download three traces from the black board.

Write a script that will execute DineroIV with various parameters. Explain how each parameter of memory hierarchy affects the performance. In some cases, the relationship is complex. Describe the results you observe and report your analasyss using proper figures where needed.

a) Block Size

Use a unified L1 cache, size 1KB, 4KB and 8KB, one-way set associative. Block size is 16B, 32B, 64B, 128B, 256B. What conclusions can you draw from this experiment?

b) Associativity

Perform the measurements on a unified L1 cache, size 4KB, 8KB, 16KB, 32KB block size is 32B, associativity s=1,2,4,8, fully associative. What conclusions can you draw from this experiment?

c) Replacement policy

Examine an 8K-byte unified, 2-way associative cache with 16-byte blocks. What are the average miss ratios for LRU, FIFO, and random replacement policies? Examine the replacement policies by increasing the cache size to 16Kbyte. What conclusions can you draw from this experiment?

d) Unified and split caches

Compare the cache miss ratios of the following two systems:

- A system with a 32K-byte unified cache
- A system with a 16K-byte instruction-only cache and a 16K-byte data-only cache.

Assume the caches are 4-way set associative, LRU replacement policy and the block size is 32 bytes. What conclusions can you draw from this experiment?

e) Write Policy

Calculate the average memory access time (AMAT) for unified L1 cache size of 16KB, direct-mapped, LRU replacement policy and the block size is 64 bytes., with:

- write back policy
- write though policy

The hit time for cache is 1 clock cycle. Let the miss penalty be 50 clock cycles. What can you say about the performance of the write policy?

f) What is the optimal configuration of the memory hierarchy for each of the three traces? Do research on the memory hierarchy of any three modern computers. Rerun the simulation with the parameters from your research. Compare the result and the optimal configuration you found. Describe the results you observe.

[Hint:] In the lab, we learned how to write a script to run a program with different parameters. Now try to write another script, which grabs the data from different output files for analysis. Modify the simulator to show the result, if you need, without changing the functionality. Listed commands might be helpful:

grep cut tr echo cat

In addition, you may generate an output file as a .csv file for data processing. But it is out of scope for this lab assignment. You don't have to use this method.

Problem 2 (40)

a) Take a look at the Arm Cortex-M7-based STM32H7 MCU series and report the cache size for it. (https://www.st.com/content/st_com/en/products/microcontrollers-microprocessors/stm32-32-bit-arm-cortex-mcus/stm32-high-performance-mcus/stm32h7-series.html)

b) Compare the cache performance of the following three systems:

- A system with a 256K-byte unified cache
- A system with a 64K-byte L1 cache and a 192K-byte L2 cache.
- A system with a 32K-byte L1 instuction cache and a 32K-byte L1 instuction cache and 192K-byte L2 data cache
- A system with a 32K-byte L1 instuction cache and a 32K-byte L1 instuction cache and 192K-byte L2 data cache

Draw the schematic of these cache hierarchies. Assume the caches are 2-way set associative, FIFO replacement policy and the block size is 32 bytes. What conclusions can you draw from this experiment? Do reseach on adding cache levels for data and instcuction and analyze its performance. Figures are preferred.