The George Washington University
School of Engineering & Applied Science
Electrical & Computer Engineering Department

Instructor: Prof. Louri
Semester: Fall 2022
Course: Computer Architecture & Design ECE 6005 / ECE 4535

Lab Assignment 4

Due Date: December 6

Instructions: Submit **one report** (preferably pdf format) and **separate codes in plain text files**, please do not compress them to a zip file. In the report, include source code with comments to explain the key steps, figures of your analysis. Make sure your source codes in plain text files are executable. Your codes will be downloaded and executed on simulator for functional testing.

The **purpose** of this assignment is to give you experience runing a benchmark ont the Gem5 and Dinero IV simulator.

Step 1: Compile Three Benchmarks

Mibench is a set of benchmarks designed to evaluate the performance of embedded system designs. Compile these three Mibench programs with and without optimizations (for X86 architecture).

consumer/cjpegLarge

office/stringsearchSmall

security/blowfishSmallE

Step 2: Run on Gem5 and get the memory trace

Run compiled binaries on X86 architecture with Gem5 simulator, a timing CPU, and the default memory system. You can use the Se.py design. Save the memory trace to a text file (.txt).

Step 3: Using Dinero IV find the optimum cache hierarchy

Using any programming language, turn the.txt file into a Dinero IV-readable trace file. Run the Dinero IV on those memory traces with different cache parameters (cache size (up to 4kb), cache

line size (up to 256b), associativity, replacement policy) to determine the best cache hierarchy for each of the applications. Report the cache hit/miss rate.

Step 4: Design your cache hierarchy in Gem5 and simulate the programs

Implement your memory hierarchy for each of those applications and run your program on the Gem5. Report performance improvements. For each application, draw the optimum cache hierarchy.