The George Washington University
School of Engineering & Applied Science
Electrical & Computer Engineering Department

Instructor: Prof. Louri
Semester: Fall 2022
Course: Computer Architecture & Design ECE 6005 / ECE 4535

Lab Assignment 1

Due Date: September 28^{h}

Instructions:

Submit **one report** (preferably pdf format) and **separate codes in plain text files**, please do not compress them to a zip file. In the report, include source code with comments to explain the key steps, screenshots of WinMIPS64 simulator (if asked), and necessary analysis. Make sure your source codes in plain text files are executable. Your codes will be downloaded and executed on simulator for functional testing.

Problem 1 (50)

1- Assume a five-stage single pipeline (IF, ID, EX, MEM, and WB) microarchitecture. Given the following code,

a) Write a piece of assembly code that execute

```
For (i=12, i<15, ++i) {
        C= 2*A + 4*B + 1
        if (C is odd)
                print(C)
        if (C is even)
                print(C/2)
}
```

and also stores the result(C) inside memory. Choose integer values for A = 2063 and B = 36725 and read them from memory.

b) Draw the pipeline diagram of one iteration of the code, and report the cycle per instruction (CPI). the number of cycles, stalls, etc. (Screenshots acceptable)

c) Change delay for multiplication unit to 6 cycles. Analayze impact of this on CPI. draw the pipeline diagram again and report the CPI. Analyze the impact of data access latency on CPI

d) If it is possible, increase your program's efficiency and report new CPI.

e) What are differences between single precision and double precision? How the statistics alter by changing value types to double precision?

Problem 2 (50)

Write a program that can calculate the factoriel of a number (n!). Factoriel is very useful for when we're trying to count how many different orders there are for things or how many different ways we can combine things. For example, how many different ways can we arrange n things? We have n choices for the first thing. For each of these n choices, we are left with n-1 hoices for the second thing, and so on. Write a computer program that can compute the factorial of integers up to 15. Then, divide it by n. Put n equal to 8.

a) Implement your code with WinMIPS64 assembly language.

b) Derive the ideal (without any stalls) CPI of your code, and run your code in WinMIPS64 simulator to obtain and report the real CPI.

c) Analyze the cause of the difference between theoretical and real CPIs and demonstrate your analysis with corresponding pipeline diagrams captured from the simulator.

d) The assumption of accessing data memory in one clock cycle is often considered too ideal. Assume we implement a data cache with a hit latency of 3 cycles (assume 100% hit rate), draw the pipeline diagram again and report the CPI. Analyze the impact of data access latency on CPI.