The George Washington University
Depart of Electrical and Computer Engineering

ECE 6213
Fall 2023
Dr. Matthew LaRue

Project 3: Elevator Controller FSM

Design an elevator controller FSM for a three story elevator. Required inputs/outputs are listed below. The FSM will interface with an elevator button Verilog block that I will provide.

Inputs:
Clock, reset_n
Floor 1 up button
Floor 2 down button
Floor 2 up button
Floor 3 down button
Elevator floor 1 button
Elevator floor 2 button
Elevator floor 3 button

Outputs:
Floor 1 (indicates elevator is on floor 1)
Floor 2
Floor 3
Elevator door open
Floor 1 up button clear (explanation for all the "clear" signals are below)
Floor 2 down button clear
Floor 2 up button clear
Floor 3 down button clear
Elevator floor 1 button clear
Elevator floor 2 button clear
Elevator floor 3 button clear

All 7 elevator button inputs to your FSM will connect to the provided elevator_button.v module. When the "button pressed" input to elevator_button.v goes high, the button pressed output of the module will stay active until the corresponding "button clear" signal goes high.

The only functional requirements that I am giving that it functions like a normal three story elevator. Spend time thinking about how elevators operate (or ride one for a while) to develop the functional requirements.

Deliverable 1: Due Thursday, September 21
Provide the initial state transition diagram for your elevator FSM.

Deliverable 2: Due Thursday, September 28

1. Elevator FSM Verilog code
2. Testbench that *fully* demonstrates elevator functionality
3. Simulation waveforms demonstrating all functional requirements are met
    a. Make sure the waveforms are legible
4. Provide the final state transition diagram for your elevator FSM.
    a. If the final FSM is different from your deliverable 1 FSM, provide details on what changed and why (ie. simulations showed a testcase that didn't operate properly)