Neural Spike Detection/Sorting Circuit Design

ENEE611 Final Project

Yihui Wang

12/18/2024

1) Introduction

a) Project Overview

This project involves designing a custom Analog MOSFET Circuit to detect and sort neural spikes from analog voltage signals. The primary objective is to develop a system capable of identifying specific neural events from recordings obtained via an array of electrodes. This task is critical for advancing neural recording technologies, particularly in the context of neural prostheses, where accurate and efficient spike detection is essential for interpreting neural activity.

b) Motivation

The motivation behind this project stems from the need to support research in neural recording laboratories. Neural spike detection and sorting are fundamental processes in neuroscience research, enabling researchers to understand the electrical activity of neurons. This understanding is crucial for developing artificial neural peripherals like prostheses, which can restore lost sensory or motor functions in individuals with disabilities. By automating the process of recording from thousands of microelectrodes, this project aims to enhance the efficiency and accuracy of neural data collection, paving the way for more sophisticated neural interfaces.

c) Problem Statement

The core challenge addressed in this project is the detection and classification of neural spikes from voltage recordings obtained from an array of four electrodes. Due to imprecise manufacturing and physical distortion during implantation, the relative positioning of these electrodes is unknown, complicating the task of spike detection. Neural spikes appear as bipolar voltage events whose amplitude varies with the distance of the neuron from the electrode. These spikes typically manifest simultaneously on multiple electrodes, with their amplitudes serving as the primary cue for identifying the firing neuron. The project involves developing a circuit that can learn to recognize these spikes and accurately classify them during a test phase.

d) Project Goals

The main goal of this project is to design an Analog Circuit using MOSFETs that can accurately detect and classify neural spikes from analog voltage recordings. The chip must be capable of learning the characteristics of each neuron's spike during a training

phase and then recognizing these spikes during a test phase. Success is measured by the circuit's ability to correctly identify the firing neurons in the test recordings. The project also aims to ensure that the design is robust and adaptable, capable of handling different datasets without requiring modifications to the circuit.

2) System Design

The initial plan was to use the Sample and Hold circuit and Vmax circuit to store the peak value of the electrode signals and compare the real-time signals with it in the bump circuit, then use the WTA circuit to decide which line has the highest current, which will be the summation of 4 bump circuit output. However, from observing the signal of the electrode, I can see that the peak values when each neuron is firing are different, as shown in the figure:

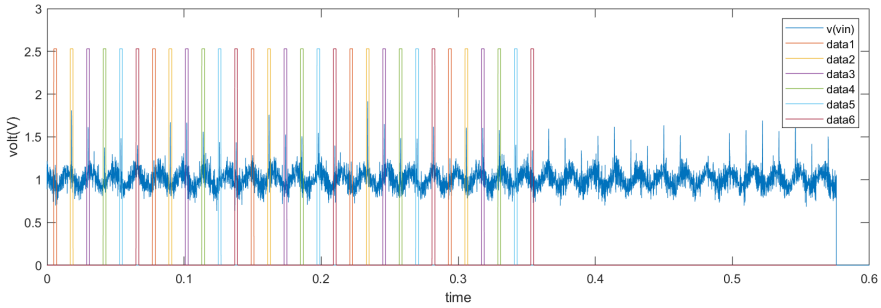

Figure 1 Channel 1 electrode signal compared to 6 neurons teach signals

With this drawback, I take advantage of digital system design and use the spikes of 4 electrodes as each neuron's fingerprint instead of the spikes' actual voltage value. The rest of the system remains the same using the Bump Circuit and WTA Circuit. The other important thing I need to notice is that the given electrode signals have strong observable noise which should be filtered before any following process to get precise results and reduce power consumption by making the signal simpler.

With a picture of that, there could be some challenges that I expect from the process of designing the circuit. The first thing will be the spike detector, should I use a simple one-threshold comparator or use a hysteresis comparator to reduce the noise but increase the power? For the sample-and-hold circuit, how should I design the Vmax function, and how to make sure the stored value of voltage in the capacitor won't change server during the hold stage? With using CMOS technology, I will see some leakage with capacitors. It is also critical to find reasonable values for the Bump and WTA bias current to be clear

and high enough but not consume too much power output. With all of that idea of how the system works and the challenges I might face, a system block diagram can be drawn at first for us to divide and conquer:

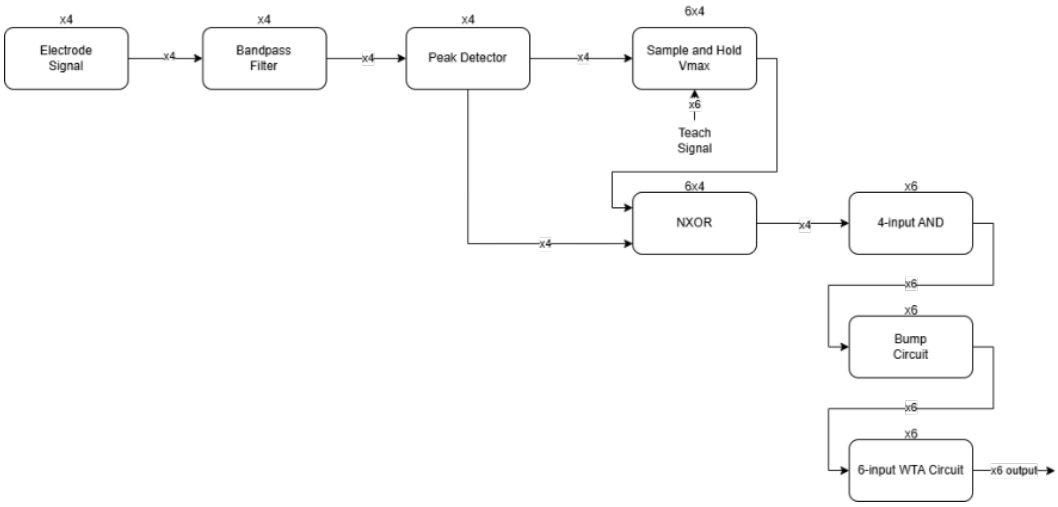

Figure 2 Top-level system design blocks

3) Circuit Design and Implementation

a) Transamp

Transamp can transform the difference between two voltage inputs to a current signal or simply a voltage signal, in our project the transamps are mainly being used as voltage followers or substitutions for resistors to save space. The circuit design of transamp is directly copied from homework resource, which contains 5 transistors:

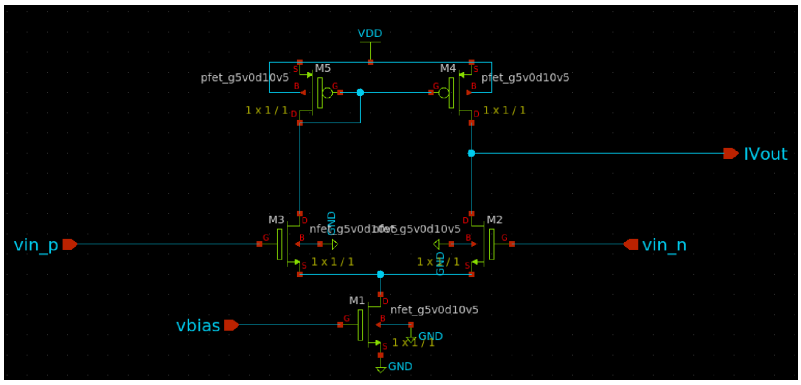

Figure 3 Transamp circuit

One of the most important things for using a transamp is to make sure it is working in the saturation stage, by simulating the Xschem with following setup:

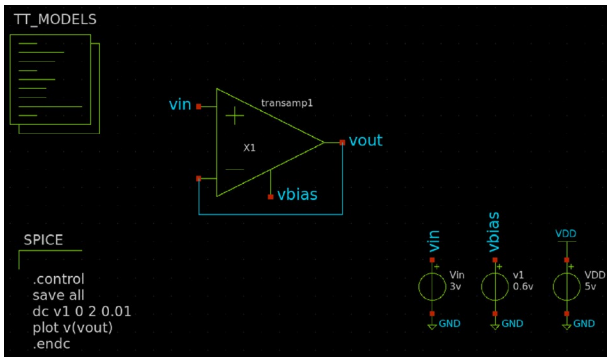

Figure 4 Simulation setup for Transamp

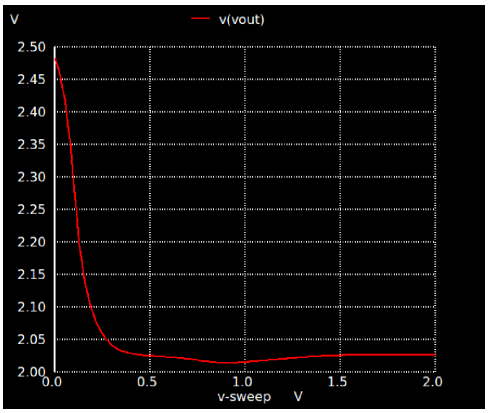

Figure 5 DC sweep with Vbias of Transamp

From the result I can see that with a bias voltage higher than 0.5V, I can have great follower characteristics, By setting up the bias the 0.6V and doing the DC sweep with Vin I can have the dynamic range of the input voltage for reference:

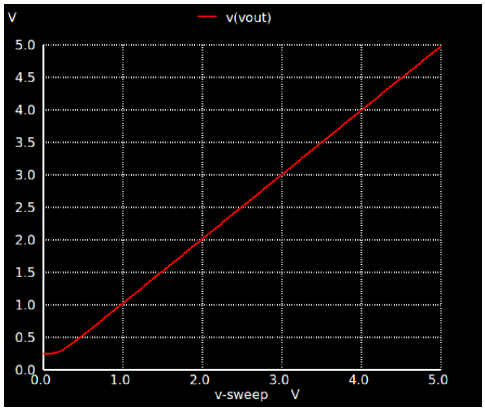

Figure 6 The effective input range of transamp with bias of 0.6V

From the simulation result, I can see that the transamp has great following function with a bias of 0.6V and an effective input range of 5V at least.

b) Bandpass Filter

A Bandpass Filter is the combination of a High pass filter and a Low pass filter, in this project I need to prevent using resistors so I are using transamps as the substitution for resistors and the relationship between bias voltage and effective resistance it, which I know is negatively related. Before starting designing the filter, I need to know the frequency components of the signal:

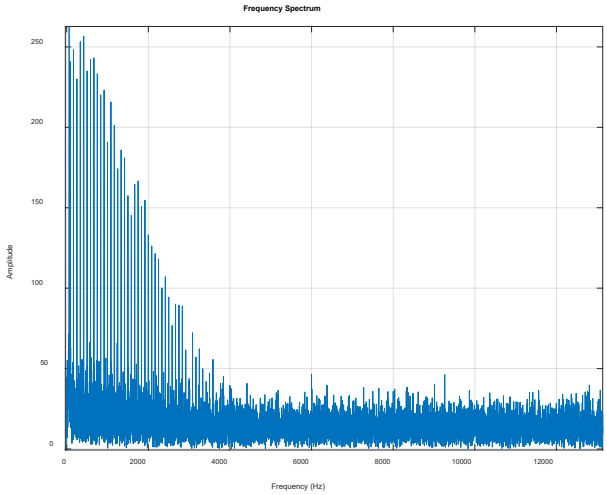

Figure 7 Frequency spectrum of electrode signal of channel 1

According to the observation, a range from 500Hz to 2500Hz seems to be a reasonable choice to filter all the high-frequency noise and the 60Hz radio noise. The high-pass filter should be applied first to limit the signal's magnitude given the fact that most of these signals are low-frequency signals, so that the voltage range of signal won't exceed the effective range of the transamp. A Sallen-key Active High-pass filter has been design for this project:

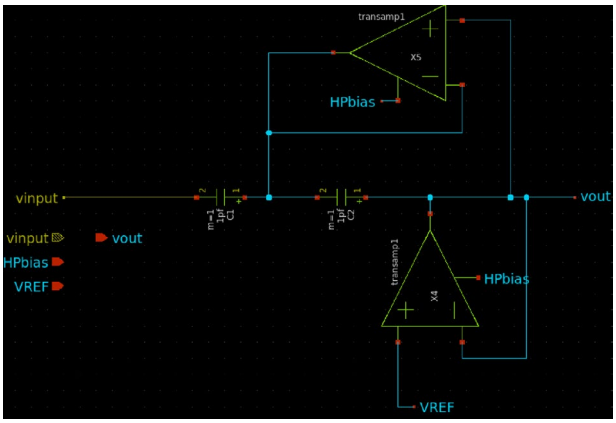

Figure 8 Sallen-key High-pass filter

To make life easier, I let effective resistance and capacitance be the same, and I can have the equation of the cut-off frequency:

$$f_C = \frac{1}{2\pi RC}$$

Figure 9 Cut-off of Sallen-key HP filter

The following bode plot shows the cut-off frequency:

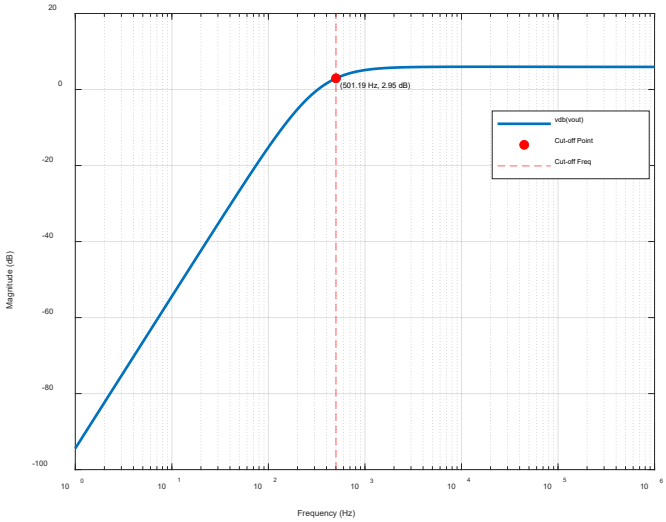

Figure 10 Bode plot of High-pass filter

A second-order low-pass filter is designed in the following way, which can also change the cut-off frequency by adjusting the resistance and capacitance:

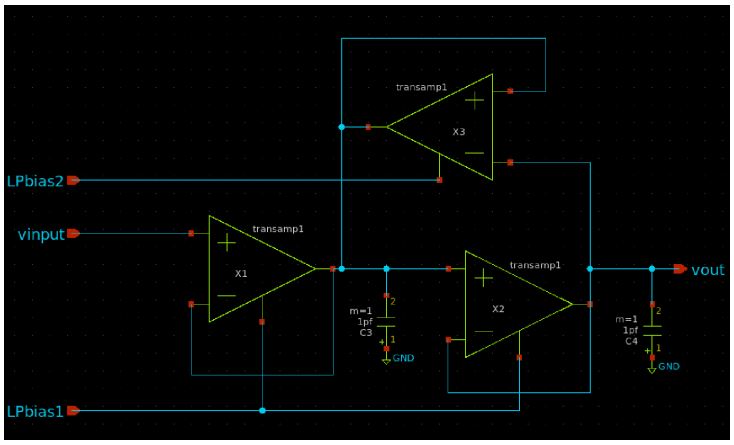

Figure 11 Second order Low-pass filter

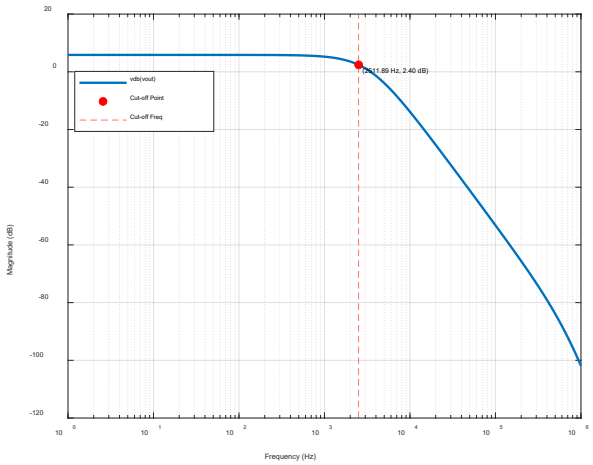

Figure 12 Bode plot of Low-pass filter

Combining the two filters together, I can have the bandpass filter for the frequency range from 500Hz to 2500Hz. The other benefit of using an active filter is that the signal with the frequency I care about will be enhanced and the noise will be weakened at the same time, which means the voltage during the spike will be stronger and it makes it easier for the peak detector to detect. The following figure shows the filtered signal compared to the original signal:

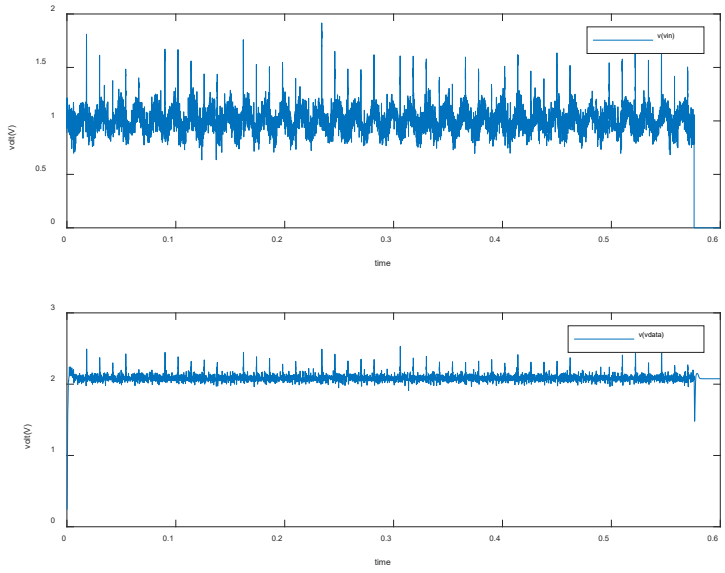

Figure 13 Electrode 1's signal after bandpass filter

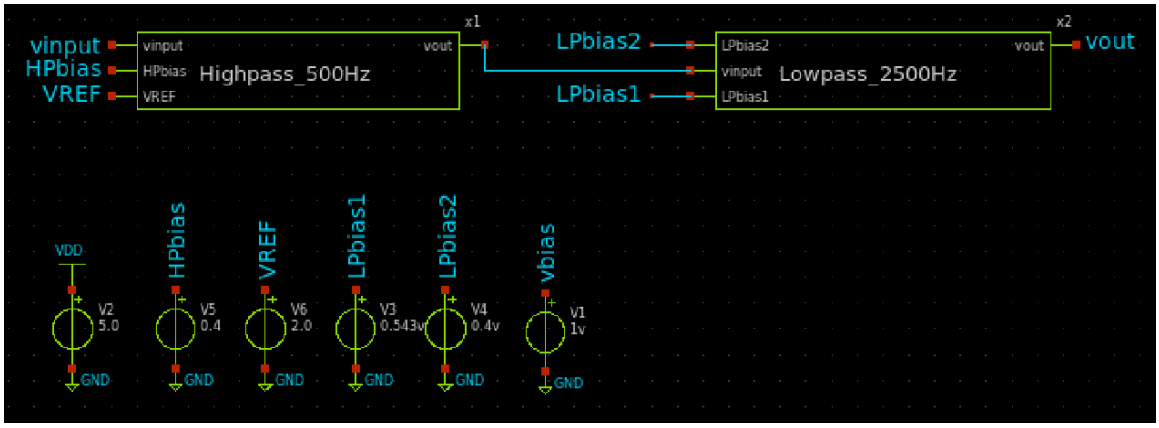

Figure 14 Bias voltage setup for the bandpass filter

c) Peak Detector

As mentioned above I are going to use the spike information of each electrode to decide which neuron is firing, however from the following plot I can see that even for the same neuron, the spike voltage values from the electrode's record are different, so a Peak Detector is needed to test if this electrode generates any spikes, and use this spike outputs to train the sample-hold circuit and all the following step.

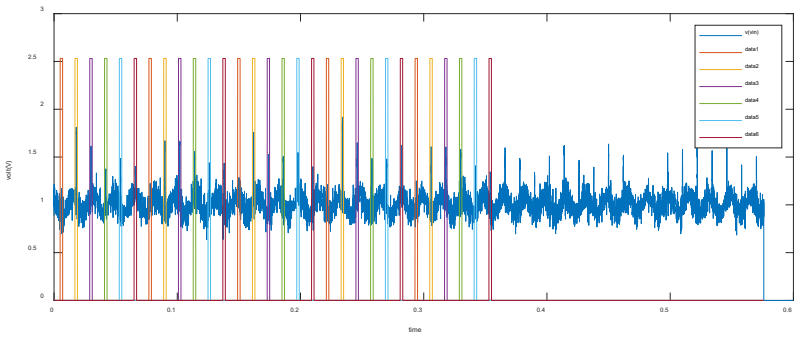

Figure 15 Electrode channel 1 compared to neurons firing signal

In order to have the ability to detect a spike, I need a comparator with a specific threshold voltage, I also need another threshold to give a hysteresis mechanism to filter the noise and have a much cleaner spike output. I chose to use a Schmitt Trigger to do this job since it is easy to build and tune for specific threshold voltage. The design I use is from [1]'s work:

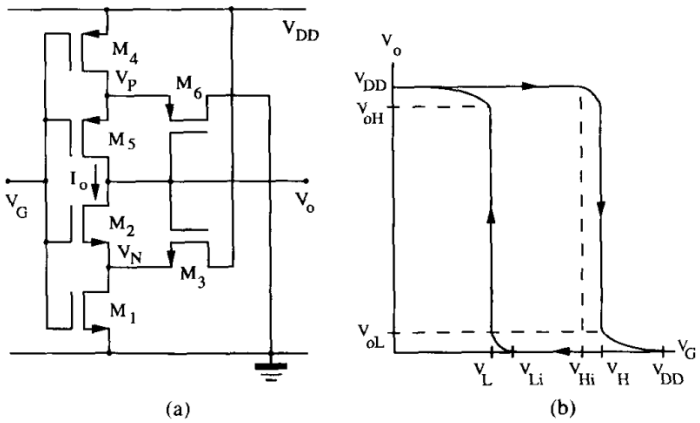

Figure 16 Schmitt Trigger circuit and characteristic

$$\frac{k_1}{k_3} = \left(\frac{V_{DD} - V_{Hi}}{V_{Hi} - V_{TN}}\right)^2$$

$$\frac{k_4}{k_6} = \left(\frac{V_{Li}}{V_{DD} - V_{Li} - |V_{TP}|}\right)^2$$

Figure 17 Equations of CMOS Schmitt Trigger

By sizing the W/L ratio of transistors accordingly, I can have the following design:

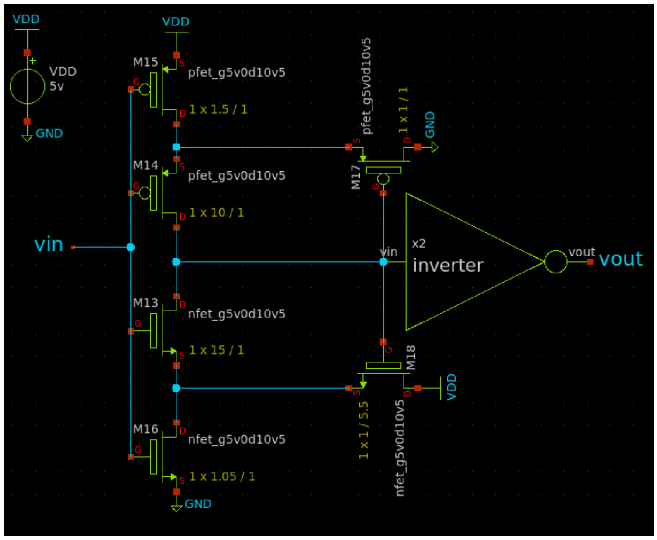

Figure 18 Schmitt Trigger circuit design

With the simulation result, I can see the corresponding threshold voltages:

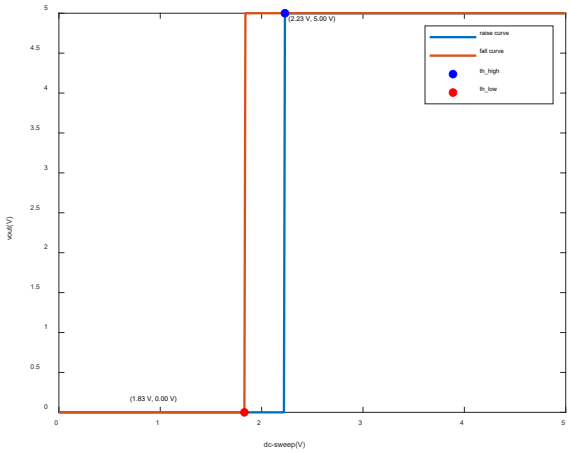

Figure 19 DC Simulation of Schmitt Trigger

From Figure 13, I can see that these threshold voltages can cover all the spikes. With the following simulation setup, I can have the spike outputs from the filtered electrode signal:

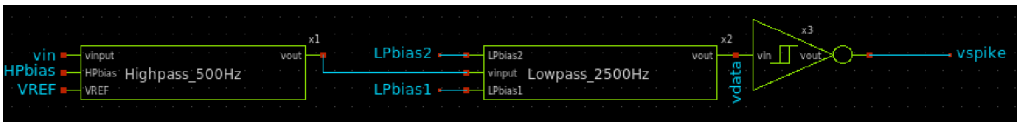

Figure 20 Bandpass filter and Schmitt Trigger Peak Detector

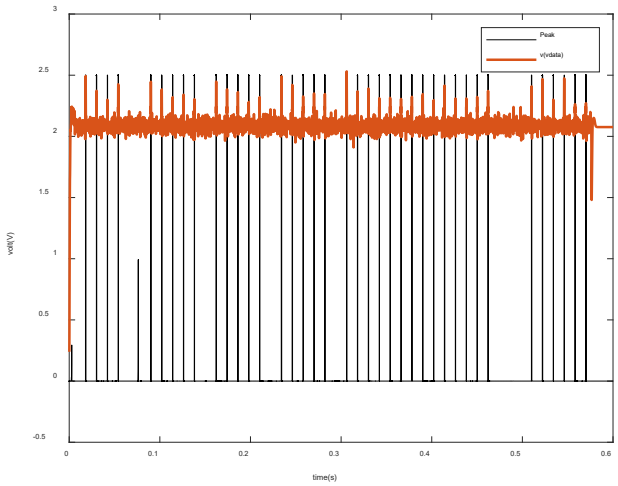

Figure 21 Peak Detector output compared to filtered electrode signal

The voltage level of peak output is divided by 2 for better observation. The output spike will be used for Vmax sample-and-hold and comparison in bump circuit.

d) Transmission Gate

Using a transmission gate as a switch in our design has significant advantages due to its low on-resistance, achieved by the complementary action of NMOS and PMOS transistors, which reduces voltage drop and power loss across the switch; its ability to handle a wide range of input voltages, from 0V to the supply voltage ensuring compatibility with different signal levels; its minimal signal distortion, as it can effectively pass both high and low logic levels, maintaining the integrity of the signal; and its complementary control mechanism, which ensures that the gate can be fully turned on or off, providing a clear and efficient switching operation. The Transmission gate is being used in the Sample-and-Hold Circuit, and it can minimize its effects on the signal I are interested in during the sample. The design and the simulation result are as follows:

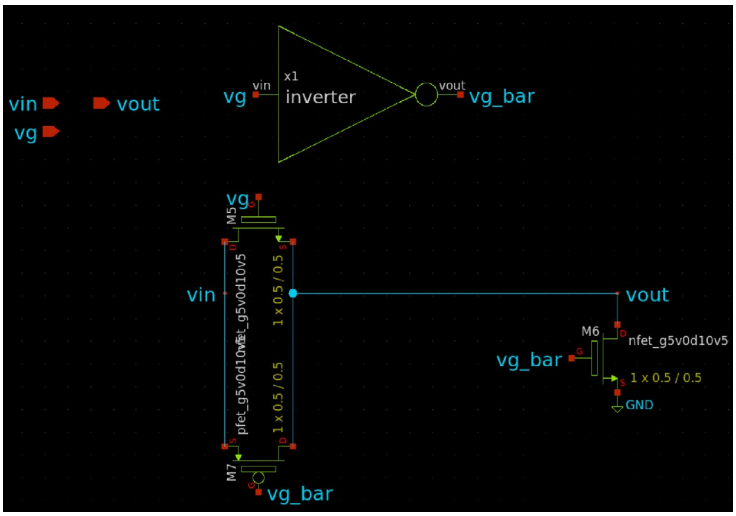

Figure 22 Transmission gate circuit

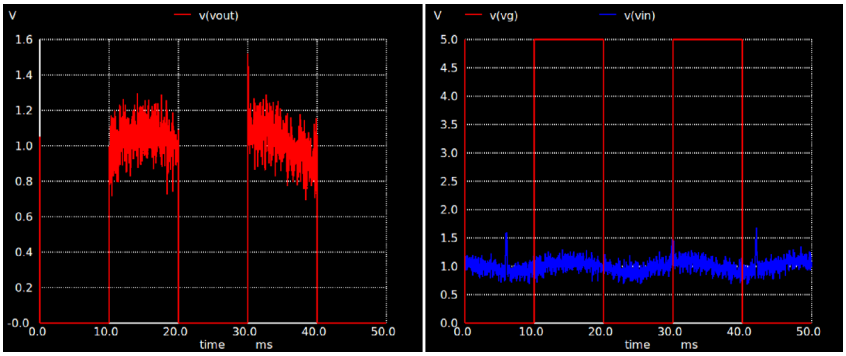

Figure 23 Simulation result of Transmission Gate

From the simulation, I can see that using a transmission gate as a switch can minimize the voltage spikes during the switch and make a clean output, which is highly close to the original input data.

e) Vmax Sample-and-Hold Circuit

To have the ability to detect which neuron is firing, I need to store the corresponding spikes of each electrode when the neurons are firing during the teach signal stage so that I can compare them as a fingerprint of each neuron during the test stage. A Vmax sample-and-hold circuit is the best choice for this task, because I want to record the spikes when the teach signal is on, and I don't want to record anything if the teach signal is off. I are using the teaching signal as the sample stage control signal for the S&H circuit. A circuit design is as follows:

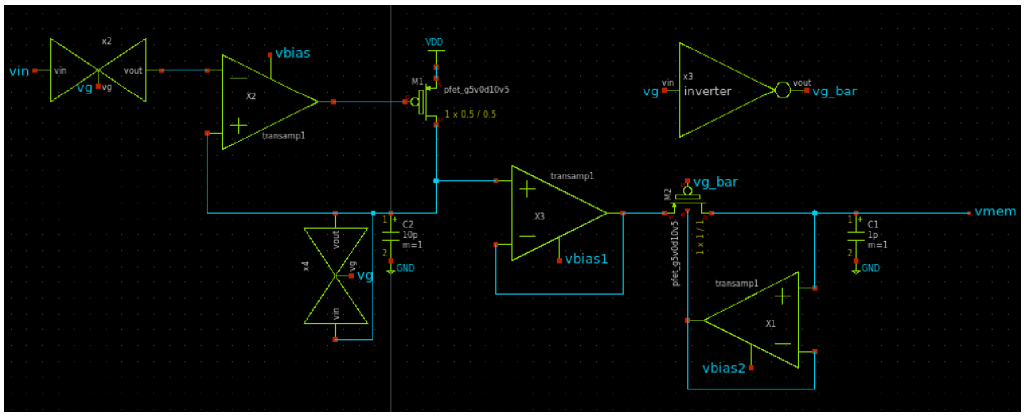

Figure 24 Sample-and-Hold circuit

Closed loop feedback has been implemented in this design so that the PMOS M1 will only be turned off when the voltage level at +input is equal to or bigger than the voltage level at -input because only in that situation will the output voltage level go to vdd and shut off the M1. In addition, a hold circuit with a biased-body PMOS is implemented to keep the voltage value stored with very little leakage current. A simulation as follows can show the ability to sample the maximum voltage and store it:

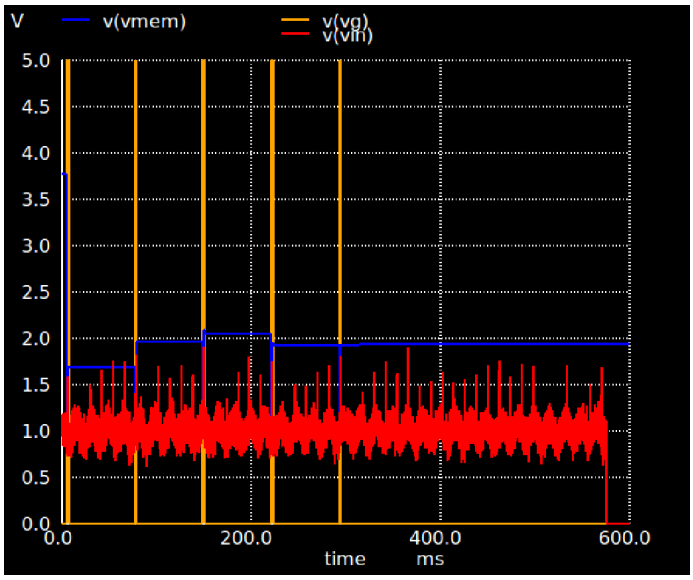

Figure 25 Sample-and-Hold circuit simulation

It is worth noting that there will be an offset every time it stores a peak value, which is caused by the parasitic capacitor in the PMOS every time it gets turned on, the charges in the caps will inject into the storage cap and make it higher than the original voltage. The reason why I can't use the original electrode signal to train this is because it seems like the offset each time is different, which will be fatal if it goes into a bump circuit with the real-time signal. After all, it will output the wrong result. One of the benefits of combining these two sample-and-hold circuits is that they can have very little leakage current after the maximum voltage has been stored, even with the offset.

f) Inverter

An inverter is needed for digital logic reversion and buffer, the CMOS design and simulation are as follows:

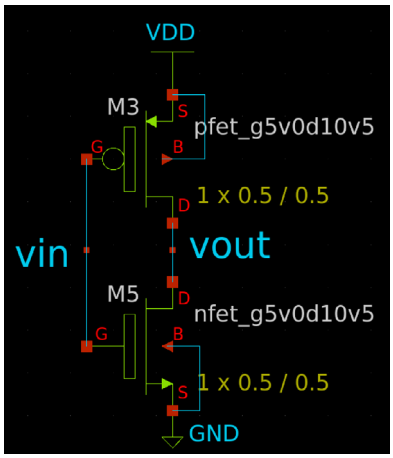

Figure 26 Inverter circuit

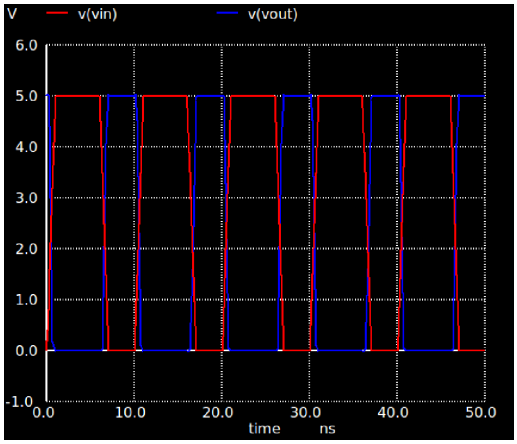

Figure 27 Inverter Simulation

g) NXOR and AND Gate

Since I am using the stored spikes to compare with the real-time output spike from 4 electrodes for 6 neurons, I simply use an NXOR gate to compare each electrode channel and use these 4 outputs as the input to a 4 input AND gate to see if this neuron is firing. The circuit design of NXOR and AND gate are as follows:

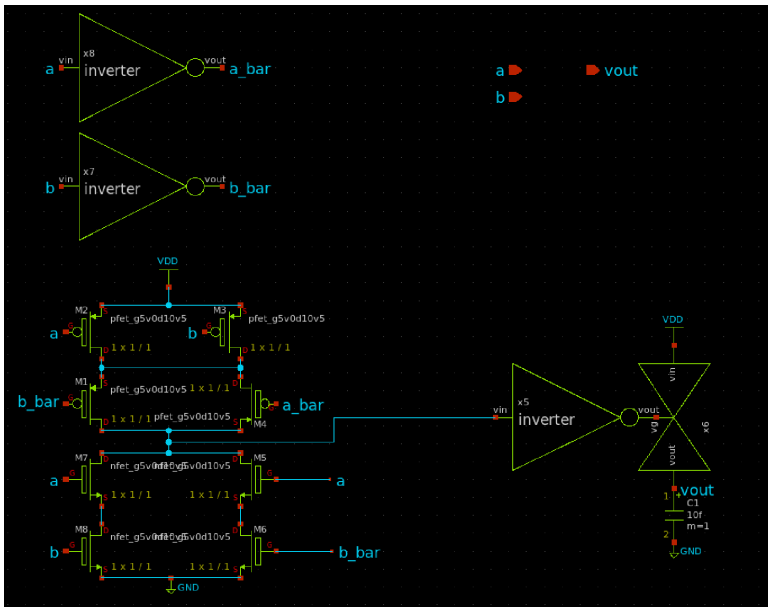

Figure 28 NXOR Gate circuit

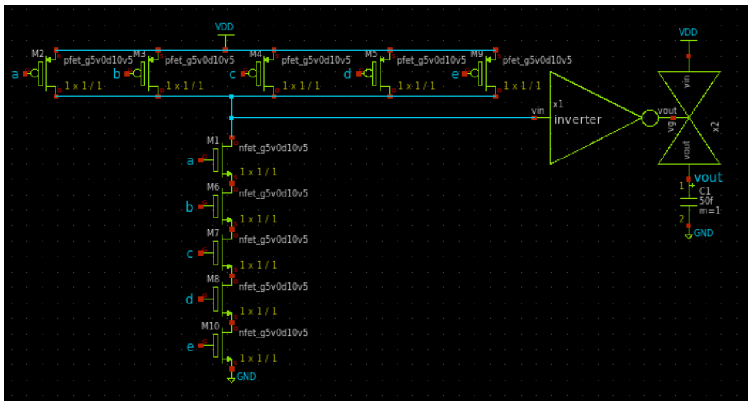

Figure 29 AND Gate circuit

Capacitors and transmission gates are implemented to decrease the voltage spike during the transition of gates, but it needs to be emphasized that this only works with low-speed applications, like this project, otherwise, the high-speed signal will be filtered.

h) Bump Circuit and WTA Circuit

To transform the comparison result from AND gate to current, I decided to use a Bump circuit not only due to its ability to output correlation of the inputs, but also because I am still trying to use the original data as the comparison sources, but I couldn't make it.

The output of the bump is copied to the WTA input by a PMOS current mirror for the following use. For each neuron, there will be 4 bump circuit outputs for each electrode channel, I need to add them together as the input of WTA.

Since I have the summation of 4 bump circuits for each neuron, I need to use WTA to decide which neuron has the highest current. Thus, for the WTA circuit, I need to have 6 lines plus 1 reference line to set a threshold that only the line has the current that is higher than the threshold can win. The example design that has one bump circuit input to a 2-line WTA circuit is as follows, as well as the simulation:

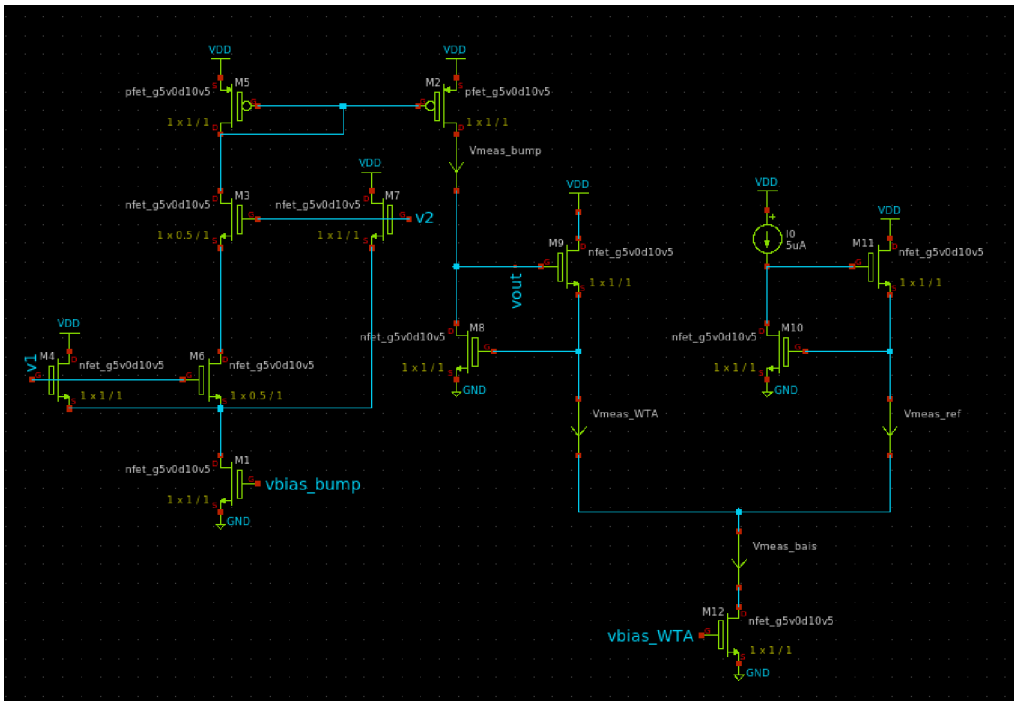

Figure 30 Bump circuit and WTA circuit

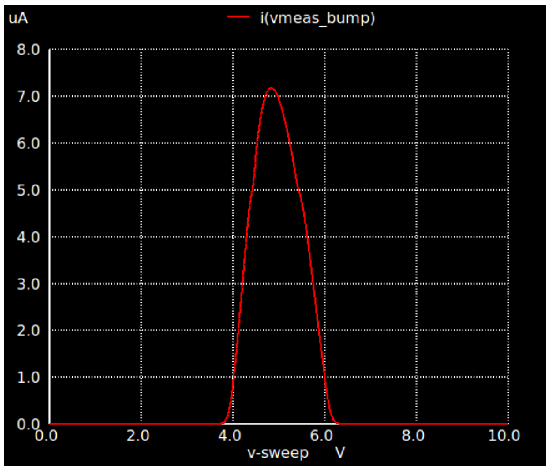

Figure 31 Output of Bump circuit with 5v(vdd) reference

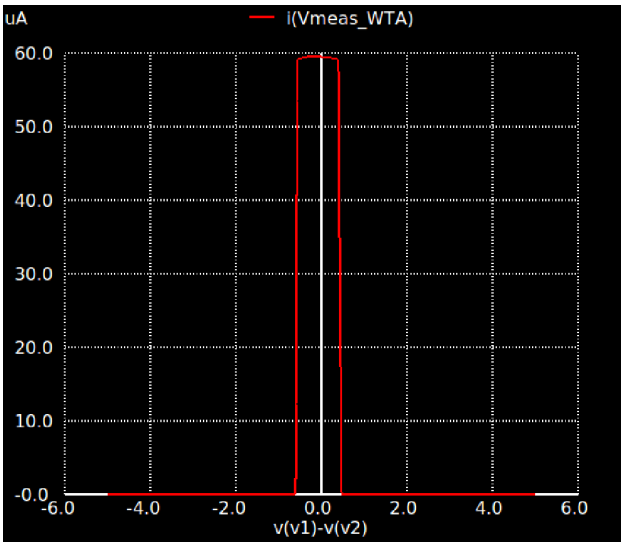

Figure 32 Simulation result of WTA current of the interested input line

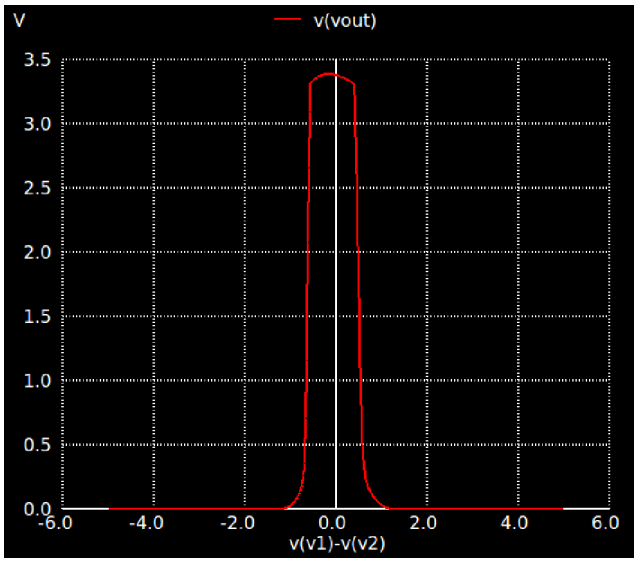

Figure 33 Simulation result of WTA output of the interested input line

One of the great things about using WTA is that I can easily get the output voltage without using some kind of current-to-voltage circuit.

i) Top-Level Circuit

With all the components I designed above, now I can combine them and make a spike detector/sorter for the neurons. Firstly, I need 4 bandpass filters to filter the original signal from the electrodes and connect it to a peak detector to output the peaks, then I need 4by6 Vmax sample-and-hold circuits to hold the corresponding peak value of each electrode for each neuron. Secondly, I need to connect the sample-and-hold and the corresponding output of peak detectors to see if the fingerprints match each

neuron. Finally, there will be 6 added bump circuits that have current output going to the input of the WTA circuit. The data filtering block, sample-and-hold block, bump, and WTA block, and all of the bias voltage blocks are shown below:

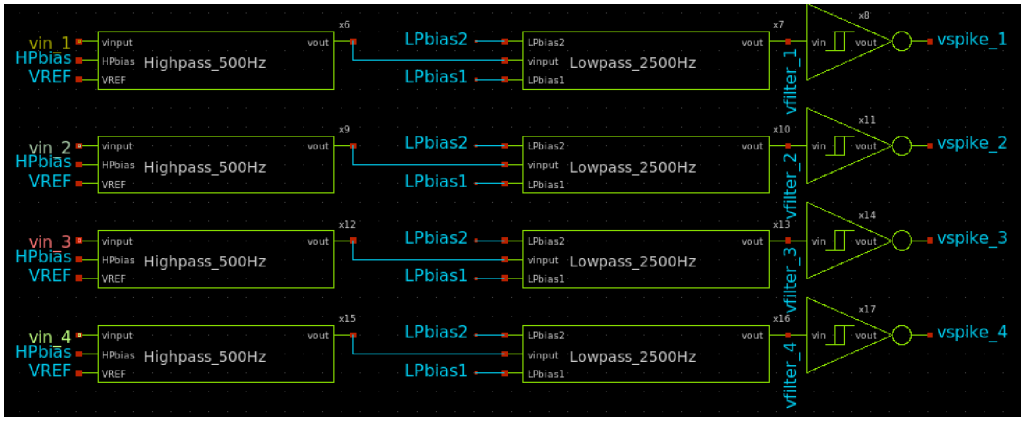

Figure 34 Filtering and Peak Detector Block

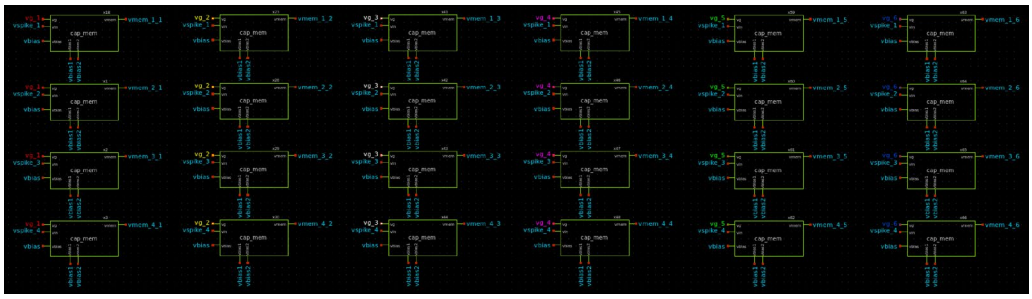

Figure 35 Vmax Sample and Hold Block

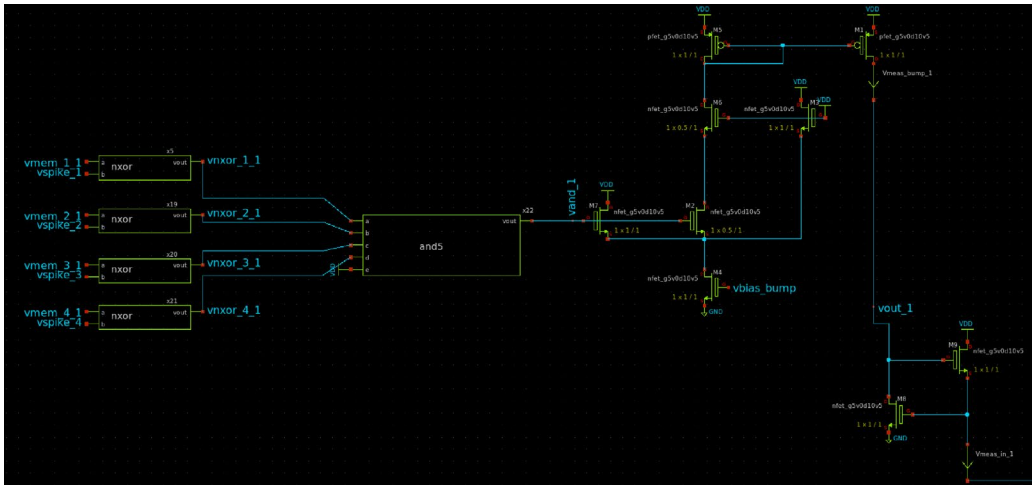

Figure 36 Firing Detector Block for one neuron

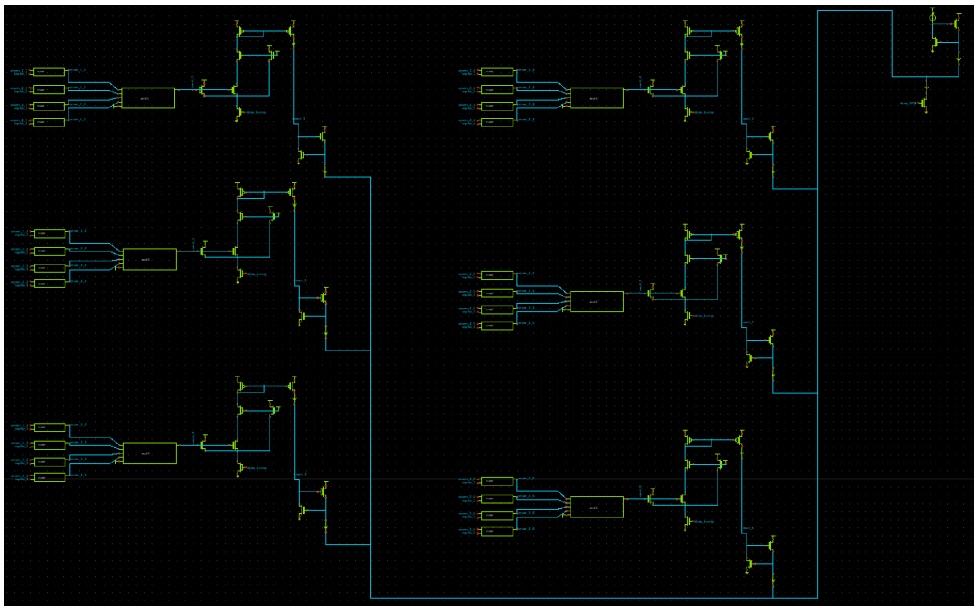

Figure 37 Firing Detector Block with WTA output

4) Neuron Spike Detection Results

The results of 6 neurons are shown below. I can see that with the system I designed, each neuron can successfully output the firing status during the teaching signal, but there will be error firing as well. The output of each neuron is shown below:

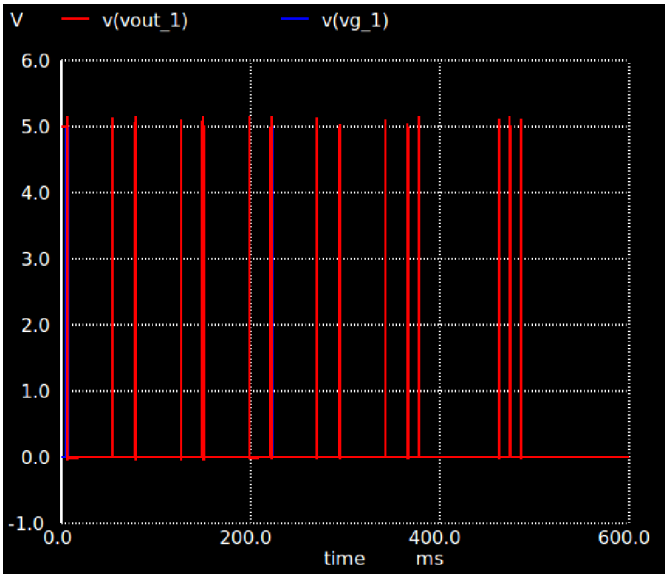

Figure 38 Output of neuron 1

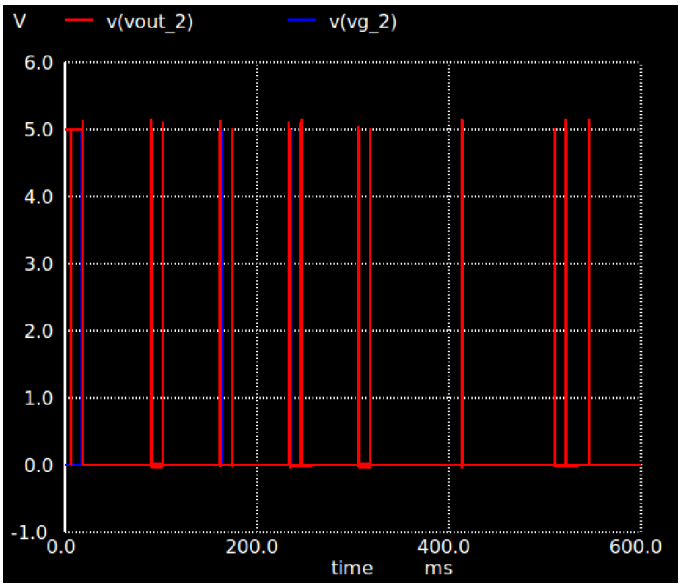

Figure 39 Output of neuron 2

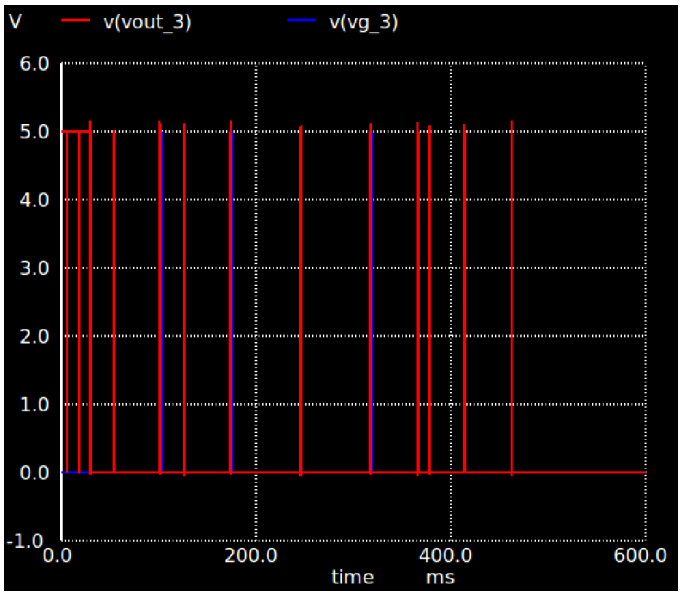

Figure 40 Output of neuron 3

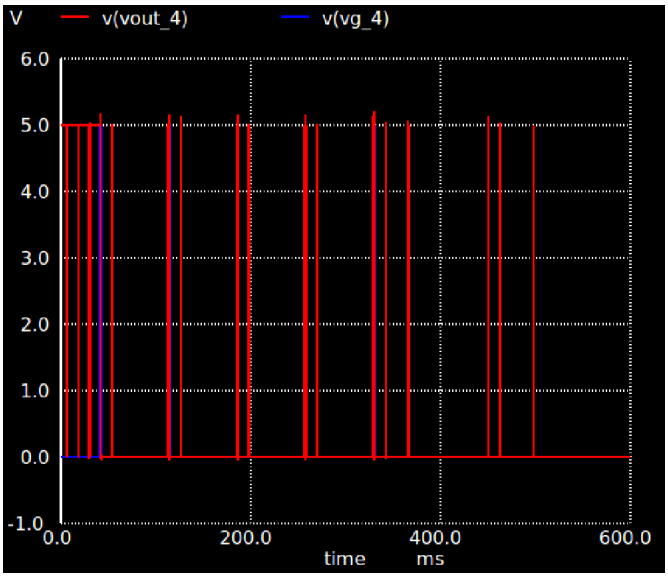

Figure 41 Output of neuron 4

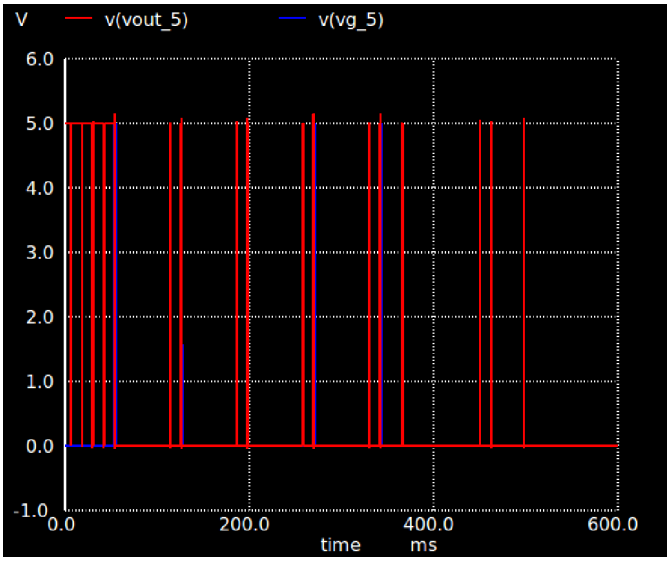

Figure 42 Output of neuron 5

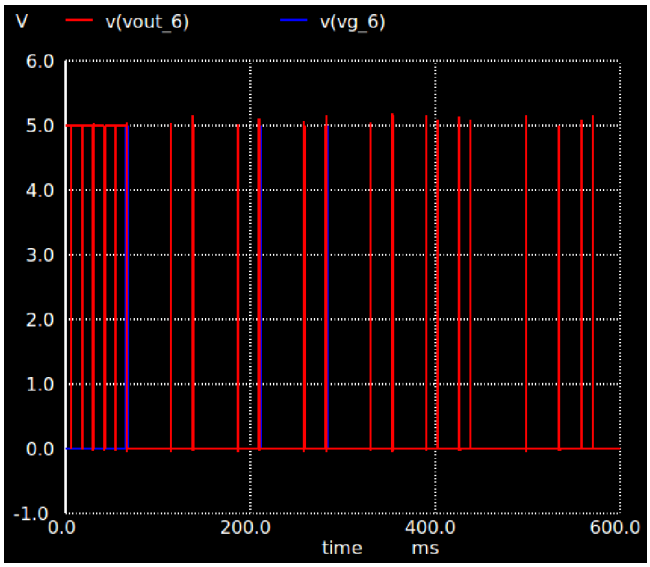

Figure 43 Output of neuron 6

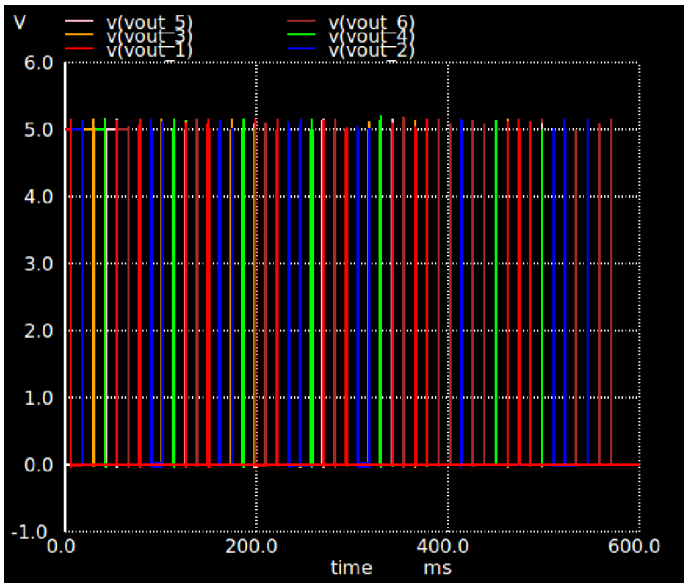

Figure 44 Output of all neurons

5) Circuit Analysis

As required, I have the limitation of transistor size, capacitor size and number, resistor number, and power consumption. The transistor analysis table is as follows:

	Filtering	Peak Detector	S&H	XNOR	AND	Bump and Current Mirror	WTA

Transistor Size and amount	1*1x25	1*1.5x1 1*15x3 1*1.05x1 1*5.5x1	1*1x16 0.5*0.5x12	1*1x8 0.5*0.5x11	1*1x10 0.5*0.5x7	1*1x6 1*0.5x2	1*1x3
Amount of component	4	4	24	24	4	6	1
Total Space	100um^2	212.2um^2	456um^2	258um^2	47um^2	42um^2	3um^2

The total space for transistors is 1118.2 um^2.

Small capacitors around the fF level are being used in the output of the digital gate to eliminate the voltage spikes during transition, which can be ignored. Big capacitors of 1pF are being used in the sample and hold circuit, which in total of 24.

Power consumption is shown as below, which the highest power is around 23mv:

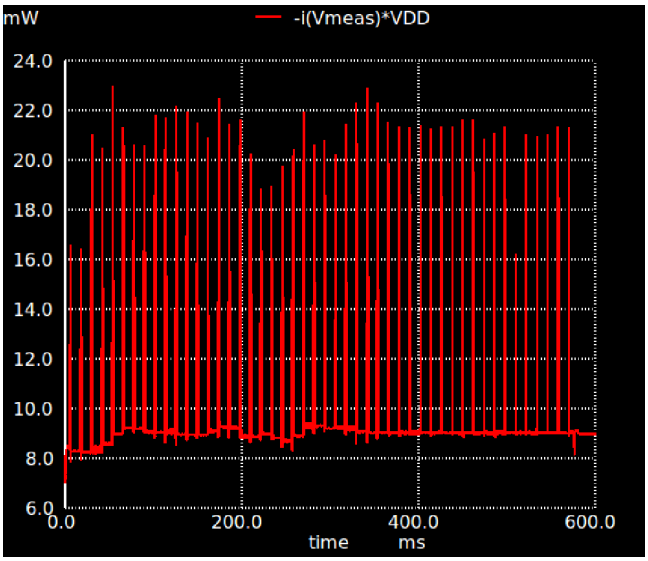

Figure 45 Power

6) Conclusion

In this project, I successfully designed and implemented a custom Analog MOSFET Circuit for detecting and sorting neural spikes from analog voltage signals. The primary objective was to develop a system capable of accurately identifying specific neural events from recordings obtained via an array of electrodes, which is crucial for advancing neural recording technologies and neural prostheses.

Our approach involved several key components, including transamps, bandpass filters, peak detectors, transmission gates, sample-and-hold circuits, and digital logic gates. Each component was meticulously designed and tested to ensure optimal performance. The bandpass filter effectively reduced noise, enhancing the signal quality for subsequent

processing. The peak detector, utilizing a Schmitt Trigger, provided reliable spike detection by filtering out noise and ensuring clean spike output.

The Vmax sample-and-hold circuit played a critical role in storing the peak values of neural spikes, which were then used for comparison in the bump and WTA circuits. The bump circuit transformed the comparison results into current signals, and the WTA circuit identified the neuron with the highest current, indicating the firing neuron.

Despite some challenges, such as managing noise and ensuring accurate spike detection, the system demonstrated robust performance in detecting and sorting neural spikes. The results showed that the designed circuit could successfully identify the firing status of neurons, although some error firing was observed.

Overall, this project achieved its goals of developing a reliable and efficient neural spike detection and sorting system. The insights gained from this work can contribute to the development of more advanced neural recording systems and prosthetic devices, ultimately enhancing our ability to interpret and utilize neural signals for various applications.

7) Reference

[1] I. M. Filanovsky and H. Baltes, "CMOS Schmitt trigger design," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 41, no. 1, pp. 46-49, Jan. 1994, doi: 10.1109/81.260219.