

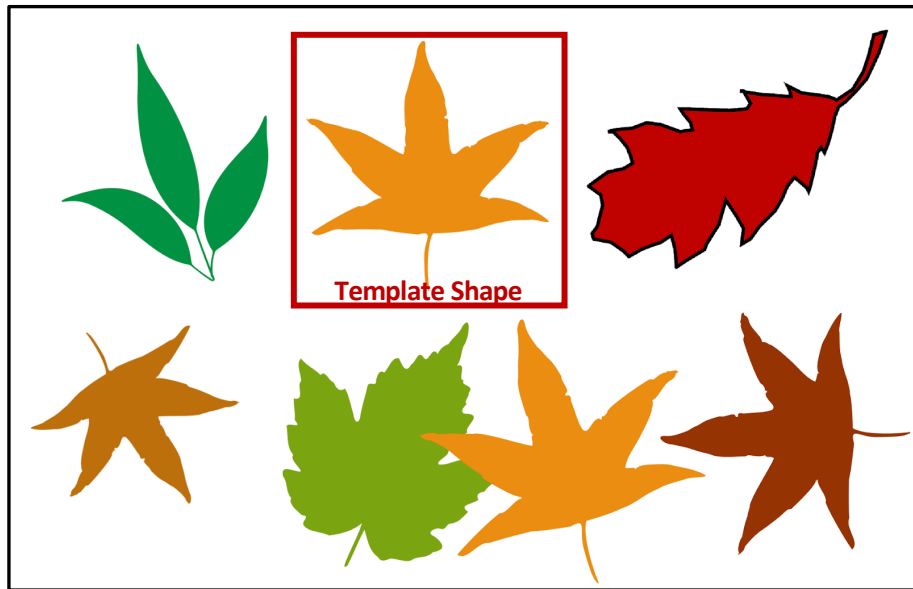
Generalized Hough Transform on GPU

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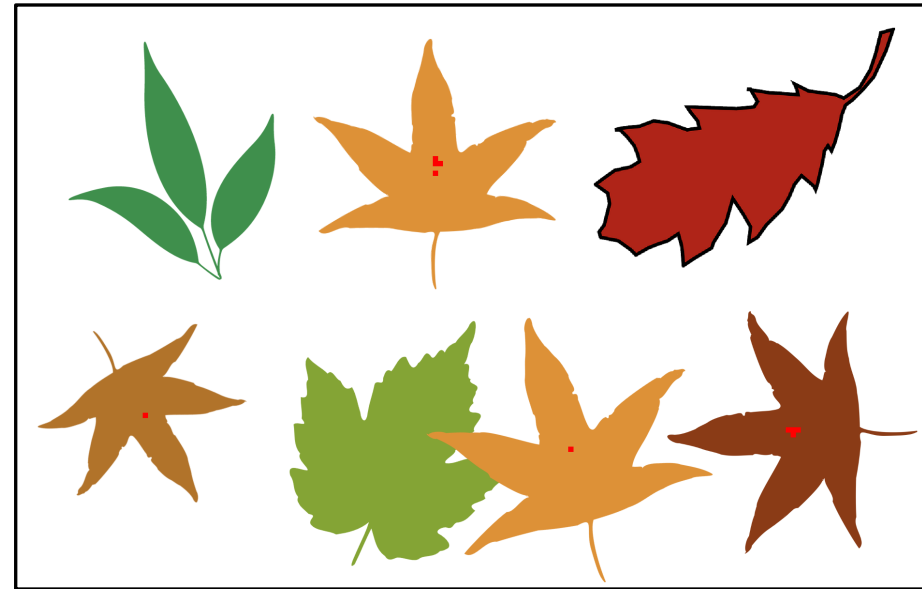
We implemented **Generalized Hough Transform** on **GPU** using **CUDA** and **Thrust**

Feature: Detect **arbitrary** target shape under **rotation** and **scaling**

Acceleration Result: **433x** overall speedup on Intel i7-9700 CPU, RTX 2080 GPU



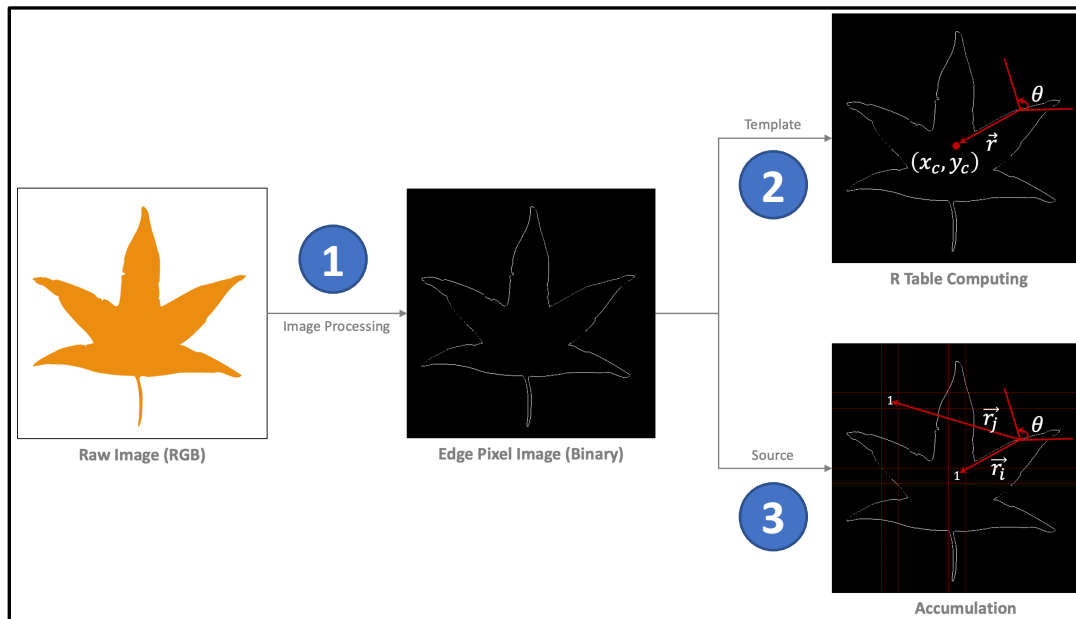
Sample Input



Sample Output

General Hough Transform Pipeline

- 1 Apply derivative filter to **detect edge pixels**
- 2 (Template) Encode all edge points in **R Table**
- 3 (Source) **Accumulate vote of each edge pixel into a 4D accumulator matrix** (x_c, y_c, s, θ)
- 4 Find the shape centers with high votes



Equations for accumulation (2D):

$$x_c = x + r * \cos(\alpha)$$

$$y_c = y + r * \sin(\alpha)$$

Algorithm 1 Calculating Accumulator Loop

```

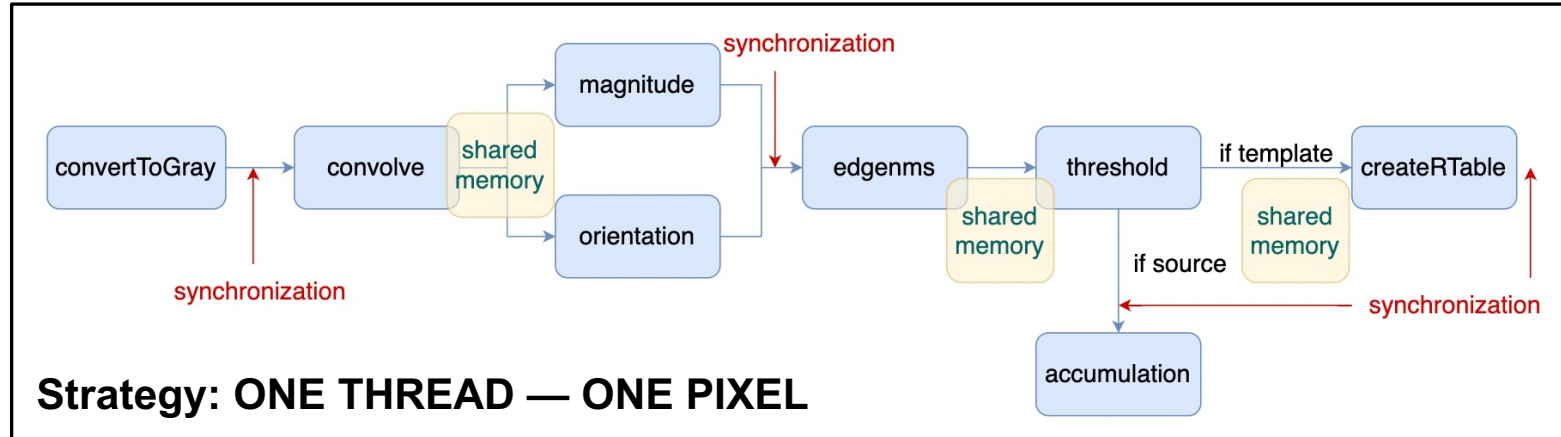
for pixel  $(x, y)$  in image do
  if  $(x, y)$  is an edge pixel then
     $\phi = \text{orientation}(x, y)$ 
    for  $\theta$  in  $[0, 2\pi)$  do
      entries = RTable( $\phi - \theta$ )
      for entry in entries do
         $r = \text{entry}.r, \alpha = \text{entry}.\alpha$ 
        for  $s$  in  $[\text{minScale}, \text{maxScale}]$  do

```

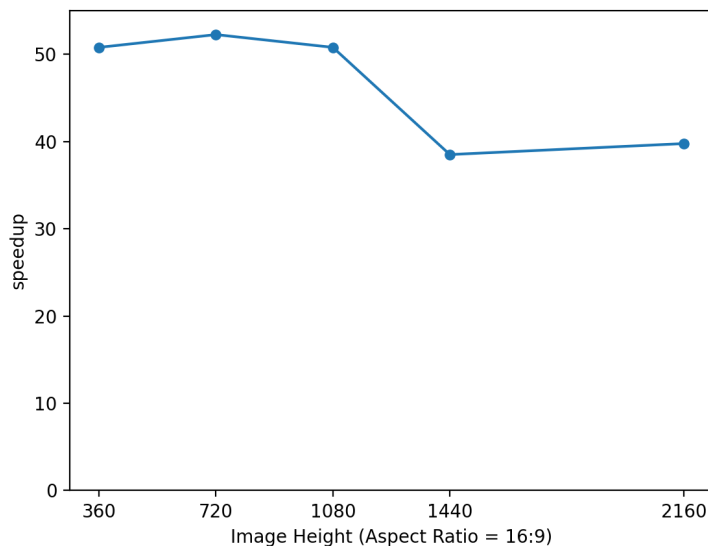
Accumulation is expected to benefit the most from CUDA parallelization.

Parallel Image Processing

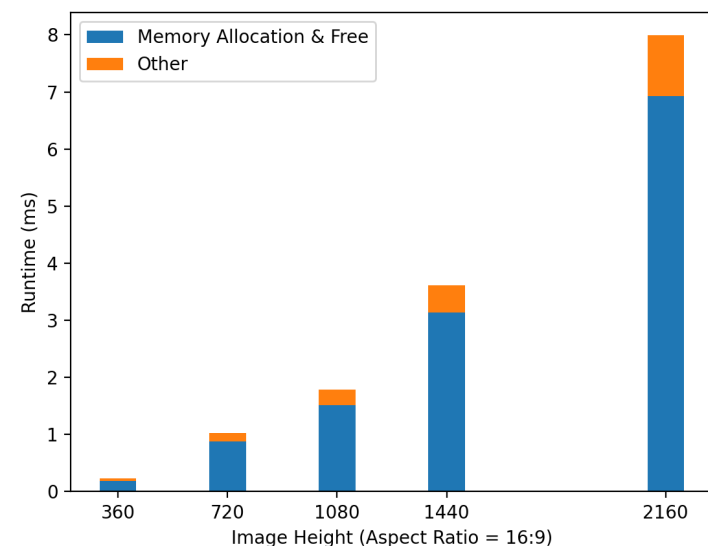
Parallel Image Processing Pipeline



40 - 50x Speedup



Overhead in Memory Allocation & Free



Parallel R Table Processing

R Table in **CPU** memory

i	ϕ_i	R_{ϕ_i}
1	0	$(r_{11}, \alpha_{11}), \dots (r_{1n}, \alpha_{1n})$
2	$\Delta\phi$	$(r_{21}, \alpha_{21}), \dots (r_{2n}, \alpha_{2n})$
3	$2\Delta\phi$	$(r_{31}, \alpha_{31}), \dots (r_{3n}, \alpha_{3n})$
...

- Each slice is with dynamic size
- Troublesome for GPU implementation

R Table in **GPU** memory

R Table (unsorted, GPU)

-1	ϕ_0	-1	ϕ_3	-1
-1	ϕ_1	ϕ_2	ϕ_3	-1
-1	ϕ_1	-1	ϕ_3	ϕ_4
-1	ϕ_1	ϕ_2	ϕ_3	-1
-1	-1	-1	-1	-1

R Table (sorted, GPU)

-1	-1	-1	-1	-1
-1	-1	-1	-1	-1
-1	-1	-1	-1	ϕ_0
ϕ_1	ϕ_1	ϕ_1	ϕ_2	ϕ_2
ϕ_3	ϕ_3	ϕ_3	ϕ_3	ϕ_4

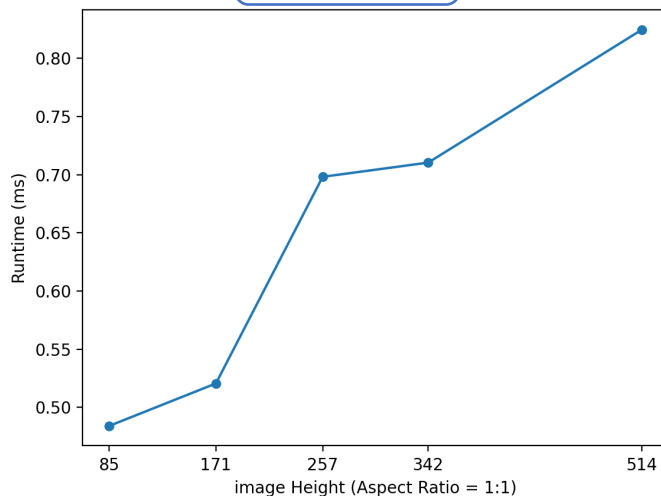
Thrust sort

Thrust lowerBound

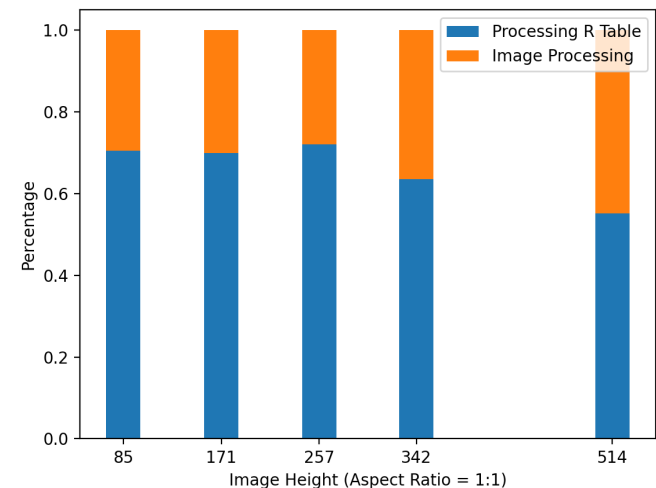
Starting Positions (GPU)

14	15	18	20	24
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Runtime

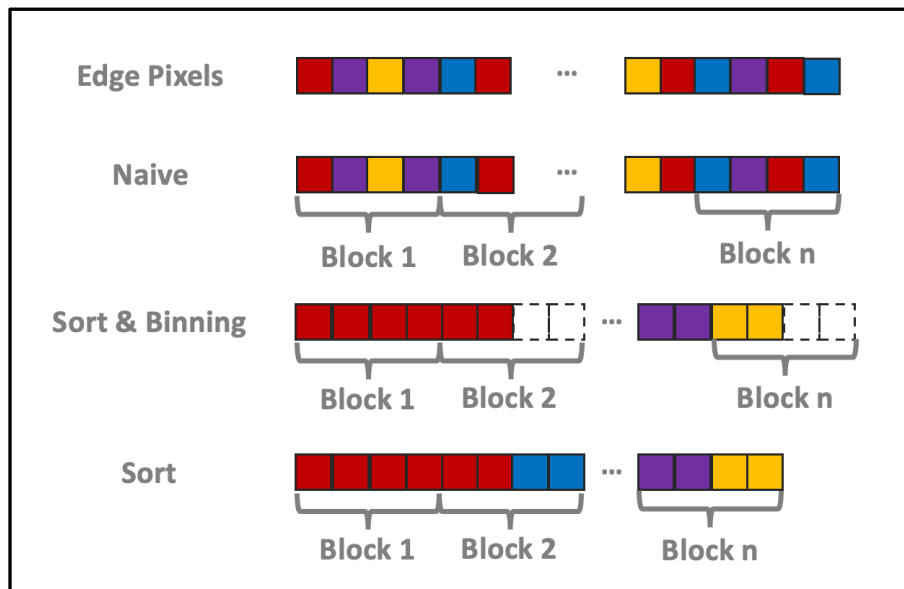


Compared with Image Processing



Parallel Accumulation

Design Alternative 1: Map Edge Pixels to CUDA Blocks



Design Alternative 2: Kernel Dimension

1D Kernel

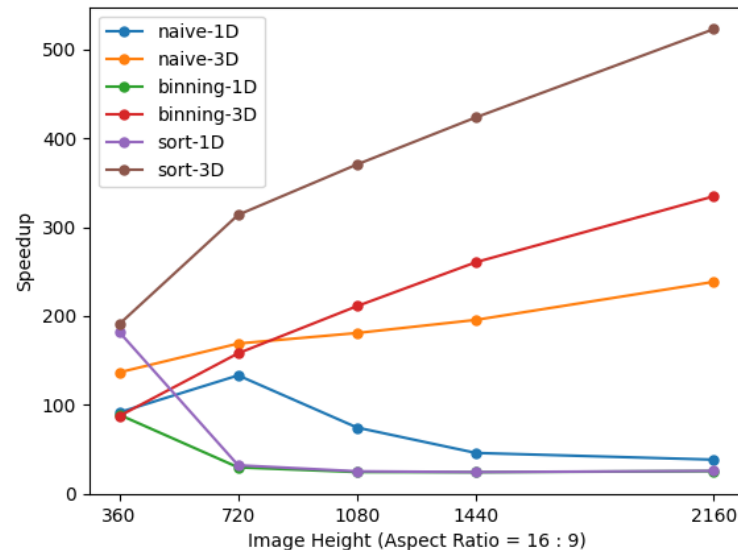
for each θ {
 for each s {
 for each $rEntry\{\dots\}$

3D Kernel

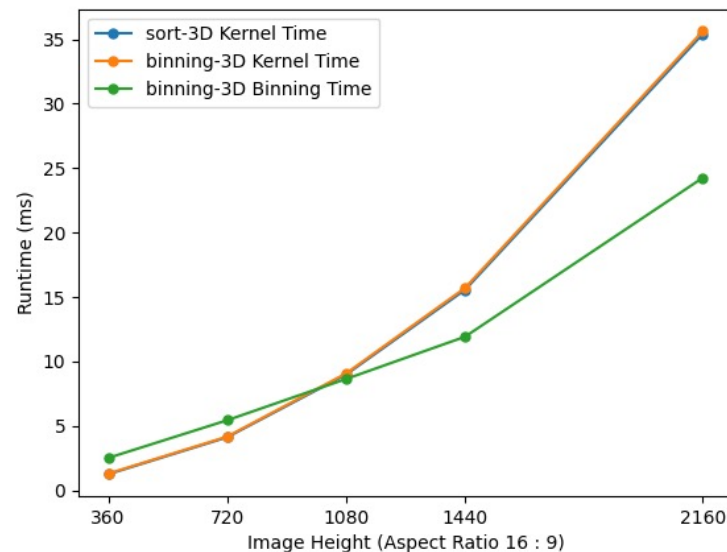
(One block share θ and s)

for each $rEntry\{\dots\}$

Speedup



Binning is expensive



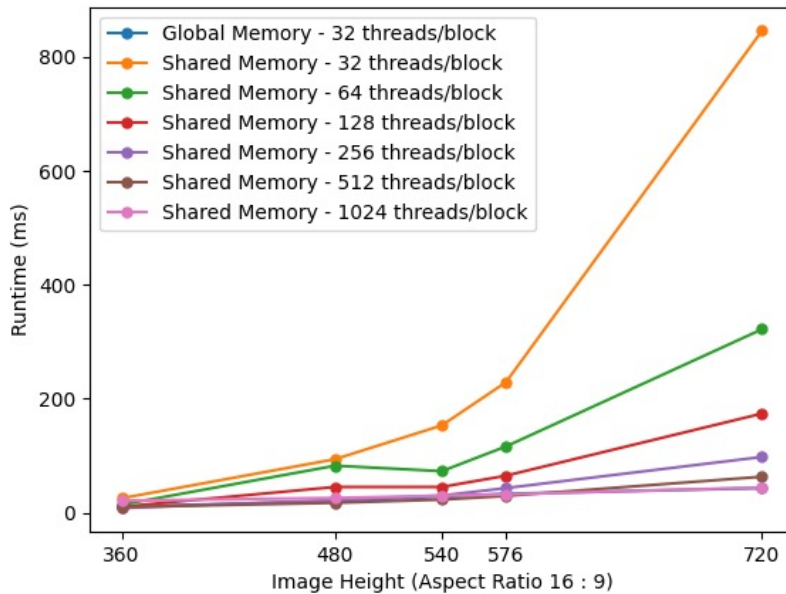
Parallel Accumulation

Design Alternative 3: Shared Memory

Global Memory

- Vote directly to **4D** accumulator (AtomicAdd)

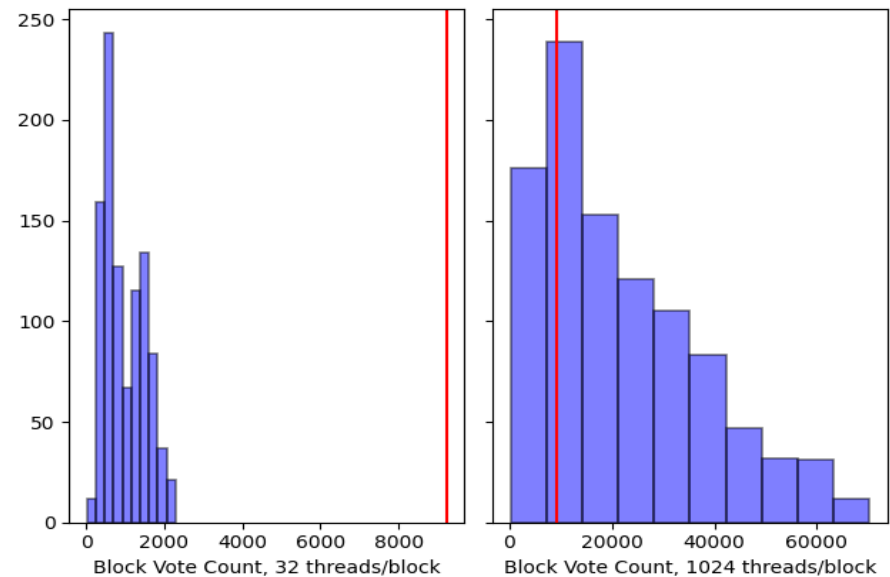
Performance



Shared Memory

- Create a shared **2D** accumulator slice / block, first vote **within** block, then write back

Overhead Analysis

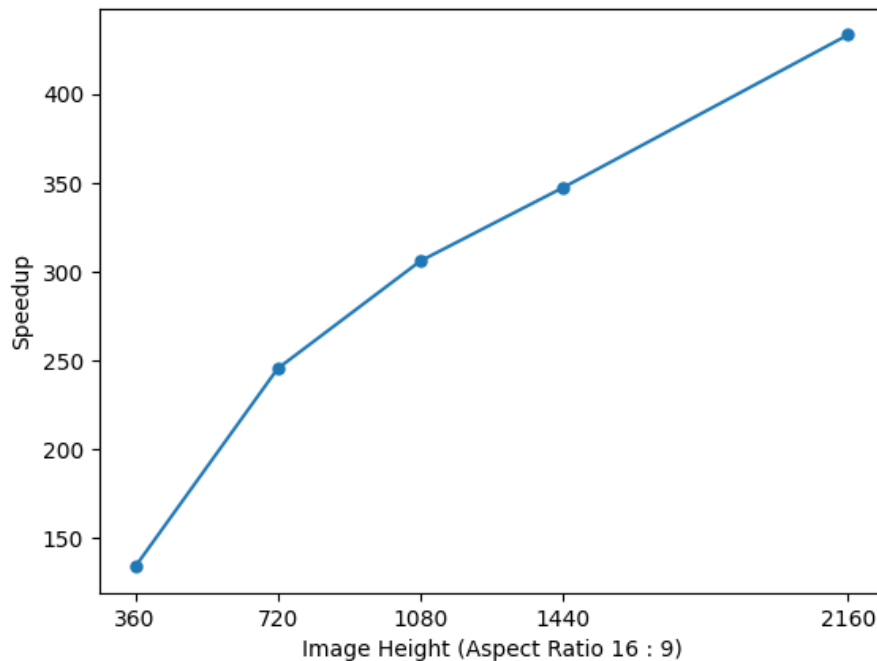


Challenges using shared memory:

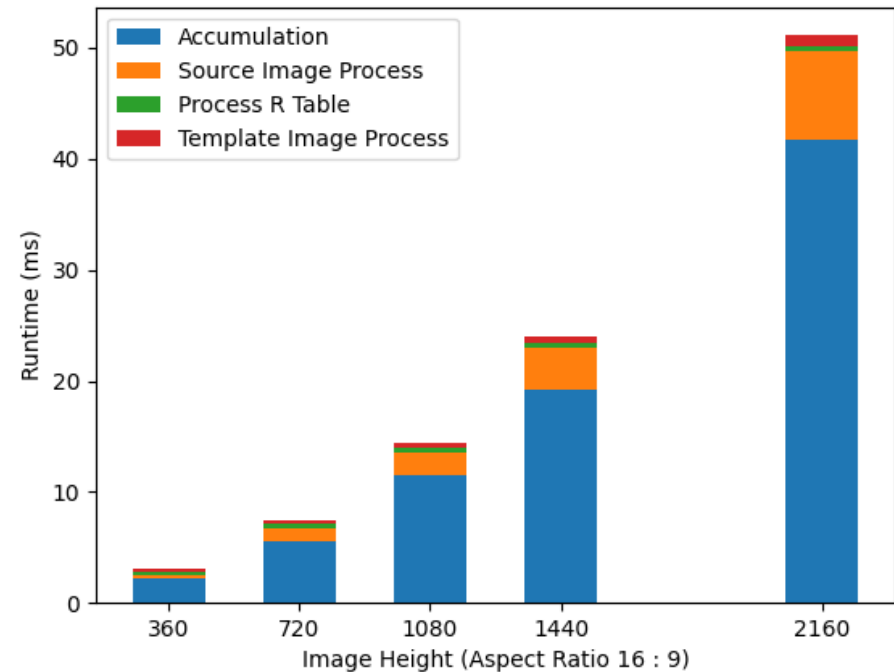
- Bounded by shared memory allocation limit (48KB)
- Need to more efficiently store and update voting data in memory

Overall Speedup

Speedup w.r.t Image Size



Runtime Break Down

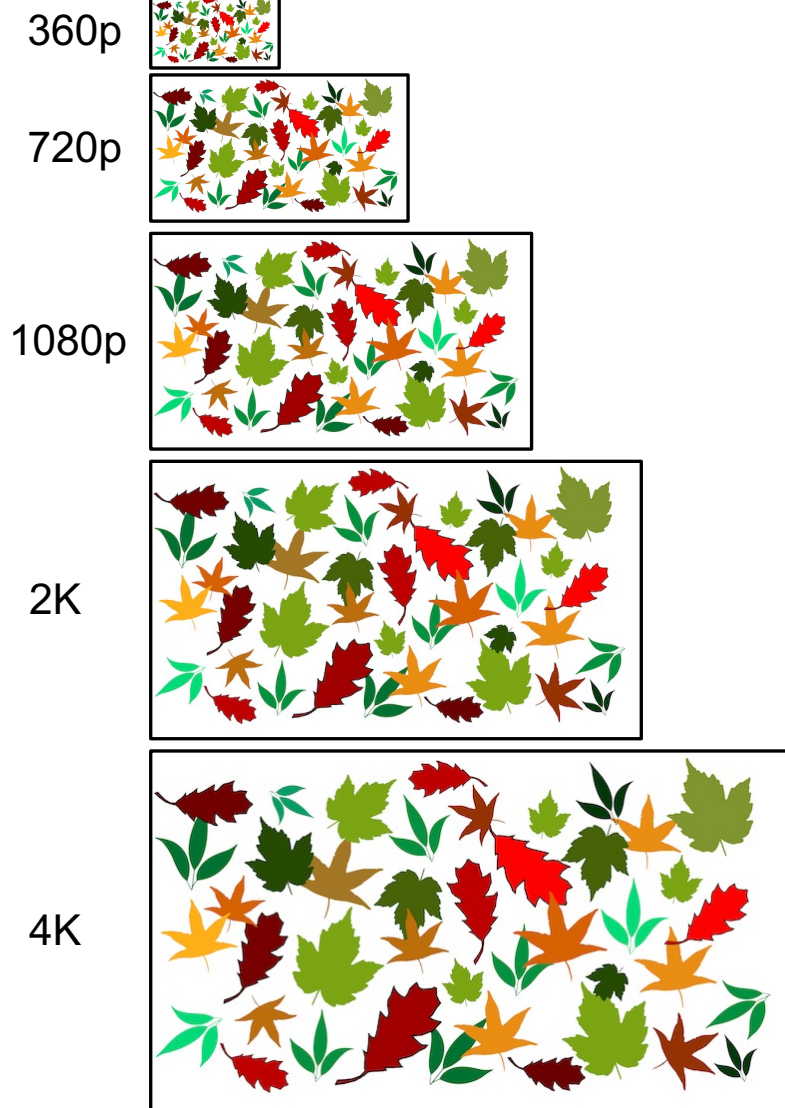


Accumulation is the most critical step to achieve a high speedup.

As the image size grows, the algorithm benefits more from parallelization.

Sample Test Images

Different image sizes



Different shape density

