

Efficient Multi-Path NVLink/PCIe-Aware UCX based Collective Communication for Deep Learning

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28th IEEE Hot Interconnects symposium (HotI 2021)
August 18th 2021

Introduction

Open MPI + UCX

Motivation

Proposed Designs

Multi-Path Copy Design

Collective Communication Design

Results

Micro-Benchmarks

Application Results

Conclusion and Future Work

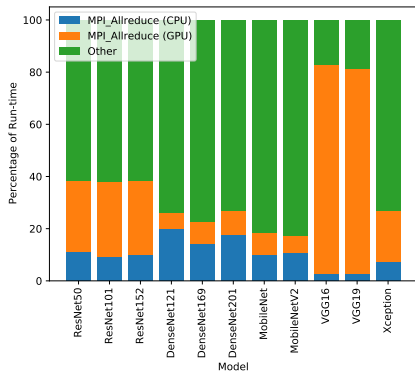
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 - ▶ Popular parallel programming model in HPC
 - ▶ Provides multiple communication APIs
 - ▶ Point-to-point
 - ▶ Partitioned point-to-point
 - ▶ RMA
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- ▶ MPI based Deep Learning on HPC systems
 - ▶ As the complexity of DL models grow we move towards using the aggregate power of HPC systems

MPI-based Deep Learning

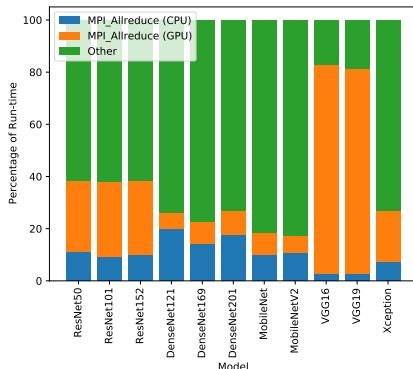
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Impact of MPI_Allreduce on a single AC922 node

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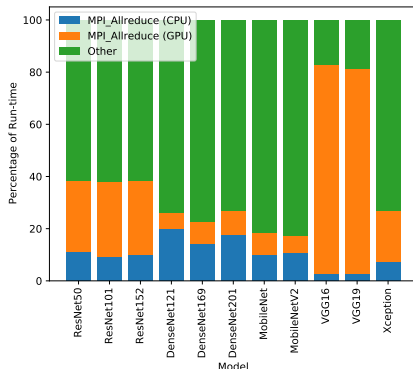
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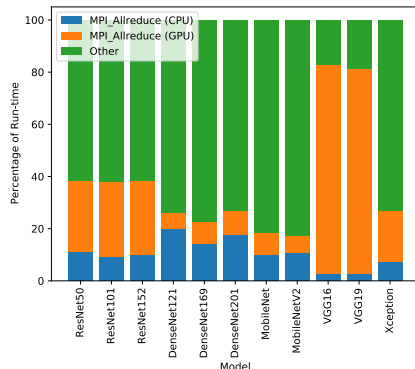
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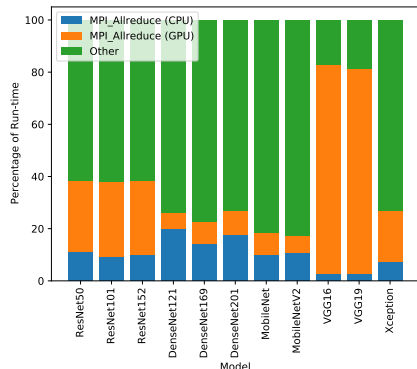
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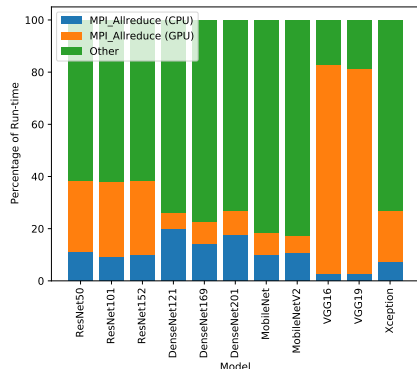
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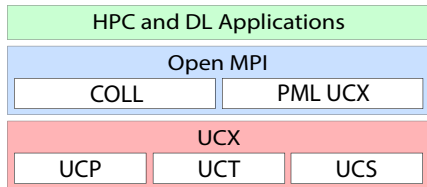
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- ▶ MPI communication is a major bottleneck in these applications



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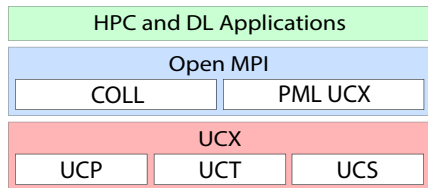
Open MPI + UCX

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 - ▶ Point-to-point implemented upon RMA Put/Get operations

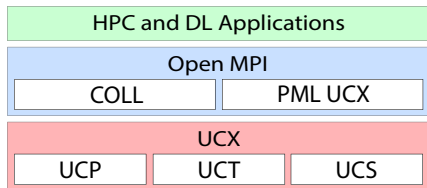


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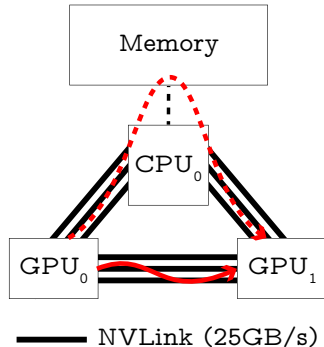


Research Goal

- ▶ Improve the performance of Deep Learning applications
- ▶ Enhance point-to-point and collective communication for MPI's large GPU messages

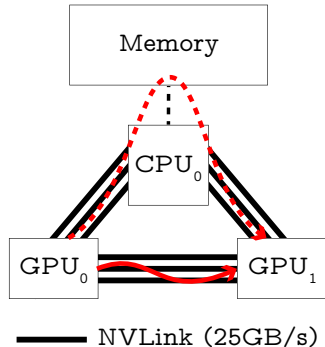
Multi-Path Copy Motivation

- ▶ Currently data transfers between GPUs, send the data directly between devices using a zero copy put operation in UCX.
 - ▶ (As shown by the solid red line)



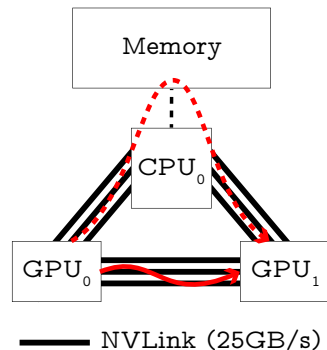
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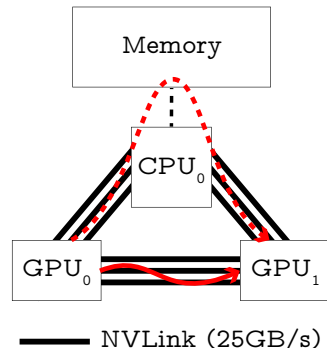
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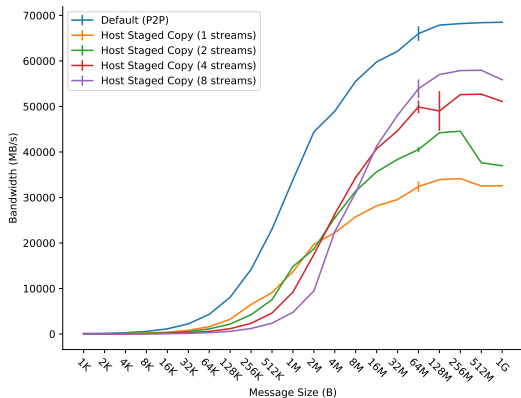


Research Question

Can we design a mechanism to use all communication paths?

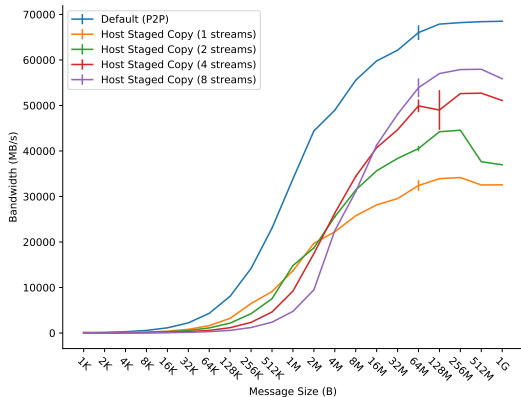
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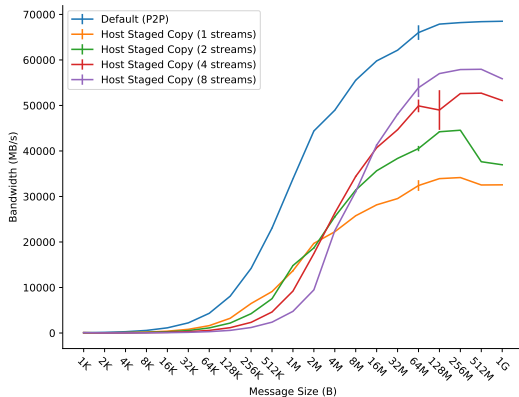
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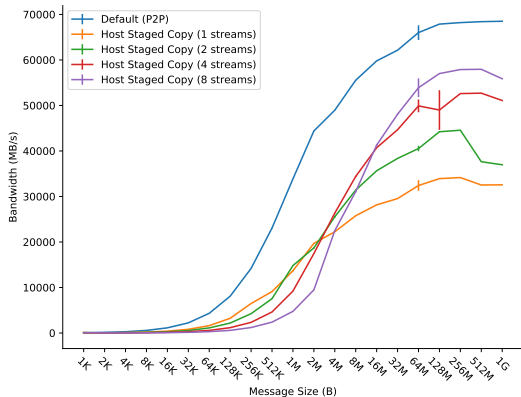
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- Up to 53GB/s of unused bandwidth

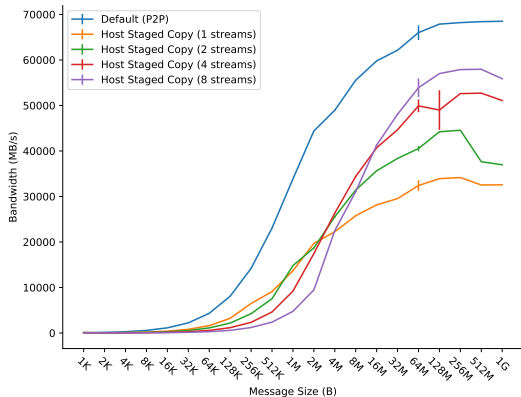


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► Good potential for our Multi-Path design



Algorithm: Multi-Path Copy Algorithm

Input: sbuf, host_buf, data_size, host_share, n_host_streams

Output: dbuf

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1 host_dsize = data_size * host_share;
2 host_chunk_dsize = host_dsize / n_host_streams;
3 d2d_dsize = data_size - host_dsize;
4 do in parallel
5     Copy d2d_dsize bytes from sbuf to dbuf;
6     for  $i \leftarrow 0$  to  $n\_host\_streams$  by 1 do in parallel
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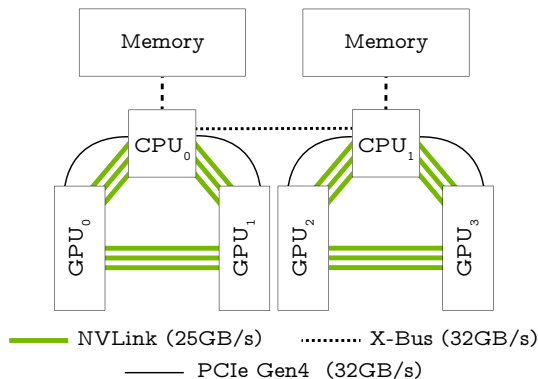
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 - ▶ Copy portion directly to destination GPU
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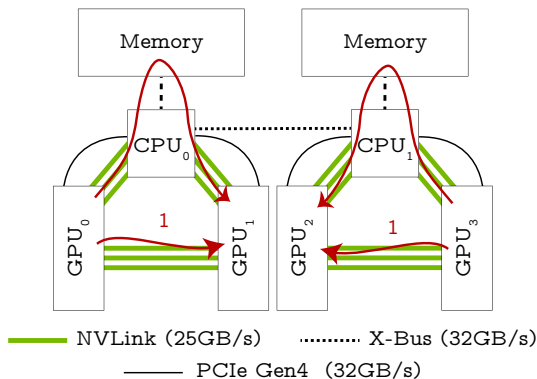
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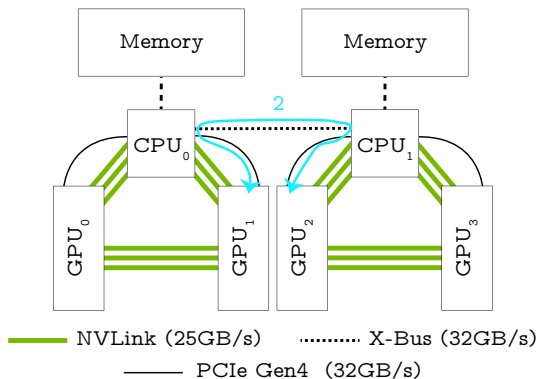
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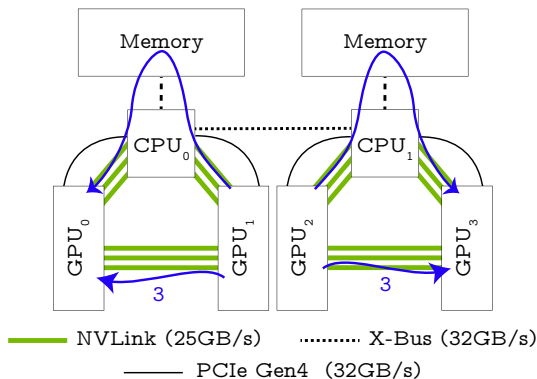
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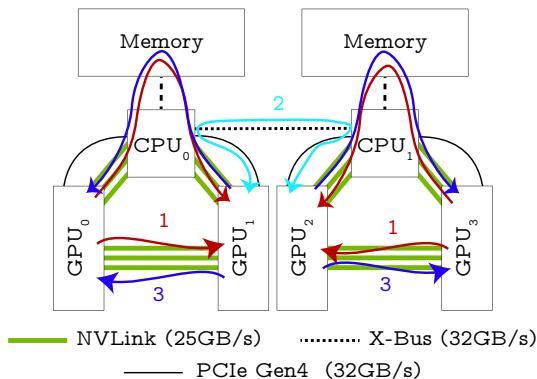
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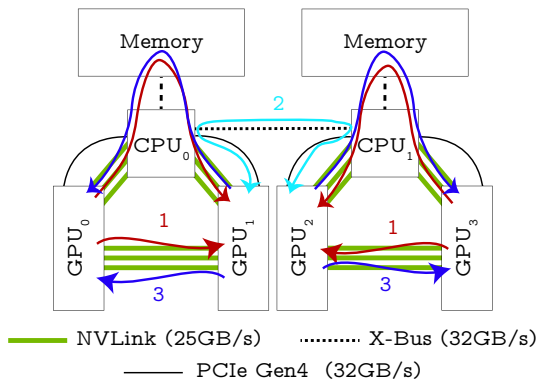
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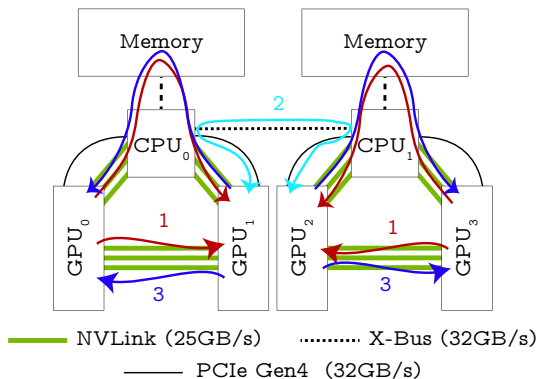
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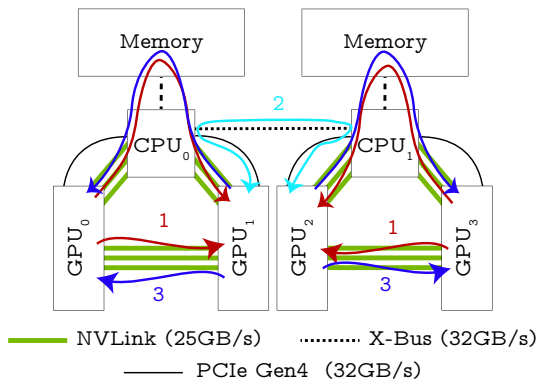
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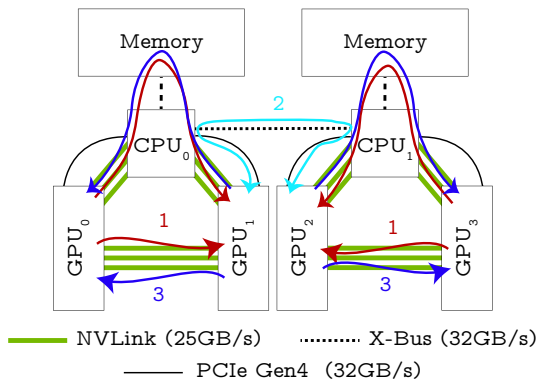
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 - ▶ Inter-socket communication dynamically switches between PCIe and NVLink
 - ▶ Dynamically send data using Multi-path or Peer-to-Peer copies via the host links
 - ▶ Minimise intra-socket congestion



Experimental Setup



► Hardware:

- IBM AC922
- 32 Core, 128 Thread Power9 CPU
- 256GB RAM
- Four V100-SMX2-32GB



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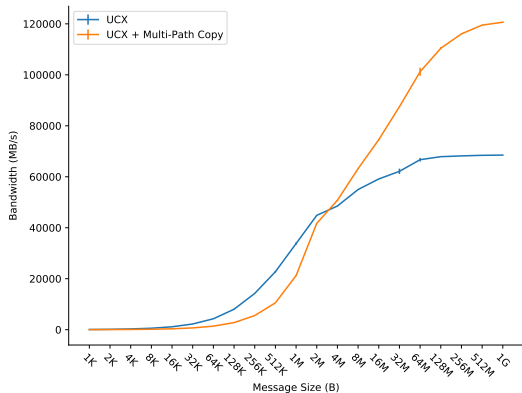
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► Software:

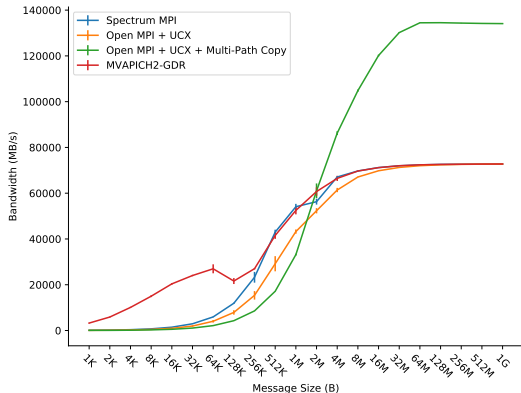
- Open MPI 4.0.4rc2
- UCX 1.8.0
- Open MPI + HPC-X v2.7
- Spectrum-MPI 10.3.1
- MVAPICH2-GDR 2.3.5
- NCCL 2.5.6
- Horovod 0.20.3
- TensorFlow 1.15.2



UCX Put and MPI Point-to-Point Results

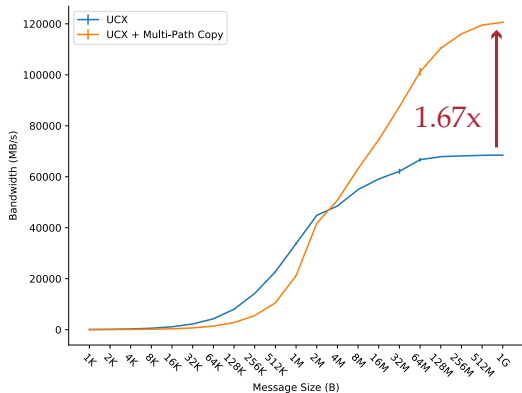


UCX Put Bandwidth

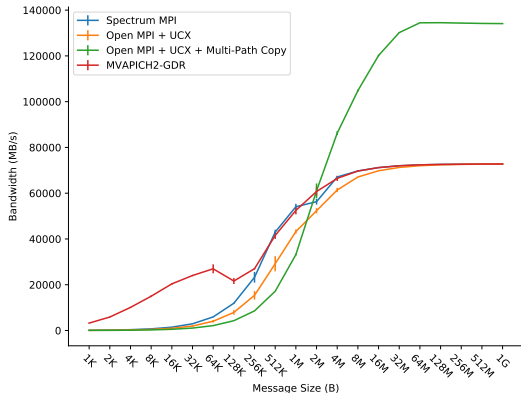


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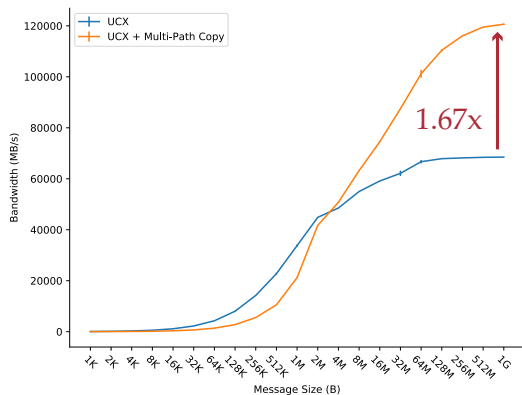


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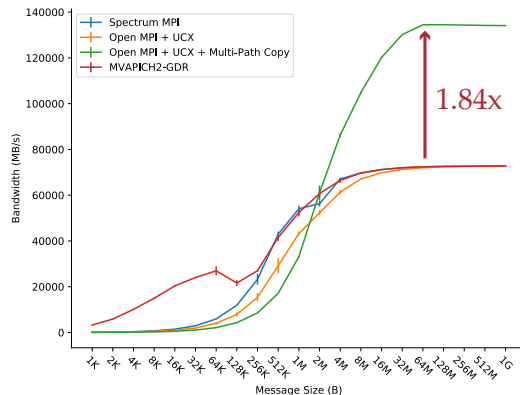


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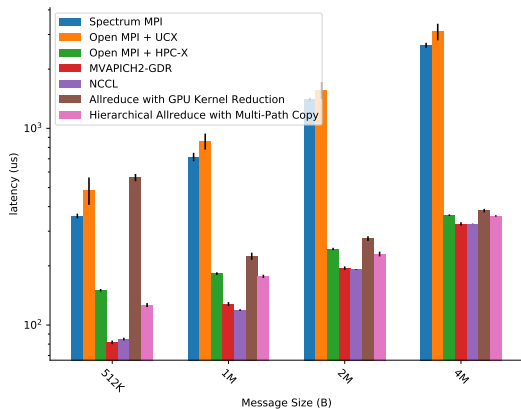


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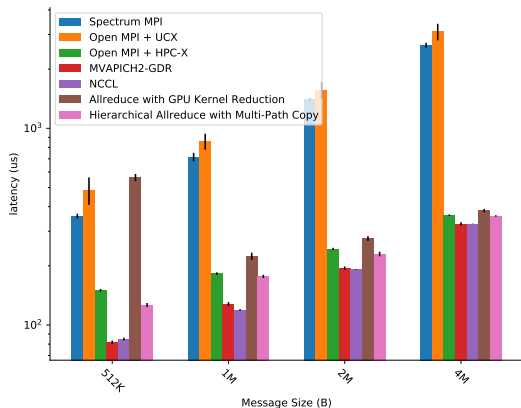
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MPI_Allreduce Results (Medium Message Sizes)



MPI_Allreduce latency on 4 GPUs for
medium to large message sizes

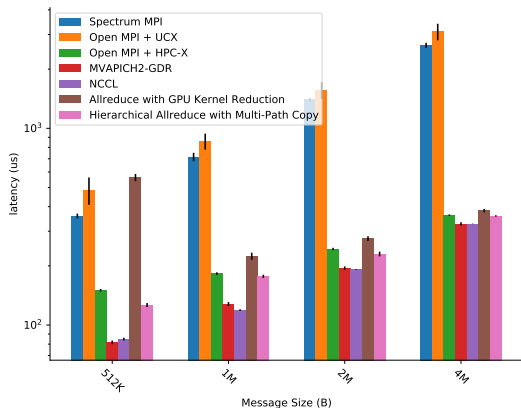
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► 2.75x speedup over Open MPI + UCX at 1MB

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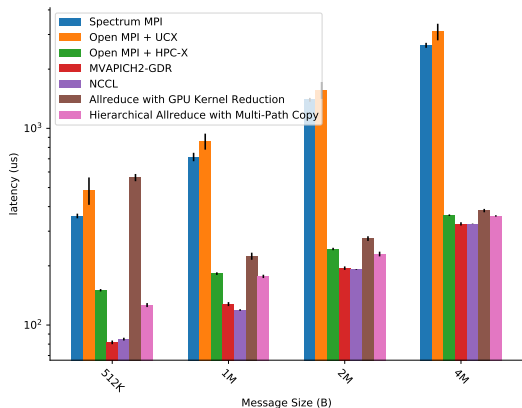
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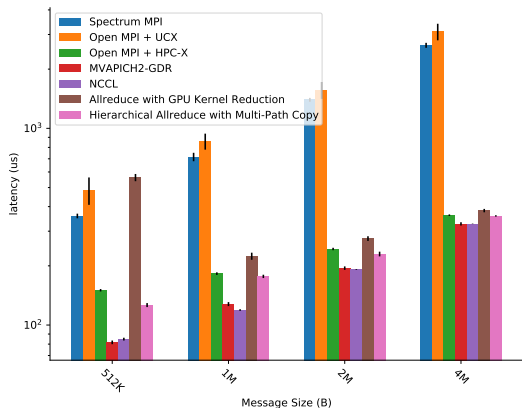
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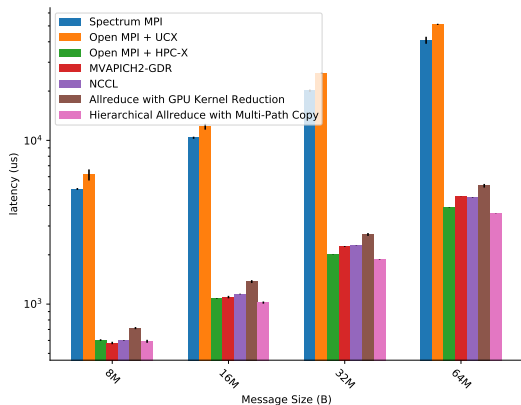
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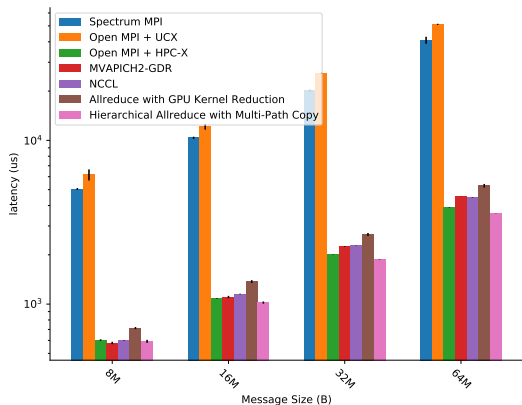
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- ▶ Comparable performance to Open MPI + HPC-X

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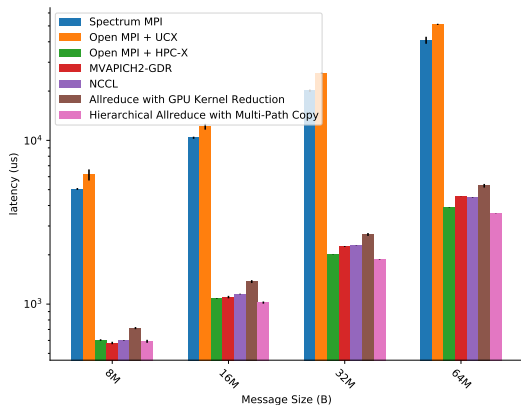
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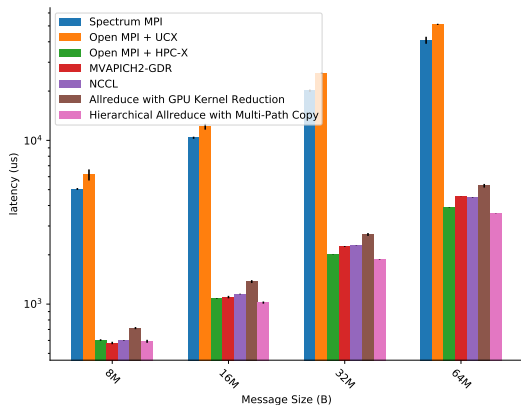
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- ▶ Comparable performance to optimised libraries at 8MB
- ▶ Outperformed all libraries after 16MB

MPI_Allreduce latency on 4 GPUs for large message sizes

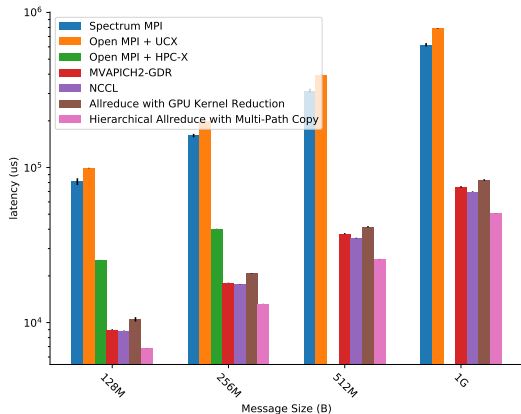
MPI_Allreduce Results (Large Message Sizes)



MPI_Allreduce latency on 4 GPUs for large message sizes

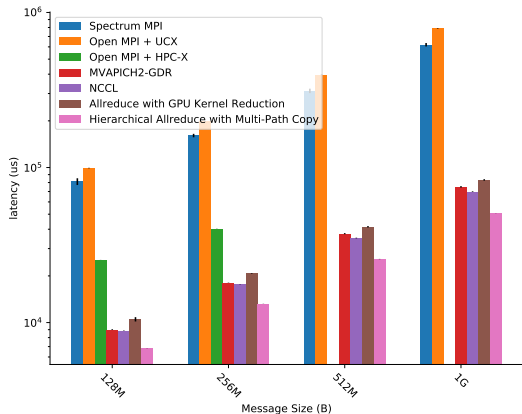
- ▶ Comparable performance to optimised libraries at 8MB
- ▶ Outperformed all libraries after 16MB
 - ▶ Open MPI + HPC-X by 1.09x
 - ▶ MVAPICH2-GDR by 1.26x
 - ▶ NCCL by 1.25x

MPI_Allreduce Results (Very Large Message Sizes)



MPI_Allreduce latency on 4 GPUs for very large message sizes

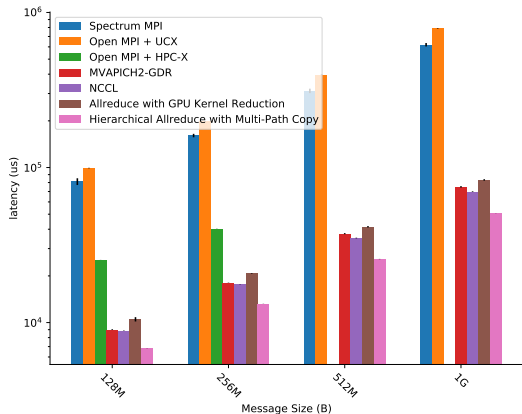
MPI_Allreduce Results (Very Large Message Sizes)



► Much lower latency than Open MPI + HPC-X

MPI_Allreduce latency on 4 GPUs for very large message sizes

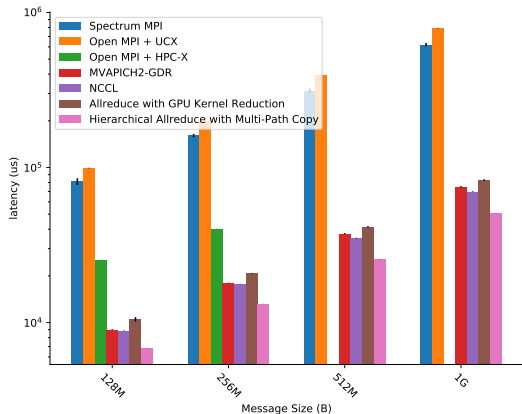
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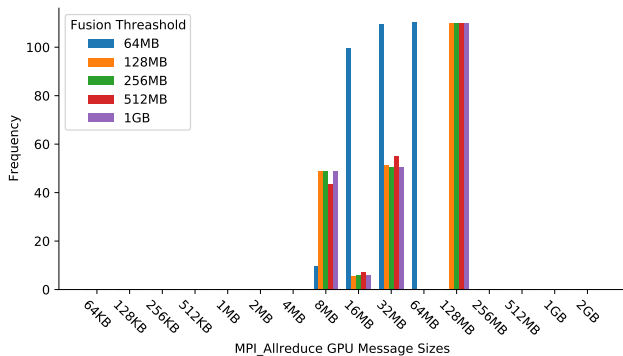
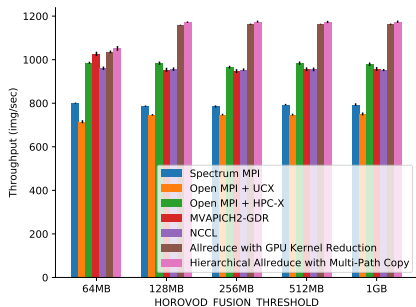


- ▶ Much lower latency than Open MPI + HPC-X
- ▶ At 1GB we see speedup of:
 - ▶ 1.47x over MVAPICH2-GDR
 - ▶ 1.38x over NCCL

MPI_Allreduce latency on 4 GPUs for very large message sizes

Application Results (ResNet50)

► ResNet50 up to 1.56x speedup

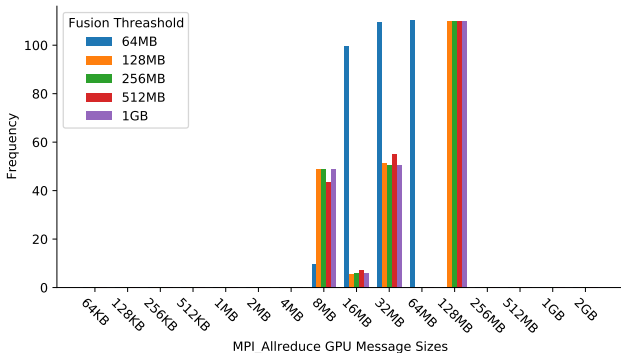
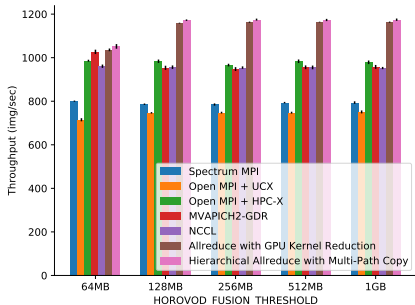


Synthetic Horovod + TensorFlow
benchmarks for ResNet50

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (ResNet50)

- ▶ ResNet50 up to 1.56x speedup
- ▶ Modifying fusion threshold increases message sizes to 128MB

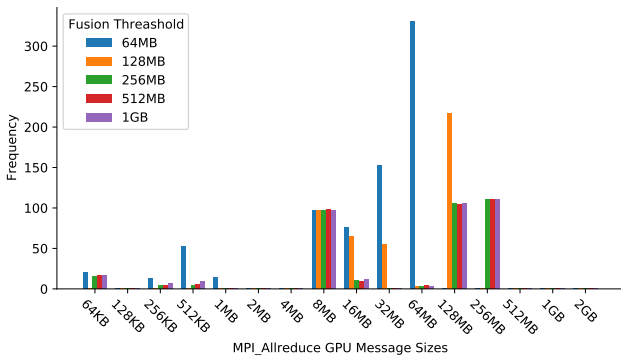
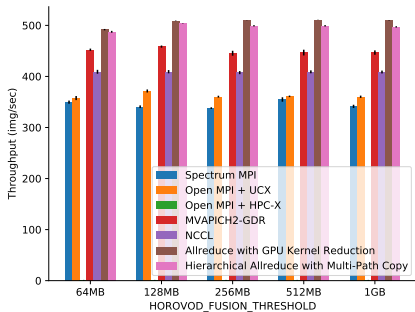


Synthetic Horovod + TensorFlow
benchmarks for ResNet50

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (ResNet152)

► ResNet152 up to 1.40x speedup

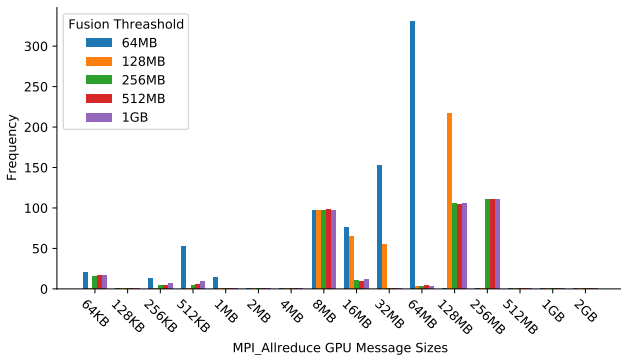
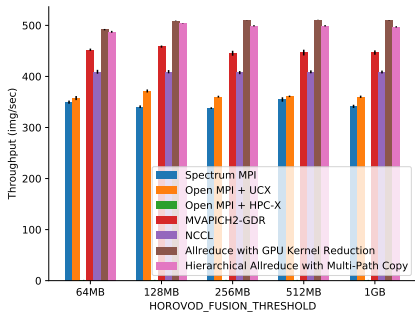


Synthetic Horovod + TensorFlow
benchmarks for ResNet152

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (ResNet152)

- ▶ ResNet152 up to 1.40x speedup
- ▶ Modifying fusion threshold increases message sizes to 256MB
 - ▶ Also results in smaller messages

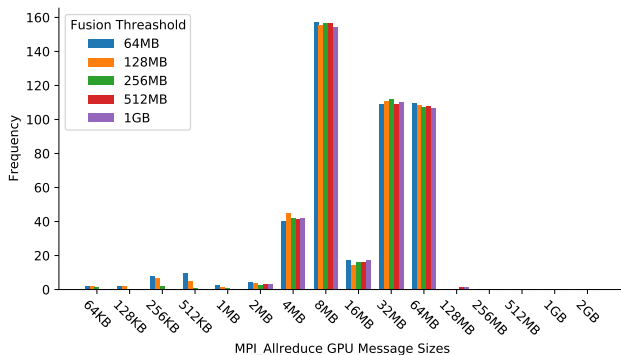
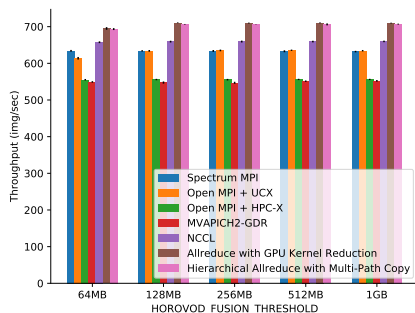


Synthetic Horovod + TensorFlow
benchmarks for ResNet152

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (DenseNet201)

► DenseNet201 up to 1.26x speedup

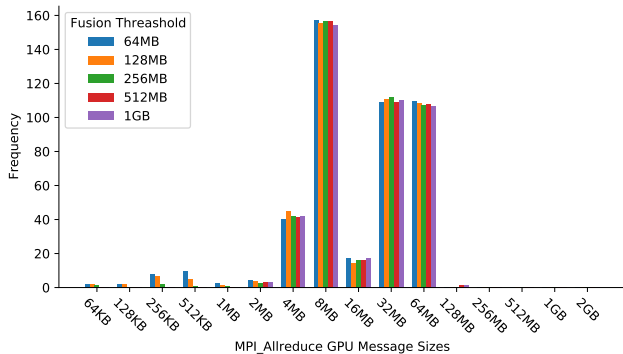
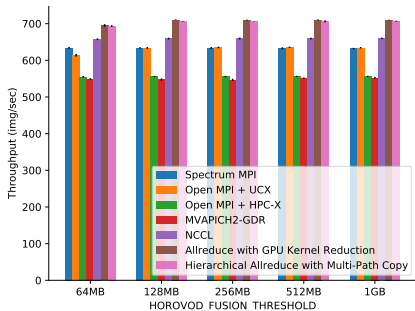


Synthetic Horovod + TensorFlow
benchmarks for DenseNet201

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (DenseNet201)

- DenseNet201 up to 1.26x speedup
- Modifying fusion threshold has minimal impact on message sizes

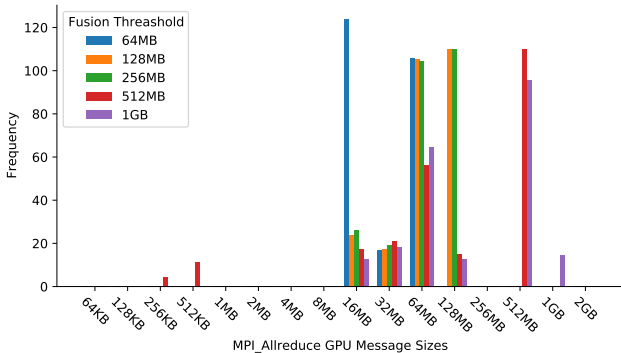
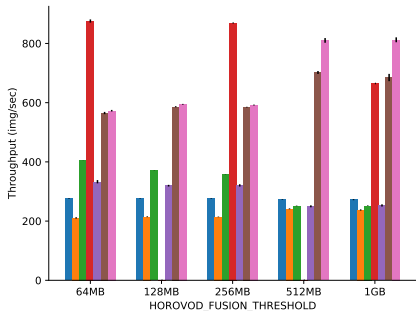


Synthetic Horovod + TensorFlow
benchmarks for DenseNet201

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (VGG16)

► VGG16 up to 3.42x speedup

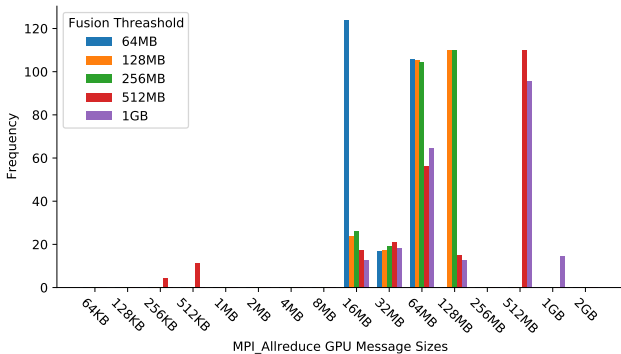
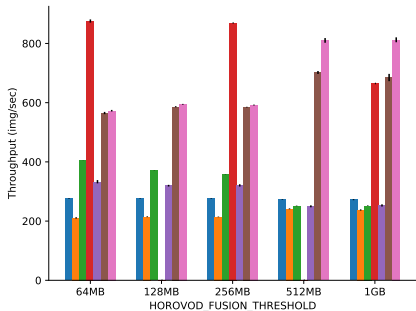


Synthetic Horovod + TensorFlow
benchmarks for VGG16

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Application Results (VGG16)

- ▶ VGG16 up to 3.42x speedup
- ▶ Modifying fusion threshold increases message sizes to 1GB



Synthetic Horovod + TensorFlow
benchmarks for VGG16

GPU Message Sizes for different
HOROVOD_FUSION_THRESHOLD

Conclusion



- ▶ Deep Learning workloads use MPI_Allreduce collective extensively
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- ▶ For Deep Learning Applications we see up to 3.42x speedup with these proposed ideas

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- ▶ We plan to devise cluster-wide collective algorithms
- ▶ We would like to study dynamic tuning approaches

Thank You!

Acknowledgements



compute | **calcul**
canada | canada

