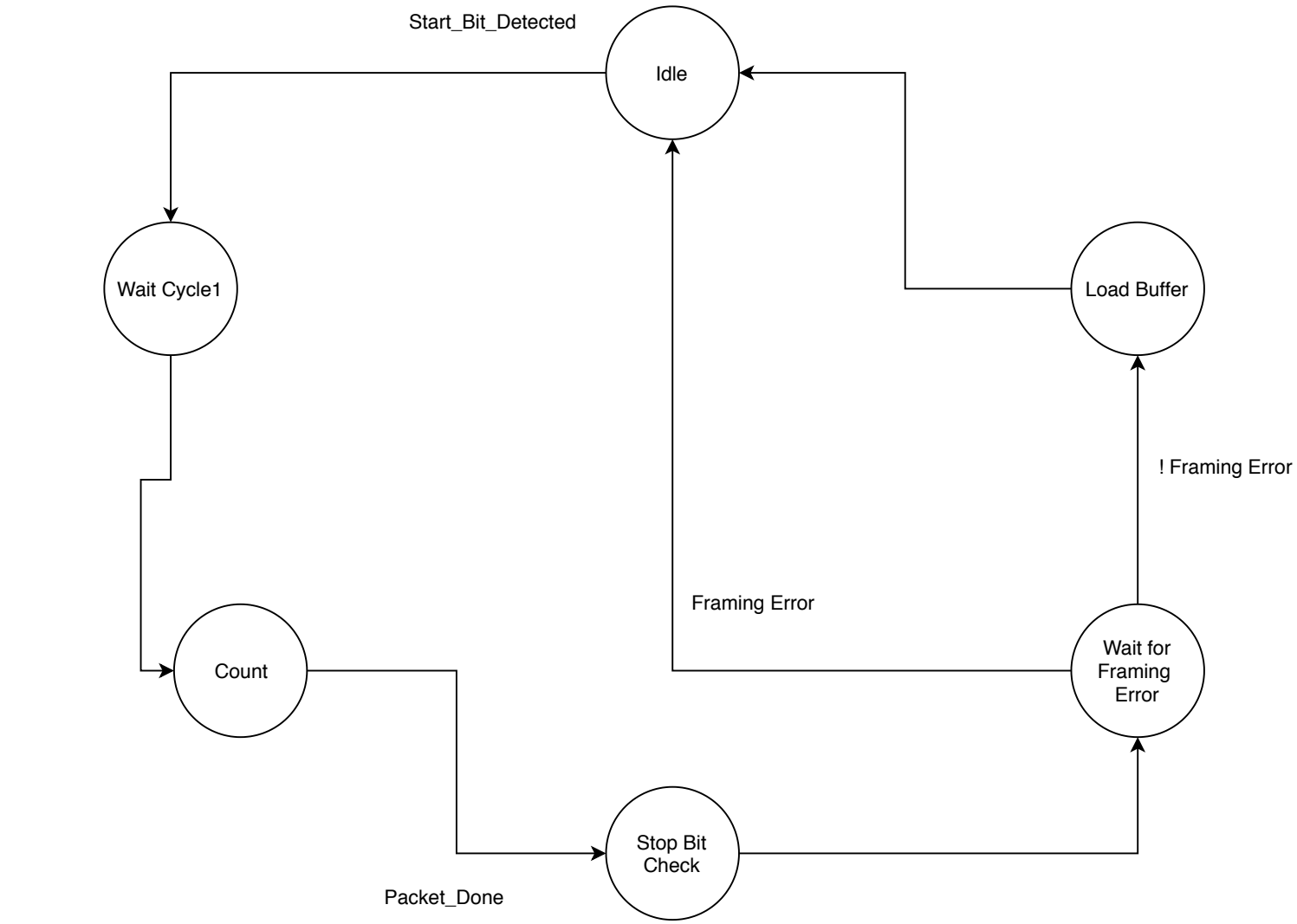


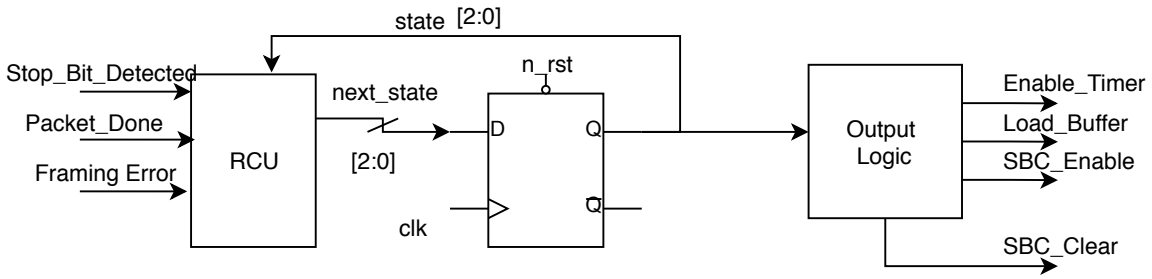


```
Case(state)
      Enable_Timer = Load_Buffer = 0
      SBC_Clear = SBC_Enable = 0
   Wait_Cycle1:
      Enable_Timer = Load_Buffer = 0
      SBC_Clear = 1;  SBC_Enable = 0
   Count:
      Enable_Timer = SBC_Clear = 1
      SBC_Enable = Load_Buffer = 0
   Stop_Bit_Check:
      SBC_Enable = 1
      SBC_Clear = Enable_Timer = Load_Buffer = 0
   Wait_Error:
      SBC_Enable = 1
      SBC_Clear = En
   Load_Buffer:
      Load_Buffer = 1
      SBC_Enable = SBC_Clear = Enable_Timer = 0
```