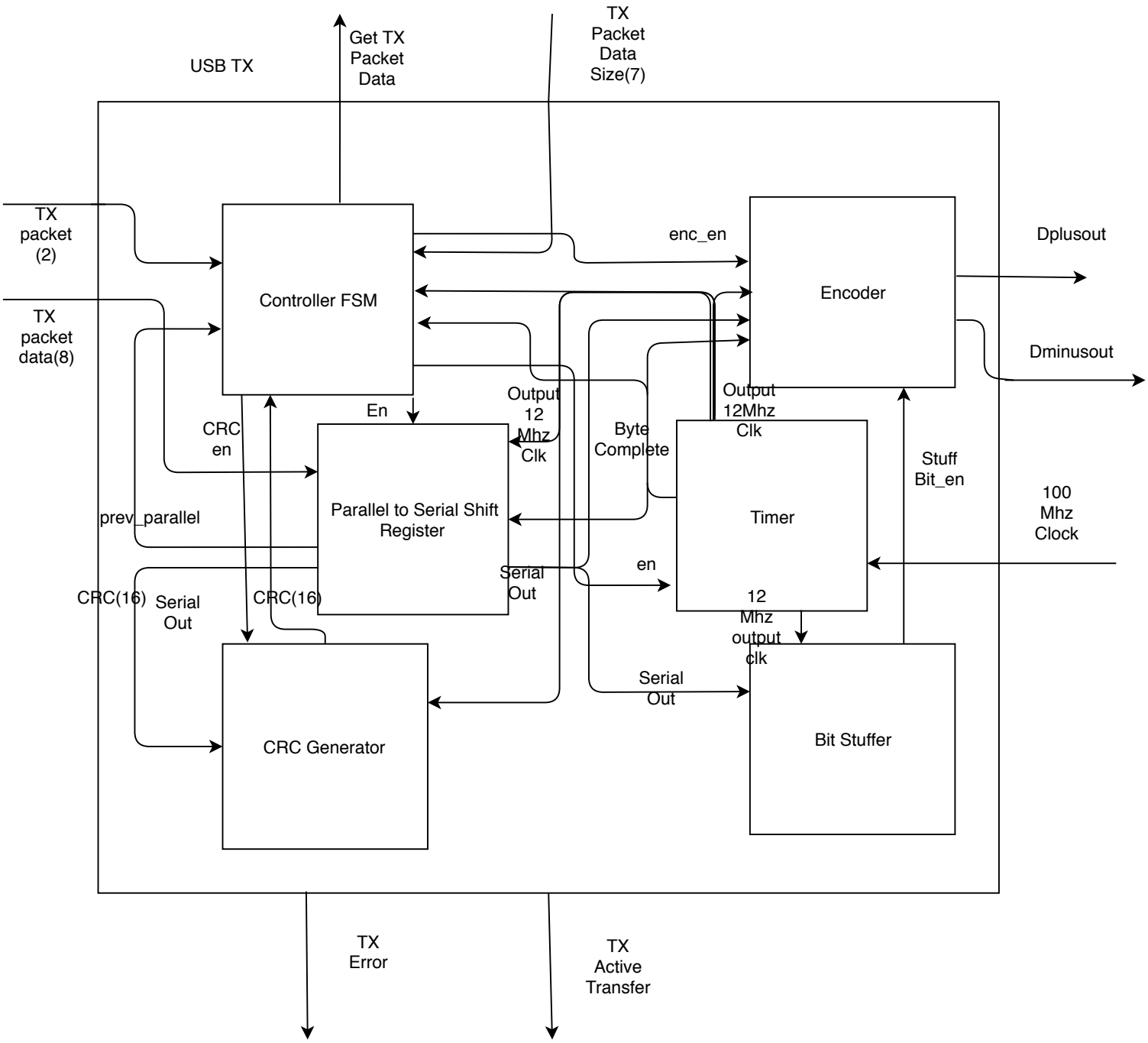
TX RTL Diagrams

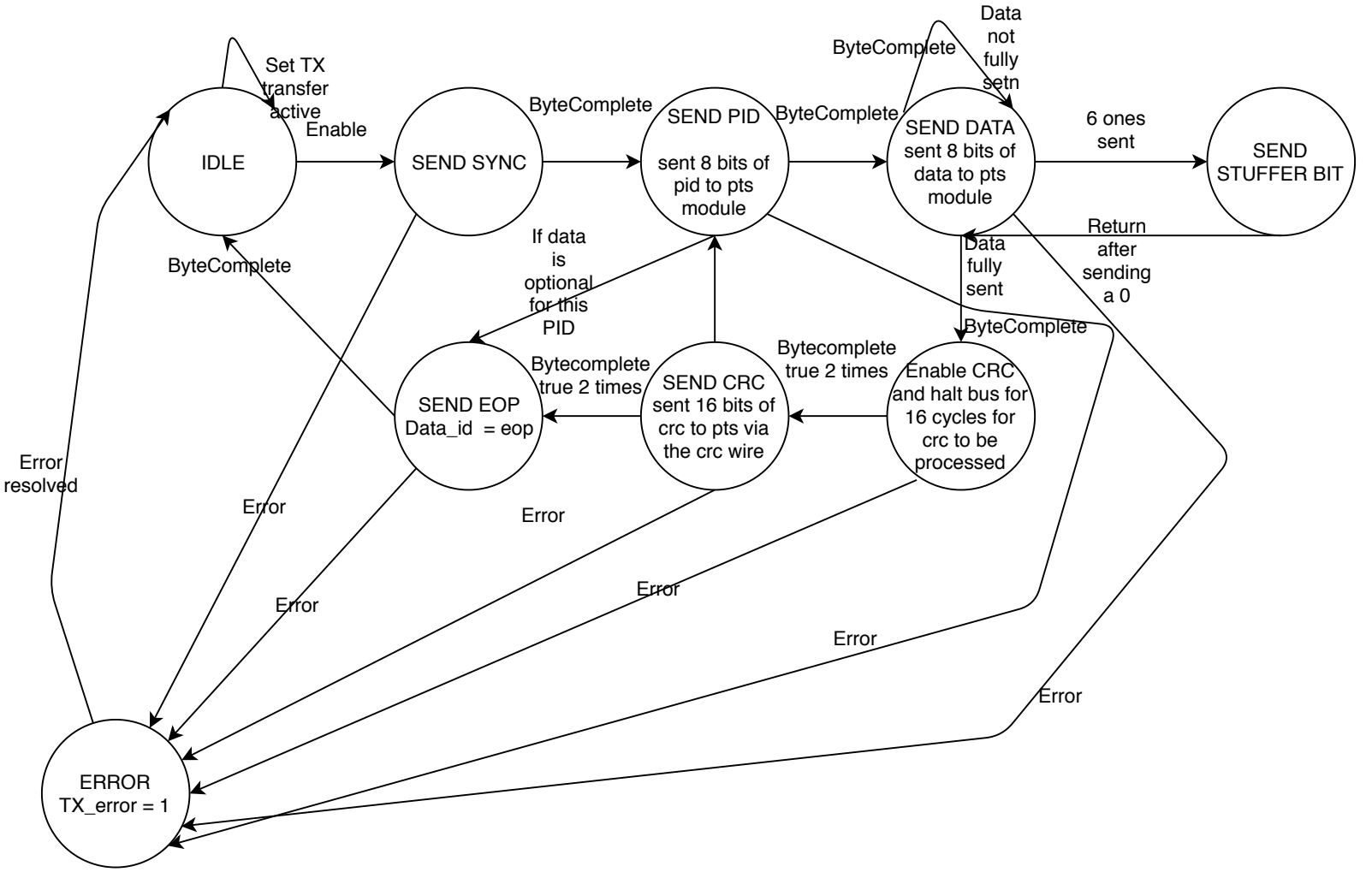
By Karan Oberoi



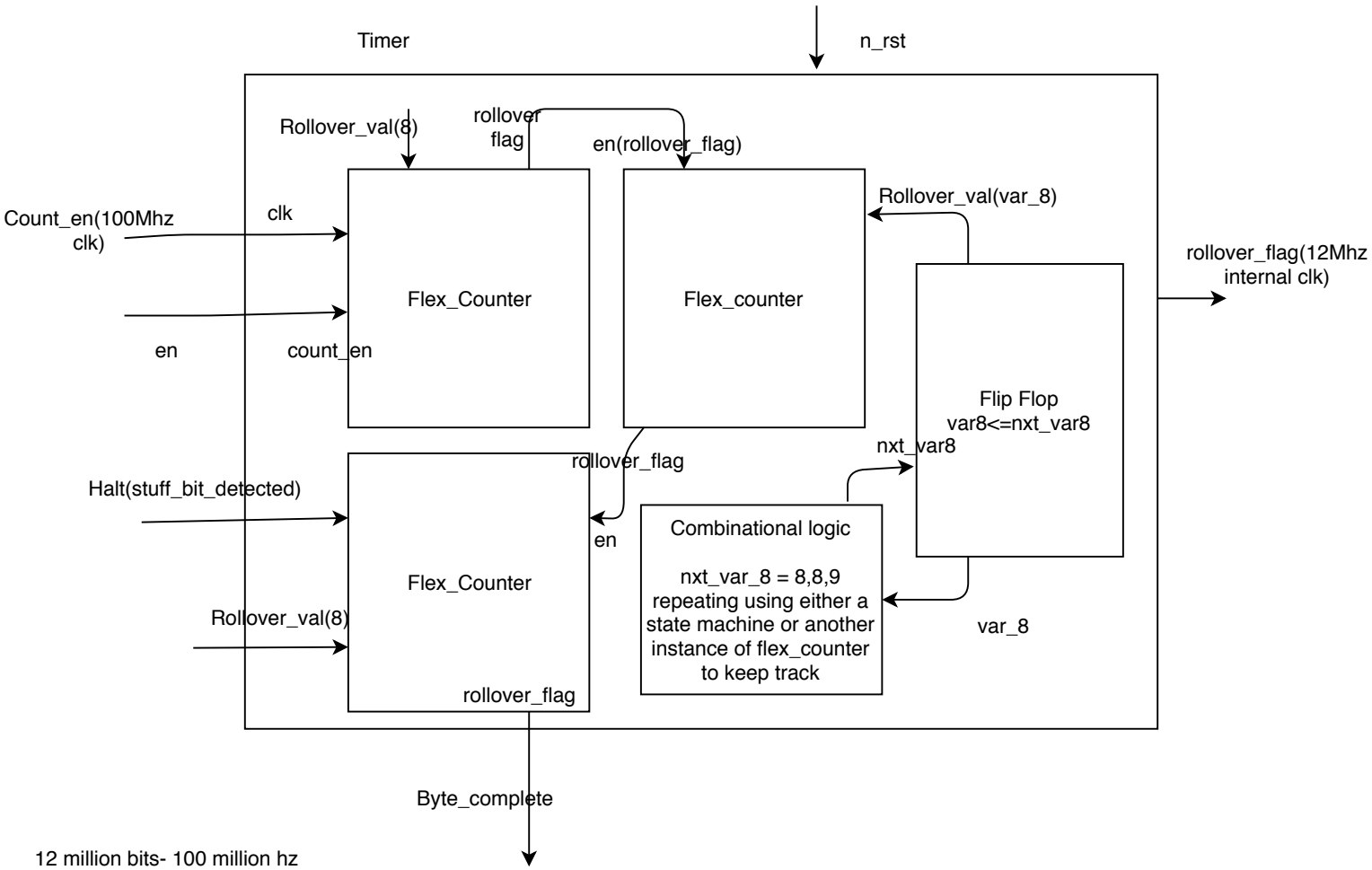
Add multiplexer in PtS take direct Tx packet data
Use 12Mhz clk in everything

CRC takes time, figure A WAy out to fix it

Top Level RTL(Functional RTL for TX)



State Transistion for Controller

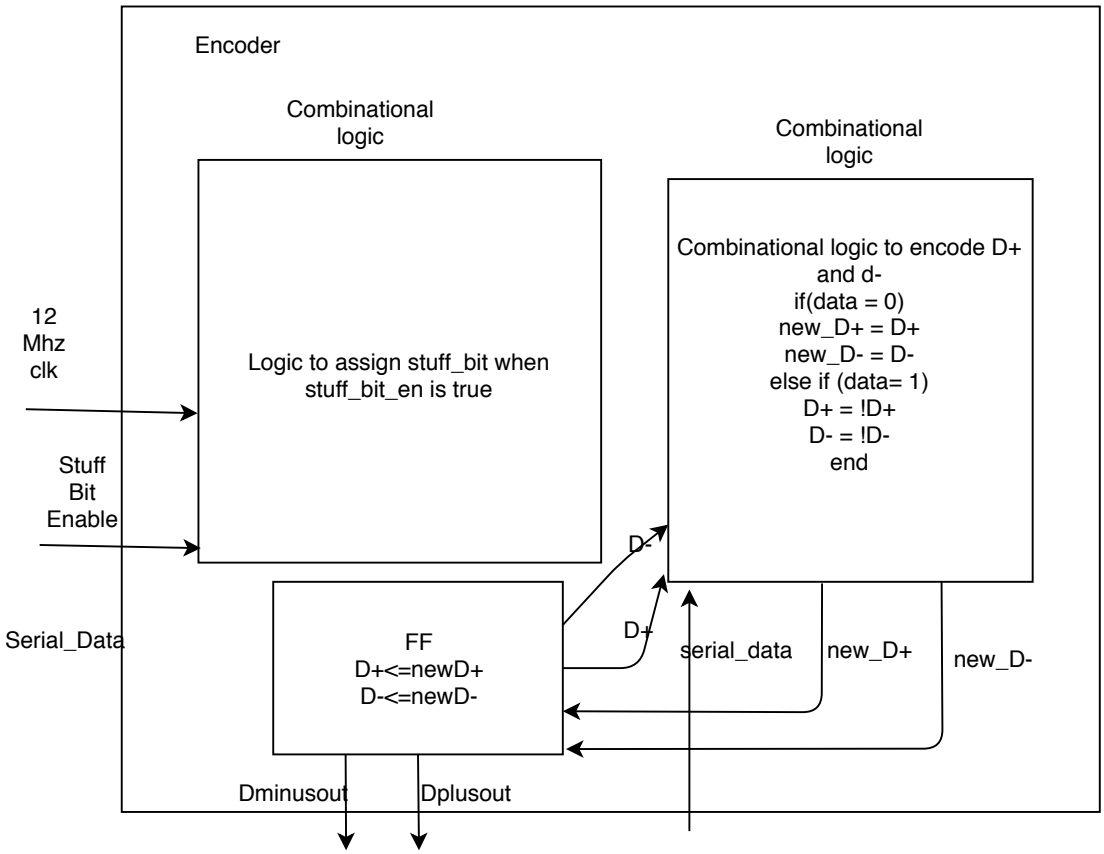


12 million bits- 100 million hz
100/12 = 8..33
call clk divider with val of 8/8/9

Modified my Flex counter to have a halt signal that will halt the counter regardless of enable

Count out is not connected and will be removed as an output from modified flex counter

Timer Functional RTL



Encoder RTL

ENABLE SIGNALS TABLE

Sync enable-
Asserted for 8 clock cycles.Decided Sync value is 8 0 bits

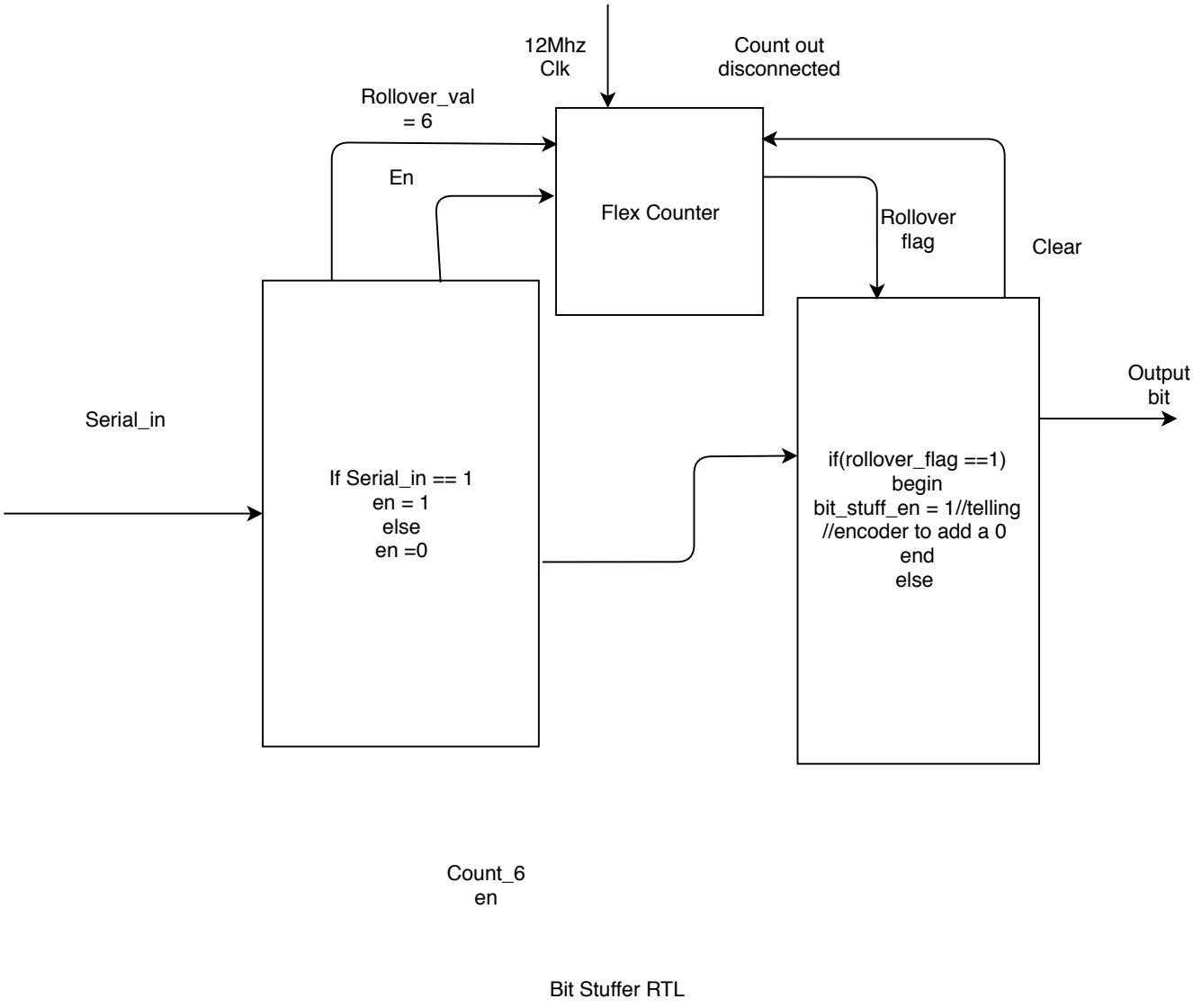
PID enable
Asserted for 8 clock cycles and PID value will have each individual bytes for the PID

Data enable
Can be asserted for 512 clock cycles , while enabled serial bit data will have the corresponding data bit to output

CRCen
Can be asserted for 16 clock cycles.At this time CRC Val will have the individual data bits for the CRC value.

Bit Stuff enable.
Will be enabled for 1 clock cycle at most. Must output a 0 for that clock cycle and carry on with the data output.Data_en will be ignored for this cycle.

EOP enable.
Will be enabled for 2 clock cycles during whcih both d+ and d- must be set to 0 to indicate end of packet.



Bit Stuffer RTL