# PICs

## The overall benefits of (wafer-scale) integration

**Complexity, overall performance, reliability** and **ergonomy** (no need 对齐掩膜) goes up;

While **power consumption, ecological footprint**, and **cost** goes down.

## The typical optical functions (active and passive) on a chip:

Light **source** (laser, III-V, but also absorbing, larger bandgap to make transparent wg);

Light **transportation** (waveguide, **transparent to light** but also has **high refractive index contrast**, confinement but also lossy);

**Wavelength filtering** (resonator, FP, ring, grating);

Signal **modulation** (Thermal, MEMS, Pockels, SAW, Franz-Keldysh);

**Detection** (compact, absorbing, III-V, Germanium/Si);

## The two aspects making SiPh a unique technology platform:

**CMOS compatibility**: The implementation of **high-density** PIC by means of CMOS process technology **in a CMOS lab, complex functionality, compact chips, high volumes, large scale manufacturing.**

**High index contrast** (Si&SiO2) capability to miniaturize the circuitry**, enables tight confinement of light, dense integration of components on chip, sub-wavelength design freedom, and** **small bend radius(1um)**

Indirect bandgap, no emission; high contrast, lossy waveguide; centrosymmetric lattice, no efficient modulation mechanism; Poor absorption for telecom wavelength (1.3-1.55 um), absorptive in visible range

## PICs need electronics and packaging to become a system

Requires **electronics control**, feedback loop, RF signals & electrical IOs, also software configurations;

**Co-packaging** with electronics

## Circuits are connected building blocks

**Functional blocks connected with waveguides**

Some passive components have active tuners, or some built-in linearities, so it’s a grey zone (slow-tuning is allowed to be modelled as passive components)

## Circuit behavior is described by propagating waves

Only **guided modes** (specific spatial profile) in the waveguide,

described by a **complex amplitude on a carrier frequency**, (缓变包络)

component model only calculated relation between incoming and outgoing modes (time and phase delay), requires accurate building block models.

## What goes into a (parametric) building block definition?

Scripted components (code) taking **input (parameters)**,

using **evaluators** (pieces of code generating the content based on parameters) to formulate

**output (multiple views, layout, circuit model, netlist)**

## The concept of a Process Design Kit:

Interface between fab and designer, process specific.

Containing **component libraries** (prescribed, **optimized building blocks**, hopefully a model(component’s simulations and measurements)), **documentations** (**technology and verification rules**), interface with design tools

## S-matrix concept for passive linear devices

Generalized scattering of an incoming wave, (一般有**互易性**，除非磁光,非线性& circulator)

LTI - can be described and analyzed in frequency domain;

superpositions principle: coupling between all ‘ports’(modes, include reflected mode) described by a frequency dependent matrix, S-matrix

**n\_{eff}**: interference pattern

**n\_g**: send pulses through waveguides

## Two ways to use waveguide in a circuit:

Logical connection wire (length and shape doesn’t matter, only need a good connection)

Functional block with certain phase/time delay (length and shape very important, should be treated as building blocks)

# Circuit Design Flow

## Definition of design flow and its purpose:

A set of reproduceable procedure with specific set of outcomes and as little chances of failure as possible, that constructs an object/system from an initial idea.

Purpose: translate ideas into a **working** chip

## Separation of design into ‘front-end’ and ‘back-end’

Front-end: translate ideas into **circuit concepts**, represented by building blocks connected by waveguides;

Back-end: put the functional description of the idea into **physical format able to be fabricated**

## Steps and tools for schematic design (‘Front-end’)

**Design function**: translate the idea into schematics (connected building blocks),

‘design capture’, need to incorporate underlying equations, behavioral models, and flow of information; uses **schematic editor** (graphical representation of netlist with components placement) to select the building blocks and connect them together (Netlist: list of connections and which components the nets are attached to);

As for constructing complex schematics (parametrized, reusable blocks and certain degree of automation), we need to employ **hierarchy**, break the circuits down to unitary subcircuits with simple functions and construct them back up hierarchically

**Simulate function**: verify the schematics, at abstract level, not at full Maxwell level; describe as the redistribution process of incoming wave/mode into output ports (input port also serve as output port)

We need to do it in **dedicated photonics simulators**, instead of SPICE (neglect the vectorial nature of field components) or Effort-Flow systems (not the best formalisms),

but various options, not standardized (**more like RF signals**)

## The most common techniques for optical circuit simulation

**Frequency domain**: LTI passive circuit/component,

**frequency-dependent scattering matrix**: one frequency at a time, gets response between all ports in one operation

**Time domain**: for active components (non-linear),

analyze the **complex envelope** (baseband equivalent, slow-varying) in time-step manner, usually described by some differential equation or functions; **slower** than frequency-domain methods, every excitation requires a new simulation

## Difference between circuit layout and component layout

Component: easier to draw and characterize, manageable units

Circuit: same hierarchy as schematics, **nested cells**, **organized in (reusable) cells**,

**Cell placements** and **transformations**, **waveguide routing** (optical, **1-layer**, no vias and 3-d geometry) and **metal wiring** (electrical), while also avoiding crossings/shorts/disconnects (designed crossing);

Constraints: optical length and phase control; minimum bend radius (metal wiring always straight); waveguide spacing (process-specified); matching port direction (0/180), single routing layer

schematics performing much complex functions, and hence the front-end transition may not be one-time right and requires multiple iterations. (**Layout versus Schematic**)

## What is schematic driven layout?

Derive **(layout)** information from **circuit schematic** (component placement and connectivity), define in python code:

1. Generate layout (P)Cells: List **building blocks** (or sub ckts.): gc, splitter, wg, …
2. Place layout Cells: Defined later in ‘translation’ dictionary
3. Connect the layout cells together: List **internal connections**: gc:out-splitter in, …

Define **external ports**

**Better do it manual+auto to achieve optimal placement**

## Design Rule Check

1. Minimum feature size (&spacing): Edge, width,
2. **Curved geometry**: acute angle, all-angle waveguides, nm scale sensitivities
3. Overlap: waveguide crossing
4. Pattern density: must be **sufficiently uniform** to achieve etch rate control and avoid CMP dishing (conditioning of etch chamber) – add tiles

## What is Layout versus Schematic?

Correspondence of layout with circuit schematic; parasitic effects existing in layout.

Check: connectivity (properly placed and connected?); functionality (right parameter, width, optical length, …),

**discretization approximating smooth geometries, which can cause discrepancy between layout and schematic**

**Retrace to layout and schematic (may not be manufacturable) and adjust**

**Finally do simulation (in time domain, waveform)**

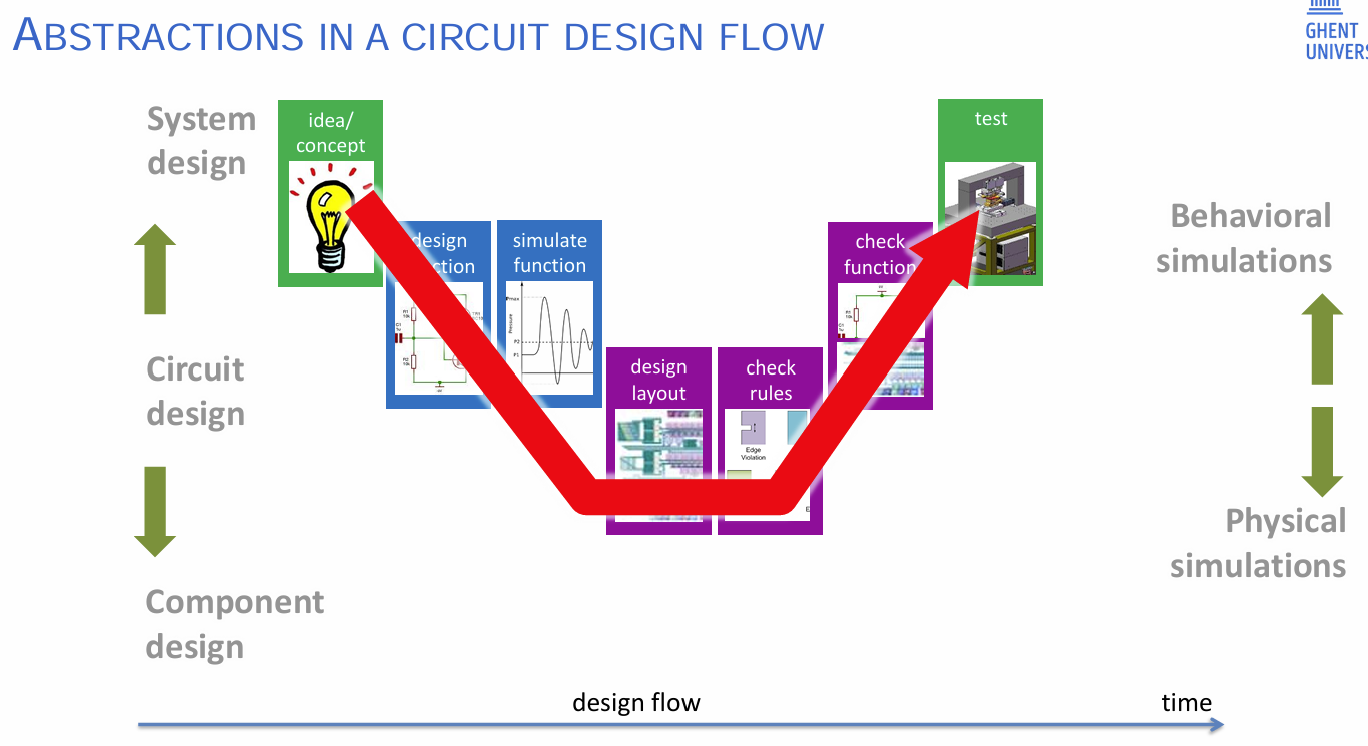
## Use of hierarchy in circuit design; PDK

Reusable circuit building blocks, instantiate defined component in the new class

levels of abstraction: physical simulation -> behavioral simulations

component design (preferably handled by the fab) -> circuit design -> system design (testing)

V-shape approach: system (idea/concept) – circuit (schematic, design function & simulate function) – component/layout (design layout & DRC) – circuit (check function, layout versus schematic) – system (fabricate & test)



**Focusing on circuit & system design and hand over component design to fab (interface: PDK, see process design kit), enabling designer to operate at their level of abstraction and omit EM simulations;**

**Electronics innovation happens on circuit level;**

**Current Photonics research requires go deeper in the level of abstraction (circuit):**

**More geometry design freedom (photonics crystal; holographic …); more complex behavior (phase: interference effects; wavelength dependence; nonlinearities)**

**Component design: layout (physical description) – geometry – simulation – packaged into reusable units able to be utilized in circuit designs**

**Circuit design: Circuit capture (abstract) – simulation – layout (physically viable)**

## GUI and code pros & cons in oral exam to be expected.

**Graphical editor**: drag and drop components from library, quick point and click (WYSIWYG, what u c is what u get), suitable for prototyping, but difficult to scale up, all manual labor (not reusabke), and easily making invisible mistakes (not robust)

Schematic connectivity; layout positioning (floorplanning); fixing the last DRC errors; quick manual routing

Code: automate with script, reduce error and time,

easier to parametrize/reuse/update/version control/documentation,

numerically correct, but no immediate visual feedback

Parameter sweeps; circuit models; automatic placement and routing

# Mask Layout & PCells (Prior to Fabrication)

## Understand how a layout relates to the fabrication process

Back-end design, translate into patterns able to be fabricated

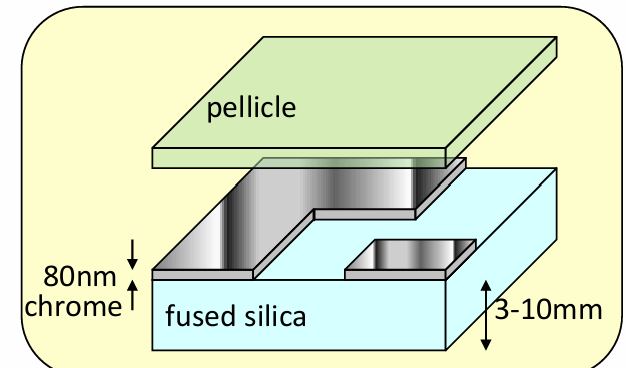
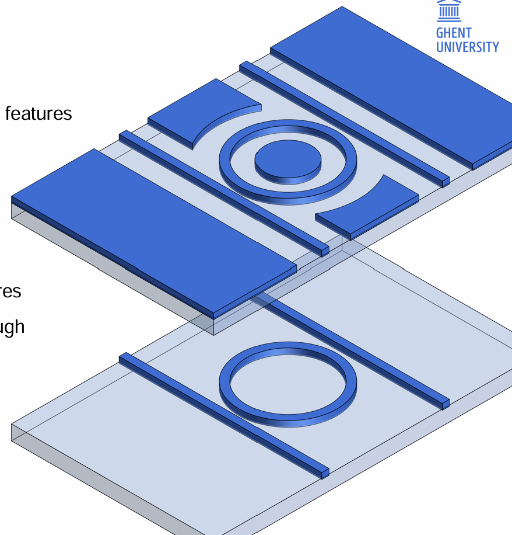
Spincoat-lithography (transfer pattern to resist)-etch (transfer pattern to Silicon)-strip the resist – pattern transfer

## What is a reticle? Dark-field and Light-field

Chrome (opaque) on glass plate (transparent to UV light, >90% transmission),

fabricated with direct-write lithography and etch, typically 4\*-5\* larger than chip to reduce error (when used for projection lithography)

illumination: chrome-down (fused silica-chrome pattern-pellicle, to keep out particles)



Defined for positive resists:

Dark-field (field: background image of the mask)

Chrome with transparent features (light mostly blocked),

dark background, write the trench (surrounding get exposed)

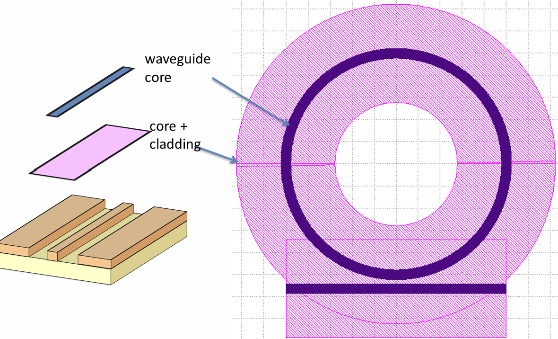
**Preferred in SiPh, easier to control amount of stray light, complicate defining pattern**

Light-field:

Glass with chrome features, a lot of light coming through,

write the ‘line’ (layout structure itself is blocked)

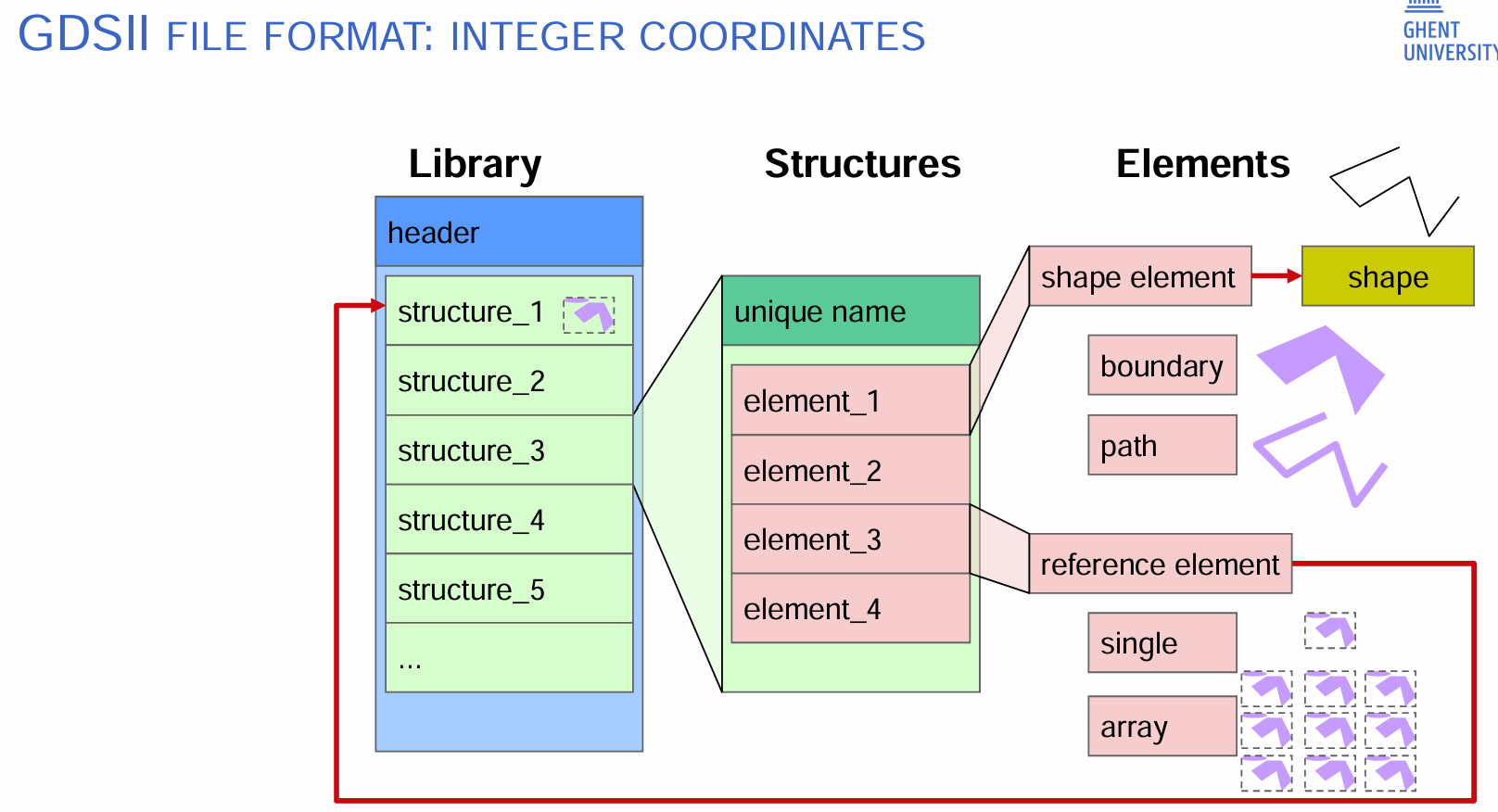
## Use of mask layers, e.g. for defining waveguides

Use a combination of light and dark patterns (2 logical layers, core & cladding layer) to define the structure itself and trenches separately;

Two layers overlapping, the end pattern to be transferred to wafer is **Boolean operation** of two layers, core being subtracted from cladding layer (positive resist)

## High-level understanding of the GDSII structure, primitives and use of hierarchy.

Design is separated in cells (‘structures’), containing polygons and references to other cells, formatted in binary stream (typical way to transfer layout to tape-out mask, ‘sending to fab’)



GDSII: **library** consists of cells (**structures**), serially streamed;

Structures need to have **unique names** to prevent overlapping, consists of multiple **elements**, either **shape** (geometry, boundary/path) or **reference** (single placement/array)

**Hierarchy**: consisting element of a structure is reference of another structure

**Boundary:** always closed

**Path:** open by default with defined width, different possible styles

Shape elements: **polygon**(boundary) or **path**, **geometric primitives** defined on a **layer**,

list of points, coordinates of which are **integer multiples of fixed grid,**

**Discretize curvilinear shapes and snapping them to the grid**

**Preferred way:**  discretize the polygon, not the center line

## GDSII transformations and how they can cause DRC errors

Native to GDSII, no distortion incurred

* Translation
* Rotation
* Mirroring (vertical, horizontal, or point)
* Magnification (don’t use!!!)

Rotation of arbitrary angle (not multiples of 90 deg), positions are calculated but not snapped together, giving rise to small gaps on export.

**Grid snapping** correct small errors in design; (integer coordinates in klayout/gds, each component has its own internal coordinate systems, so they won’t be stitched together, but leaving small gaps in between)

## Common DRC errors, their causes and how to fix them.

Design Rule Violations:

* Edge violation
* Spacing violation
* Width violation
* Encapsulation violation

Sharp angles:

Waveguide trenches intersection, needs to be fixed; add rectangle

Nanometer gaps:

Waveguide ports not matching well: snap to grid, flatten

## The concept of a PCell (views, properties and evaluators)

Generate different aspects of design (symbol view, layout, netlist view (location and orientation of ports), model) based on input parameters, dynamically

Input: user parameters:

Evaluator function: piece of software code, tool-vendor dependent

Output: data

Hierarchical parameters: global parameters defined for all views;

Parameters defined for each view separately (layer in LayoutView, …)

PCell defined as a Python class, and the views defined as classes inside the PCell class, \_generate\_elements as layout evaluator

## Different views in a PCell.

1. Symbol view: symbolic drawing with I/O ports/terms (optical/electrical), with parameters,

Visualized in schematic editor.

1. Netlist view: internal connectivity of building blocks, circuit elements and connection between ports
2. Schematic view: netlist + graphical information, position of instances + shapes of connecting wires
3. Layout view: Hierarchical description of polygons on layers (Raw polygons; Instances of other cells, single/array); parametrization is used intensively for reusage
4. Model view: allow simulation in a larger circuit, not standardized (based on equations, measurement data, EM simulations, …)

## Summary on Layout, PCells and DRC:

Back-end design process generating patterns for fabrication:

requires compatibility with the writing process (optical/e-beam, reticles (masks, Boolean operation of cladding layer minus core layer), …)

File format in GDSII, serially streamed file, library-structure-elements (geometry/reference to other structure)

PCells design allows partitioning (different views, class defined inside class; hierarchy of parameters and elements)

DRC finds unwanted errors (violation, sharp angle, nanometer gaps,…)

# The design project

## Understand the process

Passive chip with 2-layer SiPh PDK

## Two different uses of waveguides

- waveguides as connections (PlaceAndAutoRoute)

Generate waveguides for connections, place the components to prescribed positions and orientation (define **‘transformation’ dictionary** afterwards) and logical connections are placed accordingly.

- waveguides as components (AutoPlaceAndConnect)

Circuits with direct connections, no waveguide generations (building blocks instantiated upfront, full-control over wg length)

# Waveguides & PIC platforms

## Basic operational principle of optical waveguide:

Trap light in a guiding core with horizontal & vertical index contrast (higher index core, lower index cladding), no more diffraction, can propagate in curved route (no necessarily straight)

NA\*d dimension

Low index contrast – larger dimension but also lower loss (glass fibers)

## Concept of (guided) modes:

b-V curves, dimension

dispersion relation: between two light lines, converges to lower (core material’s line)

goos-hanschen phase shift displace the mode from node points,

TE TM no longer overlapping necessarily

## Difference between effective index and group index:

When propagating in a medium defines the traveling speed of a single frequency component, propagation constant over vacuum wavenumber

Dispersive behavior + signal is narrow-banded instead of single-frequency -> defines the traveling speed of a wave packet (how information travels along the medium) ,

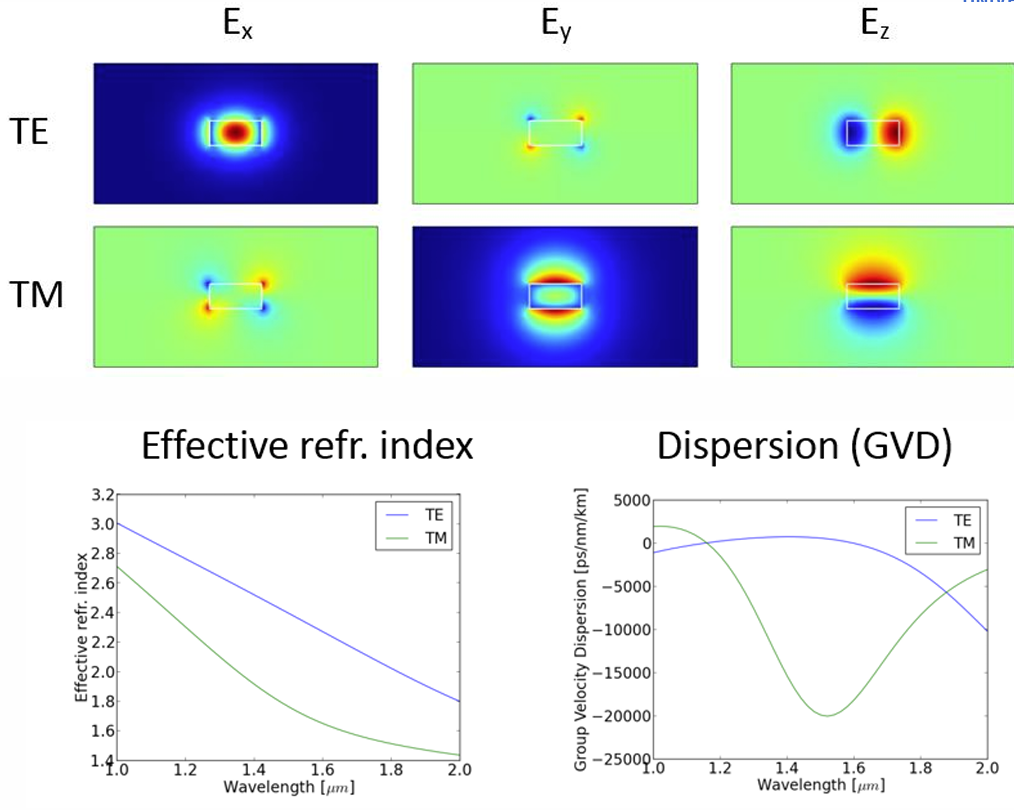
**traffic jam** analogy, propagation of fine structure and modulating envelope

## Polarization of optical modes (TE & TM):

Vectorial nature comes into play at interface, Amount of reflection and phase change is different for different polarizations:

TE: E perpendicular to surface normal

TM H perpendicular to surface normal



Different mode profiles: TE lying down (discontinuities on sidewalls), TM standing up (discontinuities on top and bottom), due to rectangular geometry,

TE is fundamental, mostly confined – higher refractive index than TM,

Also with the shrinkage of dimension (larger wavelength), TM is essentially cut off; dispersion of TM is much stronger, badly controlled.

## Effect of index contrast:

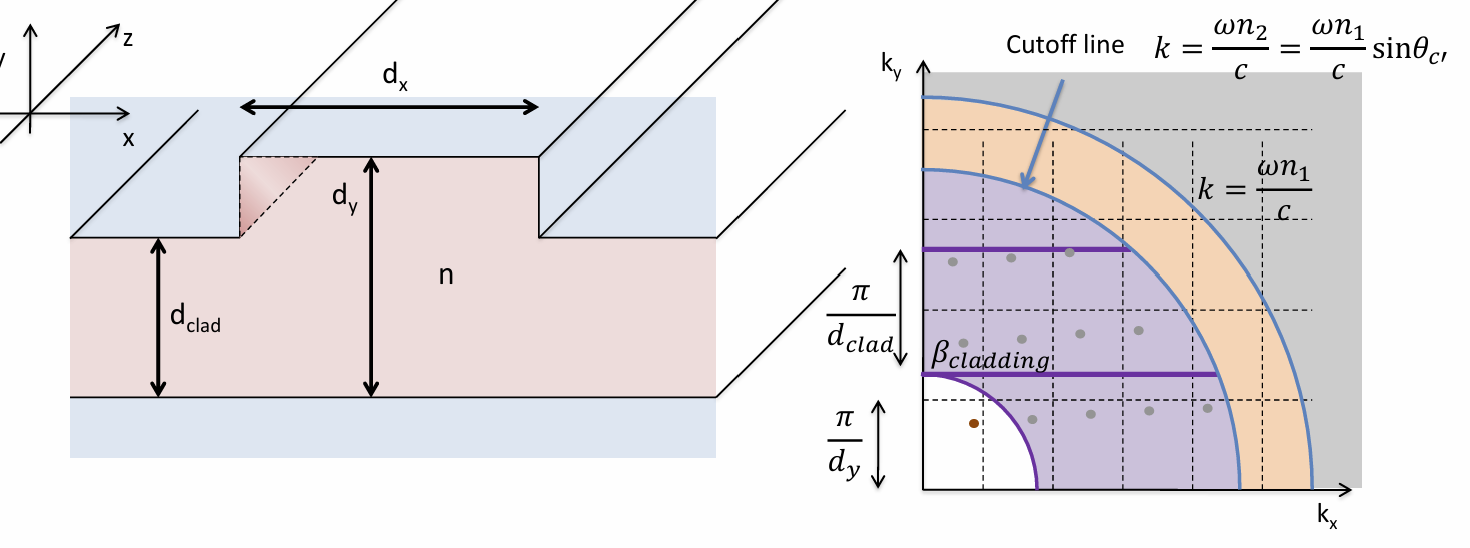
Also determines the confinement degree (in the core) and number of modes M ~ 4 \* cross-section \* NA^2 -> the dimension of **single-mode waveguide**

High contrast of Si/SiO2 shrink the size of silicon waveguide to micron scale

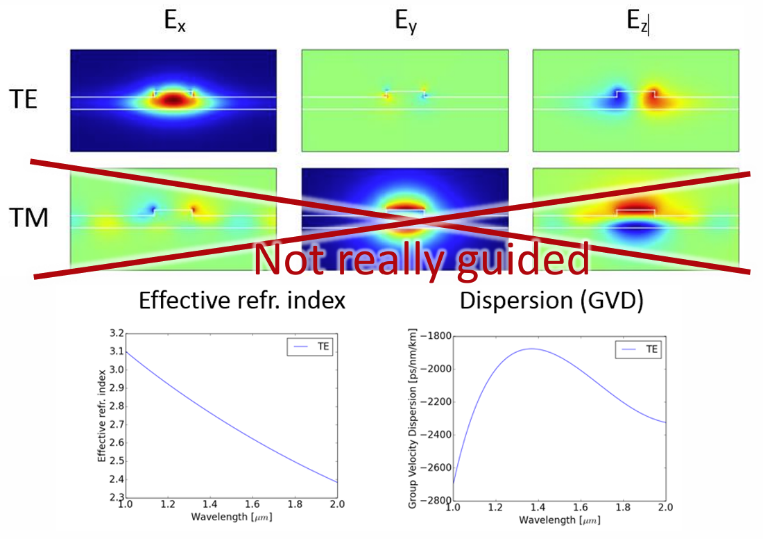
If index contrast becomes too strong, single-mode waveguide pushes the mode outward and no longer confining it inside the core but still guided, this can be utilized to making a taper

Rib waveguide: another way to make single-mode waveguide with large geometry; core is slightly thicker waveguide; cladding also a waveguide (infinitely planar),

Purple lines: guided mode in the cladding, Finite in vertical direction, can propagate in horizontal direction, any modes exceeding the first purple line is leaked into the horizontal modes (no longer confined), and hence drawing a circle and making it single-mode

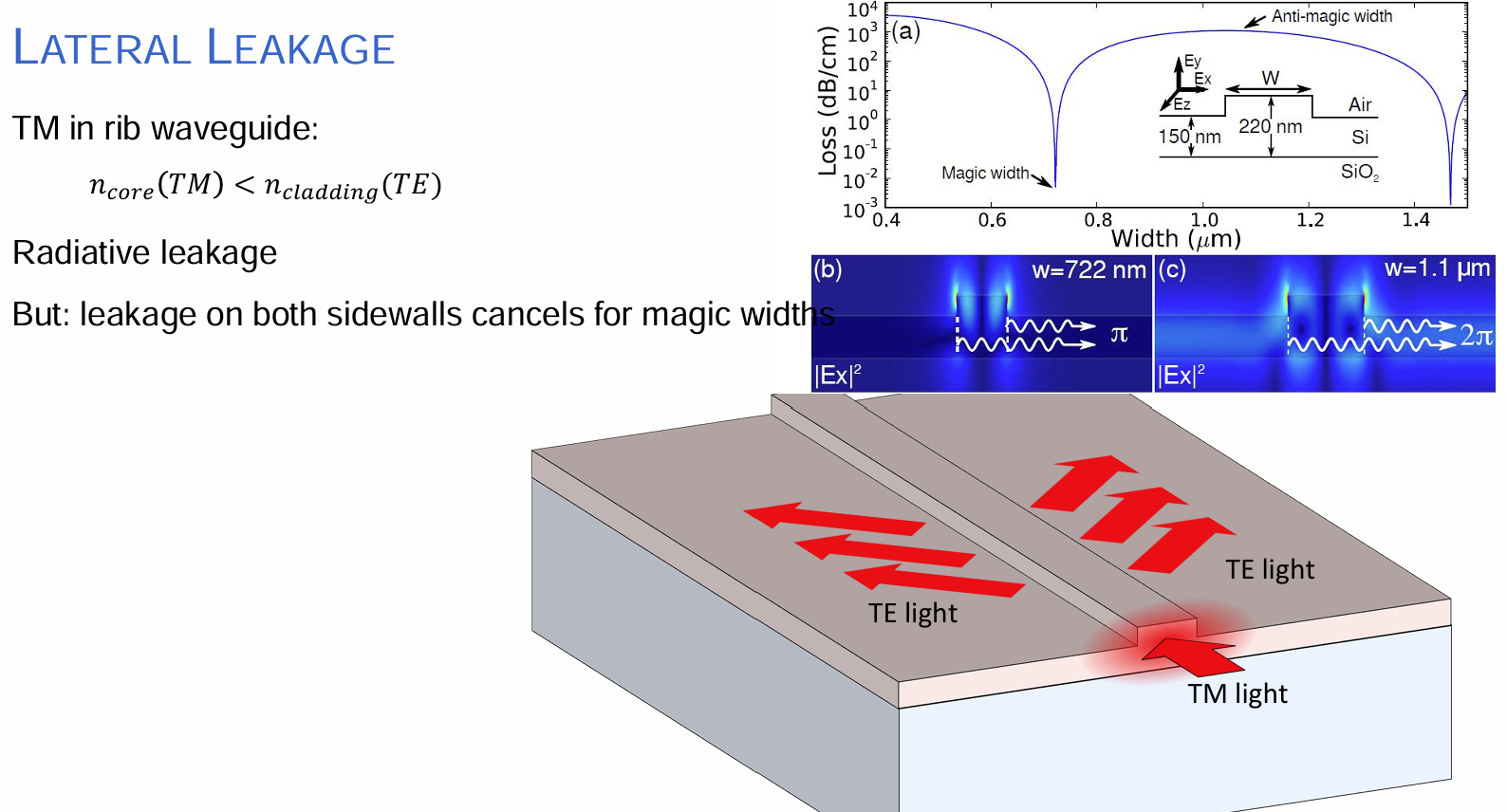


High index contrast, large dimension and single-mode – rib waveguide (effective slab index, can also explain the weak contrast in the horizontal direction)



TM mode profile is obtained, but is computed inside a metal box due to algorithm; but **not physically true**, actually coupled into the radiation mode in horizontal direction.

Lateral leakage: cancelling out leakage to realize propagating TM modes (非必要)



## Effect of bend losses in optical waveguides:

Some rays of light are outside TIR range (no longer fully confined) and hence leaks away

Wavefront revolves around the center, group velocity of which cannot exceed c/n, hence at certain point wavefront curves and radiates

Tradeoff: compactness (small bend radii) – radiation losses

Mode adaptation loss (peaks shifting outwards)

## Effect of dispersion in optical waveguides:

Pulse broadening, range of wavelength,

normal dispersion, red travels faster

anomalous dispersion, blue travels faster

crossover point – zero dispersion

## Loss mechanisms in optical waveguides:

Propagation loss in waveguide:

Interaction light-material – absorption

Imperfection in the waveguide (spatial refractive index variations, rough interfaces) – scattering

Imperfect guiding – radiation (oscillation exists outside the core)

By absorptions: multi-photon absorption (nonlinear), free carrier absorption

By scattering: At **bulk irregularities** (subwavelength refractive index fluctuations, Rayleigh scattering-fourth-power law)

At **geometrical irregularities** (variations in geometry of the waveguide, depend on fabrication process; high index contrast, stronger scattering , larger perturbance, sensitive to **surface non-uniformity**: etched sidewalls of the waveguide, interface between grown layers



Radiation leakage: fundamental loss mechanism

Imperfect waveguiding: adjacent area with higher refractive index – draws the mode over and power is leaked (SOI, leakage into substrate)

## Material systems for ICs (和调制方式整理在一起了)

# Components & Building blocks

## Distinction between active/passive building blocks

Redistribution of light, store, leak, scatter photons; not modified, just redistributed; no electro-optic effect; linear component, frequency-domain analysis, described by S-matrix;

Modifies the frequency, nonlinear, generation/modulation/detection;

Time-domain analysis/coupled mode theory, not in frequency domain

Passive: Transporting and distributing light;

Filtering light, according to wavelength/polarization; Coupling light

Coupling light: between waveguides = between modes (**think in terms of modes**)

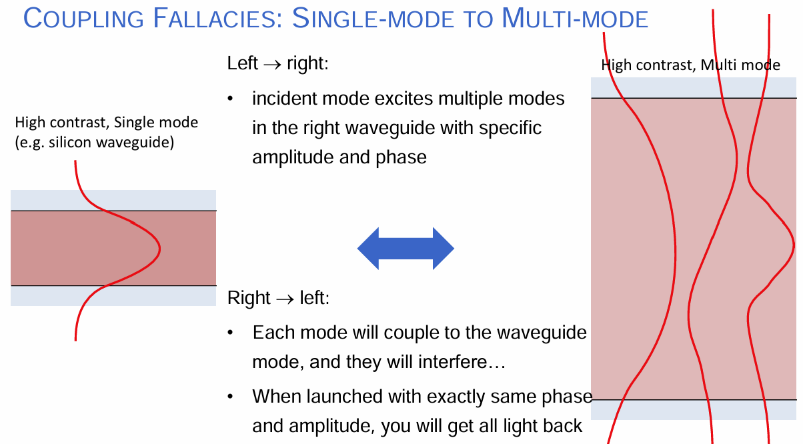
2 determining factors:

overlap of mode profile;

compatible modal propagation with same constant

(other available modes to couple to, including radiation)

Reciprocal (transmission, reflection), between same pair of modes



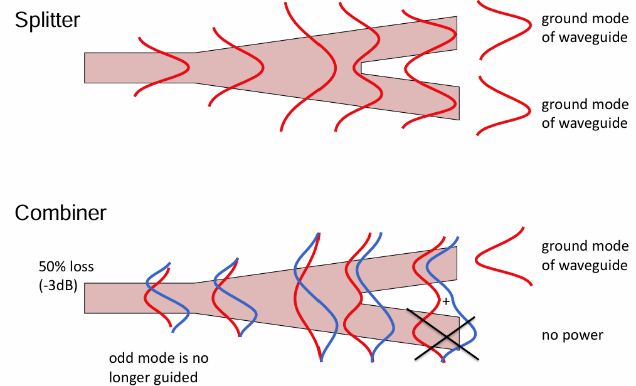
左->右：

100%功率保留，但会进入不同的的mode

Coupling定义在mode之间，而非波导之间

右->左：

部分进入single mode,其他的radiate



Think in terms of odd/even mode, instead zero/yes input in the waveguide,

1\*2 coupler: lossy in nature

## Operational principles of directional coupler:

90-degree phase shift in cross port

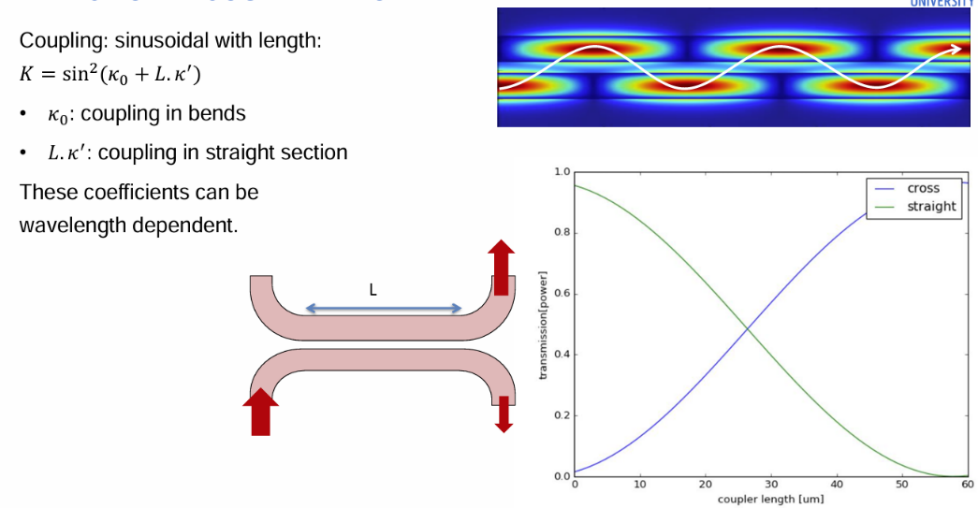
Interference between even and odd mode in double waveguide, propagating at different phase velocities

-odd mode propagates faster, starts beating

– field coupling between the two waveguides sinusoidally

design to achieve the desired power splitting ratio ();

can essentially lossless if properly designed (due to 2-mode interference, and 2I2O schematic)

Power coupling (sum of coupling in the bends and straight section),

50-50 splitting only

at a single ,

(make a choice, equal splitting/half of the power output in 1 port)

## Understand the working of the Multimode interferometer:

Nice imaging pattern, make 1 to n splitter, distribute to more than 2 ports; concentrate again in some distance

Large width, capability to excite and support multiple modes, the modes evolve with different phase shift, able to fabricate power divider, and **inherently lossy**.(can’t retrieve them back wholly after exciting them)

Cross-coupling coefficient, phase delay

Other coupling schemes:

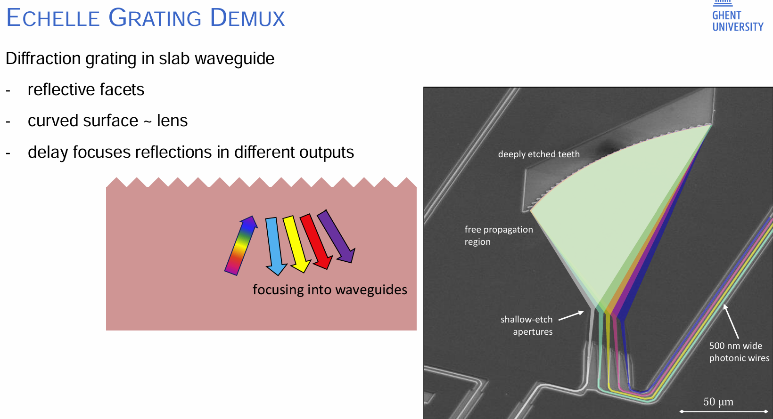
Adiabatic coupler, multimode-interference taper, crossing (horn-antenna)

## Different wavelength filters

* Channel drop filter: with selected passband from a wavelength range
* Interleaver: separates alternating wavelength bands
* Demultiplexer: separates into multiple wavelength channels

Filter principles: interferometry, cancel out transmission of selected wavelengths,

separate into multiple delay lines, add different phase delays, and combine back

MZI: 2-arm filters, sinusoidal spectral response

AWG: distribute and combine light through free-propagation region (FPR) into delay lines

Gratings: periodic reflectors, in-line (Bragg), FPR (echelle), high index contrast – compact features

Ring: infinite delay lines through circulating the ring circumference, quality factor \propto cavity losses

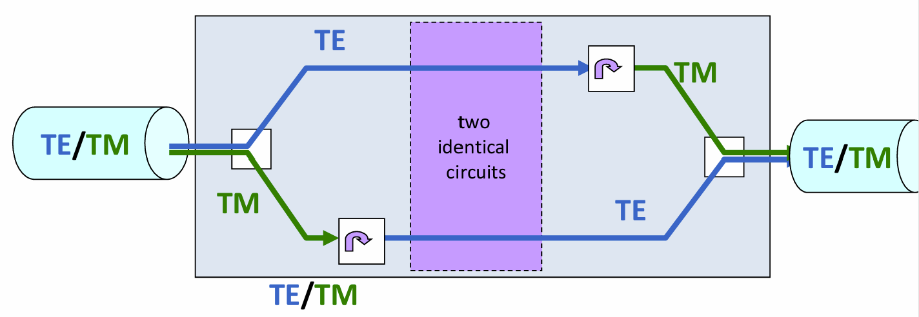
## Optical fiber coupling mechanisms (mostly for Silicon):

**Inverted tapers** (shrinking down the size of taper gradually to let it explode at the end, to match the mode diameter inside fiber, expanding or reshaping waveguide mode)

Overlap is also polarizing sensitive, optical fiber has 2 degenerate polarizations; susceptible to strain and temperature variation and unable to distinguish

– coupling to on-chip waveguides requires special treatment (different fiber coupling efficiency and difference propagation constant

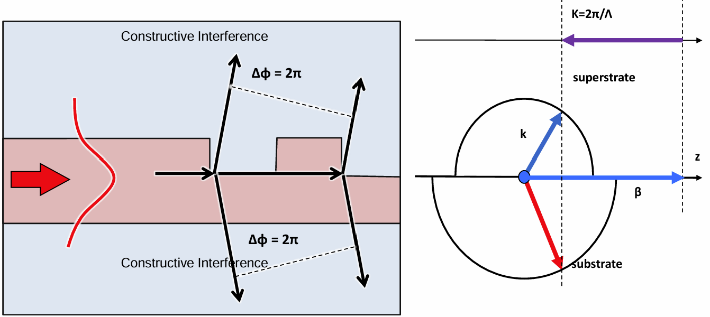
**Grating couplers**, only for silicon photonics, platforms with high index contrast, to make diffraction grating compact enough, limited wavelength range

Split into two separate lines; TM then converted to TE through rotation; then two lines processed through identical circuits; then TE line is rotated to TM (**for reciprocity**) and combined together

Polarization rotation scheme: directional, coupler mode interference, adiabatic, evolution, …

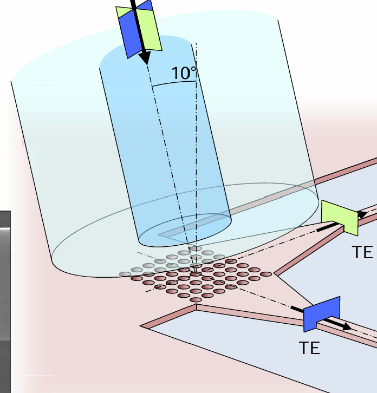
## Understanding the working of grating couplers:

Diffraction grating’s periodic ridges provides **sufficient scattering** in 20 periods, the size of a fiber mode to scatter all the line; other platforms don’t have strong enough scattering

Couples light from fiber into waveguide, wavelength dependent (parabolic profile); linear, reciprocal, reflections between GCs form an FP etalon and hence little ripples in the pattern, FSR characterized by the overall circuit length.

Polarization sensitive, only works for TE;

prevent back reflection (2nd order diffraction), tilt angle (determines the coupling wavelength)

antireflection coating (mirror, creating constructive interference pattern towards fiber) on the bottom to prevent diffraction scattering under; adjust the thickness of upward and downward tooth depth

Exponential profile, attenuating by nature – apodizing, adjust the spacing and size of ridges to achieve Gaussian profile

Realize polarization splitting, through 2D grating; both end up in TE polarization, polarization splitter realized as well.

## Electro-Optic modulation and tuning techniques:

Amplitude/phase-modulated, electrical signal modifies it

Different applications:

* Tuning: slow, analog, modifies the structure in quasi-static way
* Switching: slow, digital(< kHz), full amplitude, on-off 2 way
* Signal modulation: fast (GHz-100GHz), amplitude (hard) or phase (easy)

Amplitude modulation

* Direct: absorption (electro-absorption; free carrier absorption)
* Indirect: phase modulation in delay arms
* Change refractive index (thermal, slow; carrier injection/modulation)
* Resonator (on resonance/away from resonance)
* Interferometer (MZI)

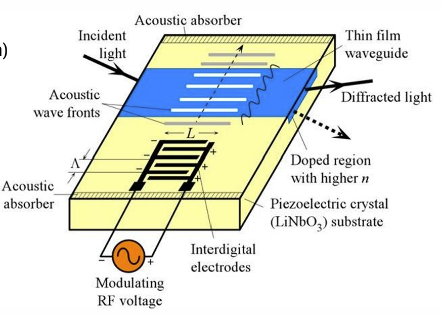
**Heater:** phase shifter, metal pad on top, 1um away (insulation layer in between),

thermal crosstalk (leakage to adjacent ones) and power consumption – bad for integration and compactness

**MEMS** (Micro-ElectroMechanical Systems, mechanical modulation, switching, tuning)

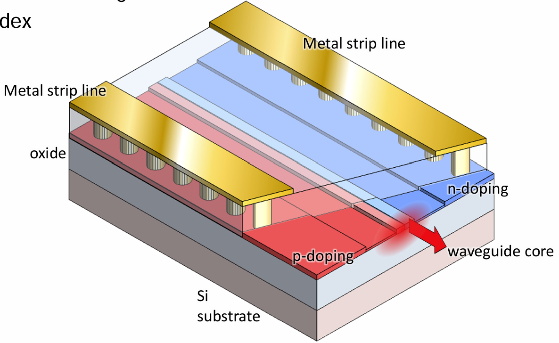
changes coupling by inducing strain and movement, changing the coupling of evanescent fields (<MHz)

Requires electro-mechanical actuation, mechanical stiffness, release/undercut process

Acoustic Modulation (piezo-electric effect, use mechanical waves instead of movements)

**SAW** (Surface-Acoustic Wave, modulates the refractive index via strain)

LiNbO3,…

Modulators in Silicon: **Carrier absorption**

Adding doped junction (carrier concentration) to waveguide to modulate refractive index (plasma dispersion effect, )

**Modulate carrier density in waveguide**:

Phase modulation

Amplitude modulation (free carrier absorption)

Speed limited by RC constant

**Carrier-based ring**: amplitude+phase modulation

resonance shifts, extinction ratio changes (absorption ratio changes)

**Franz-Keldysh Effect**: High E field + right material (with suitable bandgap)

E field tilts the band diagram, shifts the absorption band edge in semiconductor;

(加电场, Eg变大, 吸收->透明)

can be enhanced through quantum well (quantum-confined Stark Effect)

Also introduce phase shift (chirp)

**Pockels Effect**: Right material + High E field

intrinsic EO effect, linear change in with external E field,

nearly instantaneous (~ps)

Requires material with strong nonlinear effect (Lithium Niobate, Barium Titanate, …)

Polymers (push-pull MZI, slot waveguides)

## Photodetection techniques:

**Photobolometer** (absorption heats up the device and changes the electrical resistivity);

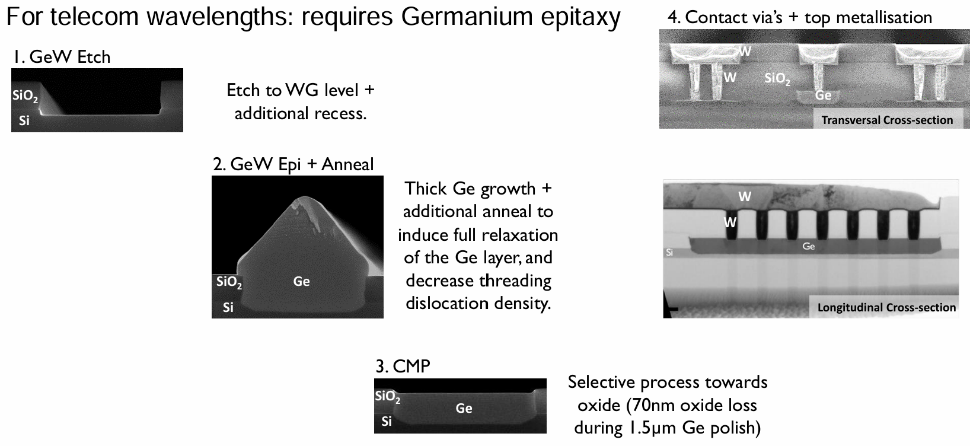
**Photoconductor** (absorption creates free carrier)

**Photodiode** (electron-hole pair generation, most effective, pin, msm diode);

**Photodiodes**: good responsivity, III-V semiconductors (direct bandgap), Ge used for Si

reverse-biased p-i-n junction, absorbing material, good carrier collection, low RC (fast operation, low series resistance and capacitance)

**Epitaxy growth of Ge on Si for photodetector**



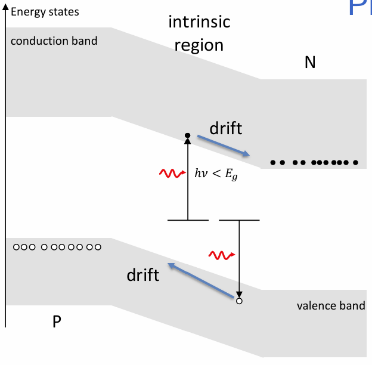
Only grow on Si, not on SiO2 – CMP planarization

Parameters:

Responsivity,

Bandwidth,

Dark current



**Photoconduction** – defect mediated

Defects can absorb photons with energy smaller bandgap

(surface states on sidewalls, lattice defect)

Less efficient than photodiode, can be combined with diode for collection, usually slower

**Bolometer**: when no direct way to generate current (large lambda)

Absorb light – material heats up – measure temperature

Speed determined by thermal mass/conduction, temperature measured 电/光

– superconducting material sensitive for single-photon detection

## Gain mechanisms (for lasers and amplifiers):

Gain: direct bandgap semiconductors being electrically pumped, rare-earth doping (EDFA), nonlinear scattering…

Introducing optical gain: with correct bandgap (heteroepitaxy, bandgap engineering)

Heterostructure – active layer embedded between cladding with higher bandgap

Whereas gain also incurs absorption, so separation between waveguide and gain section is needed – **active-passive integration**

Heterogeneous integration:

Micro-package, flip-chip (alignment, low scalability),

Die-to-wafer bonding (good local alignment, wasting substrate) micro-transfer printing(cost-efficient)

## What can affect a component’s performance:

* Geometry
* Materials
* Environment (T, stress)
* Fabrication process
* Neighbors (thermal crosstalk, em crosstalk – temperature gradient)

Geometry: differ from design due to process limitations

in simulations, represent by rectangles (2.5D)

vertical: layer stacks, process-defined

in-plane: mask layout, from gds file

Real fab:

Biases, corner rounding,

proximity effects (Electron scattering, EBeam),

sidewall slopes, roughness, variability

fabrication process simulation: TCAD

## Integration strategies with electronics:

More than optics: electronics control the system, I/O, feedback loops, actuators and monitors, software layers …

**Front-end integration**: embed photonics in the transistor layer,

Incompatible layer thickness (Electronics, 55nm Si on 145nm SiO2);

Photonics: wg far away from substrate to prevent radiation leakage (different constraints on insulation layer, 0.2-0.4um Si on 0.4-3mm SiO2)

trade-off for integration: dedicated substrate (sufficient oxide and waveguide thickness)

Develop CMOS process, change local BOX(oxide) thickness, original process

**Back-end integration:** put photonics in information-processing layers

Hard to make active device (deposition of material) due to lack of crystal/substrate(modulator, detector); BEOL full of metal, lossy

**Separated photonics and electronics and bonded together: co-packaging** (wire-bonding, flip-chip,…), 3-D stacking, monolithic integration (only with silicon, front-end: photonics and transistors; back-end: photonics and metals)

Monolithic integration: material compatibility, temperature compatibility (deposition and annealing), codesign (design rules,…)

# Component Simulation

## Difference between component design and circuit design:

Circuit design only an abstraction:

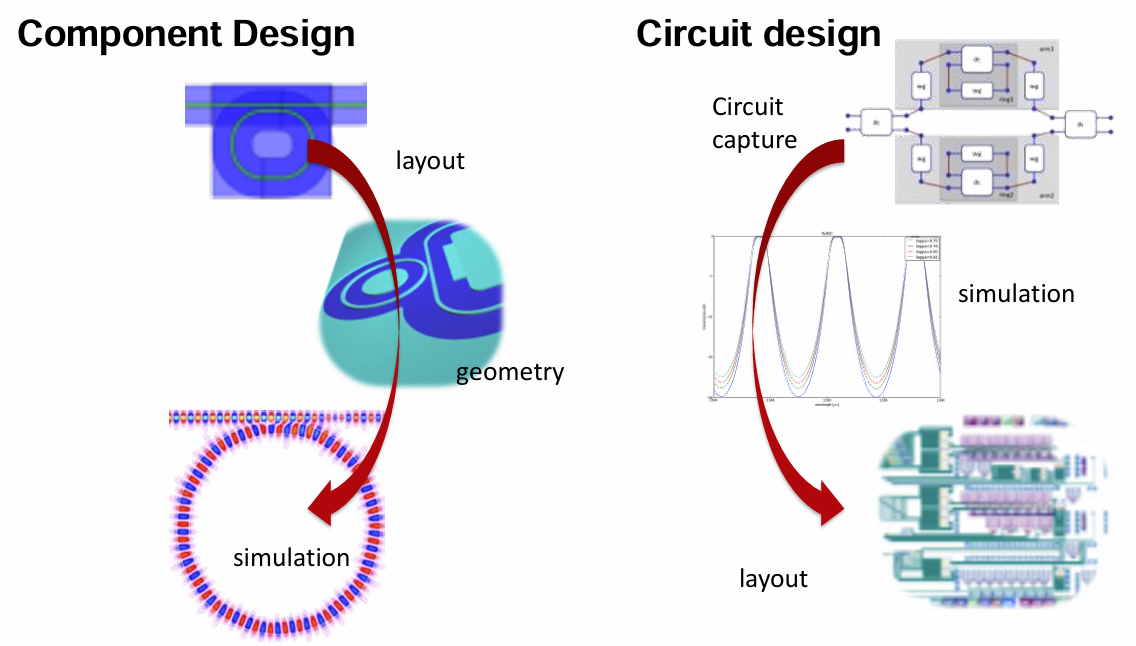
real object behind this symbol,

Signals are real EM waves instead of complex envelopes, geometries in the layout differs from real fabrication

Light isn’t confined entirely to the waveguide

should look into components, physical level during design

component design: physical design



**Component design: layout** (physical description, 3D geometry) **– simulation – extract parameters** to build a model and **package** into reusable units able to be utilized in circuit designs

**Circuit design: Circuit capture** (abstract, schematic) **– simulation – layout** (physically viable)

Component design – perform intended functions (filtering, modulation, detection, emission,…)

## Explain how photonic components require Multiphysics:

Optical (Maxwell)

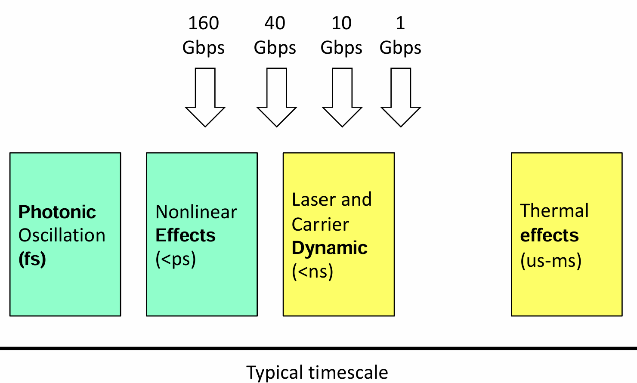
– Electrical (modulation/detection)

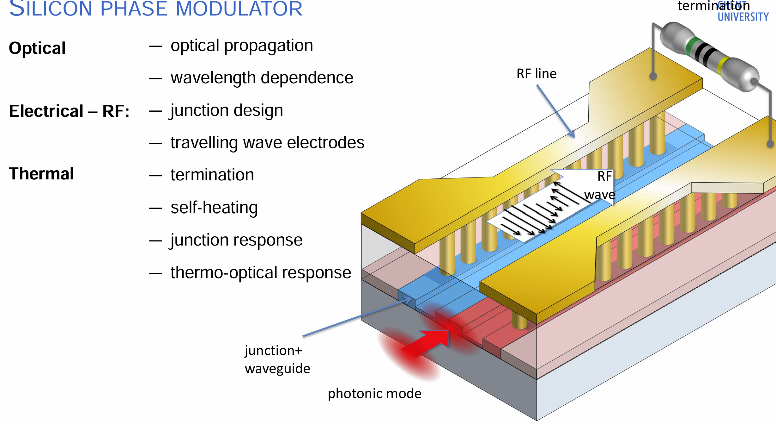
– Thermal (semiconductor热敏的)

RF (high-speed RF signals), Fluidic(Sensing), Chemistry, Mechanics(MEMS), Stress,…

Not just equations, but also time scales different

## Understand timescales for modelling components:

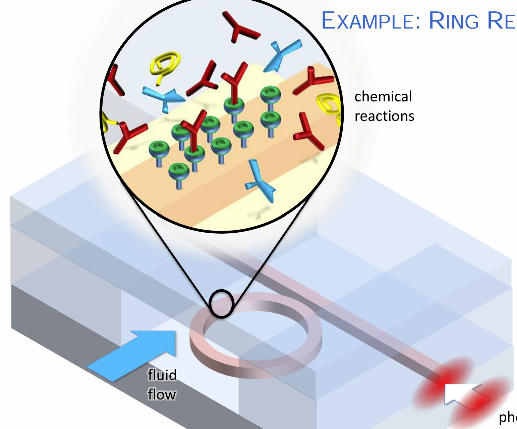
Timescale discrepancy between physical simulation (real oscillation) and functional simulations (modulated signals)

rf signal changes refractive index of the waveguide and optical mode feels that

rf wave same propagation speed as optical mode; TWE

variation of refractive index; junction design; rf signal not attenuated;

heating in the junction and termination – thermal effect – thermal-optics effect



Optical (lambda-dependent,

optical binding response)

Fluidic (flow and diffusion of the fluid)

Thermal (noise, bio-reaction might be thermal-dependent)

Chemical: diffusion, binding

More than解麦克斯韦方程

**Component Simulation Strategy:**

**Materials**: semiconductor, metals, nonlinear, anisotropic

**Geometry**: size, symmetry, invariance, index contrast

**Physical effects**: thermal, mechanical, EM, carrier transport

**Desired response**: frequency/time domain

Depending on these considerations to determine solver type

Component (physical model, accurate&slow) –> Circuit (functional model, approximate&fast)

Describe component behavior by a compact model

## Linear components, S-parameters, waveguide ports:

Passive – linear, can be mostly simulated into frequency domain by S-parameters,

Solve for each frequency independently

Ports of S-matrix are orthogonal states, physically separated fields, every mode in the waveguide (TE/TM separated), but only use the relevant modes

## Difference between active and passive components:

Passive components described by S-matrix, solved for/described by each frequency separately;

Active components: S-matrix is no longer relevant,

time-domain modelling, special frequency models (fast modulators, nonlinear phenomena,…)

Exception: slow-varying circuits (thermal-tuning phase shifters)

## Reciprocity:

Most linear photonic components are **Reciprocal**: S\_{xy} = S\_{yx}

The scattering coefficient is equal for the same ports for two directions

Nonreciprocal – optical isolators, circulators;

Only possible with magneto-optics materials in magnetic field (linear);

Nonlinearities (amplitude-related), Time-varying systems (SAW,…)

Fine-tuning parameters would result in what effect?

## Understand the basic concepts and difference of different Maxwell solvers:

General Purpose: **FDTD**, **Finite Elements**

Specific/Approximate: when certain requirements are met

**Raytracing**, **Beam Propagation**, **Eigenmode Expansion**, **Boundary Integral Equations**,

**Plane-Wave Expansion**

**RayTracing** – rarely used in PIC (on the scale of wavelength)

Shooting rays through the structure and follow path, uses high-frequency approximation

Pro: simple, accurate for large devices (not diffracting)

Con: too much approximation, not suited for on-chip waveguides

Can be used to **acquire far-field profile**

**FDTD**: generic, maxwell equation, differentiator->difference

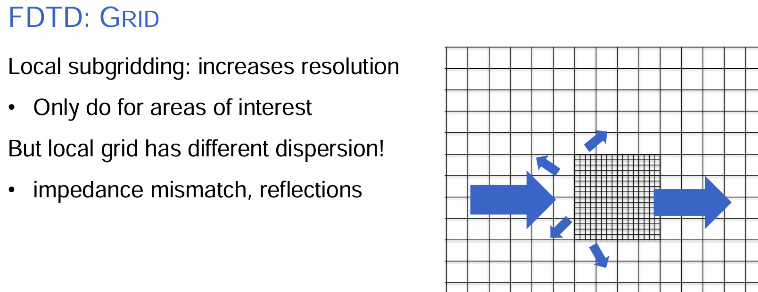
Discretization: E and H field components are not in the same position, uses interpolation to acquire field at a position

Update the field by leapfrogging (time-stepping)

**Scaling**: **more accurate with smaller cells**, energy shouldn’t traverse more than 1 cell a step

comes larger simulation time(立方) and memory(四次方)

cube geometry – introduces anisotropy (leapfrogging updating introduces a new dispersion relation, and make propagation direction-dependent, hence anisotropic)



to minimize anisotropy in areas of interest: add subgrid inside, but numerical dispersion varies between them- introduce artifacts

**impedance mismatch/reflections**

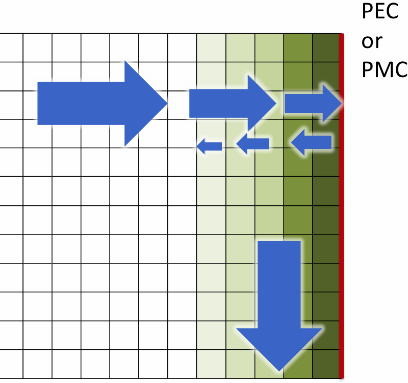
Boundaries of overall volume: PEC/PMC/PML

**PEC**: Tangential E set to 0

**PMC**: Tangential H set to 0, numerically efficient but them both reflect/ bounce back

But can be quite efficient if certain that light stay bounded (waveguide modes)

However, if radiation mode exists, takes reflection into account in PEC/PMC -> PML

**Perfectly Matched Layers (PML)**

Create layered stack of material on top of PEC/PMC with matched impedance

Gradually changing layers – **unphysical anisotropy**:

Absorbs perpendicular incidence

Guides parallel waves

Sources: Hard/Soft sources

Hard sources: set E-/H-field (like a dipole) – acts as a **scatterer** as the reflected waves hit it

Soft sources: **induce a field/using current** – transparent to reflected waves

**Convert to Frequency domain**: Fourier Transforms

H = output/input, short pulse – wide spectrum

Response to excitations takes the form of modal profiles, varies for different frequency components inside the pulse (waveguide modes are frequency dependent) - Mismatch between modal profiles of different frequencies

– applies 1550nm mode profile for calculation induces error for 1500&1600nm mode calculation – S-parameter extraction only correct for the frequency selected for mode profile

for correct response, 1 simulation correct for 1 frequency; narrowband excitation.

Need to perform simulations at different frequency to verify the frequency distortion of FDTD

Brute-force, computationally inefficient – optimized for parallelization, run on massive clusters – material setting are specialized

**Finite elements:**

**Discretization of Maxwell; Non uniform meshes (triangle/tetrahedrons)**

**Vertices: Scalar potential; Edges: Vectorial potential – current: vertex integration**

**Robust to rounding error (variational method), 无法并行计算，要解高维稀疏矩阵**

Optimize locally with fine meshes – easier to discretize curved geometries

Open boundary by nature – introduce PML boundary

2 most common, generic methods – specific structure

**Plane-wave expansions:** describe the field as superposition of plane waves, calculate coupling between waves by scatterers (scatter and couple)

Solving for eigenvalues (band diagrams) or excitation-driven, easy far-field calculations

Plane waves are eigenmode for free space, discontinuities are hard to express

**Pro:** simple base set, standard fourier transform

**Con:** many waves needed, difficult to describe **discontinuities (waveguides不连续边界)**

**Eigenmode expansion:** to deal with discontinuities description

Discretize structure into parts transversally invariant, and describe the field as series of eigenmodes in that section (lower degree of freedom/number to express the field);

at interfaces, **coupling matrix** needs to be calculated (**difficulty!-find all eigenmodes!**)

– acceptable for real materials,

suitable for components with **large area with same cross-sections**, propagate instantaneous

Gradual changes in cross-section – chop into sections, inefficient simulations (mode overlap)

Speed-up for **periodic structures (gratings)**

**Advantage: no need to solve all the fields if only S-matrix is needed**

**Not suitable for structures with a lot of variation in cross-section profile**

**Beam propagation**: discretization of paraxial wave equations (propagate in one direction)

extended with reflections, wide angles

**Pro: fast, large devices, includes radiation**

**Con:** perturbation theory - **low index contrast (not for silicon photonics)**

**Boundary Integrals: Rayleigh-Sommerfeld,**

fields can be determined by boundary conditions, no need to go through volume

easy for transmission through uniform areas (star-coupler, AWG, echelle gratings)

Combining Techniques: AWG

Input star-coupler – array of delay lines (simple waveguides) – output star-coupler;

Star-coupler:

* Input aperture(taper+MMI) : eigenmode expansion/FDTD
* Free propagation region: Fresnel diffraction model/Boundary integral
* Output aperture

Stitch together at the interfaces

S-parameter extraction from this stitching together –> input to output matching

## S-parameter extraction:

Frequency-domain simulation: one wavelength a time, easy to extract dispersion and mode overlaps, very accurate at single frequency

Time-domain simulation: inject a pulse and calculate pulse-response, get all frequency at the same time

but modal spatial profile is frequency-dependent (modal dispersion), mode-overlap varies for different wavelength; hard to acquire overlaps, only correct for center wavelength

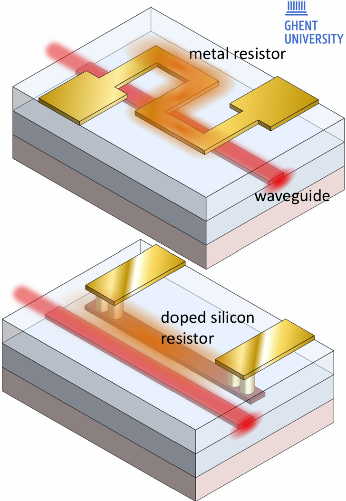
S-parameter extraction (using FDTD): what is the process? (defining geometry, waveguide ports, modal overlaps,…)

Defining geometry and waveguide ports,

inject a narrow band pulse (with corresponding eigenmode) into a port,

and check the output waveform of each port (including reflection) after iterations,

use the eigenmode profile of output port at that center frequency of injected pulse to calculate overlap efficiency

fourier transform the output waveform into frequency domain and compute transform function as S-matrix

Multiphysics: Thermal phase-shifter simulation

Electrical: driving (ns)

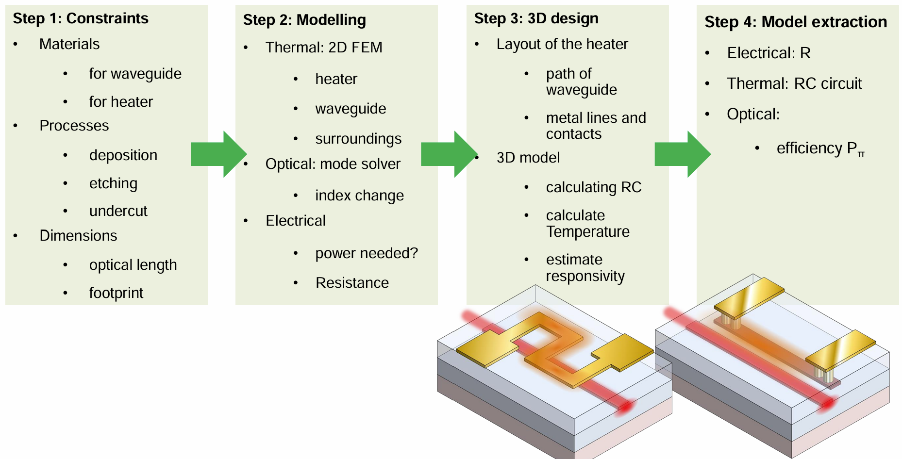
Thermal: heat transport (ms)

Optical: waveguide propagation (fs)

**Working principle:**

**Joule Heating** (Electrical current through a resistor, ns)

* **Heat Transport** (changes waveguide temperature, us-ms)
* **Mode solver** (affects , hence optical mode, fs)



对三个问题同时建模-

What platform?

What material for heater?

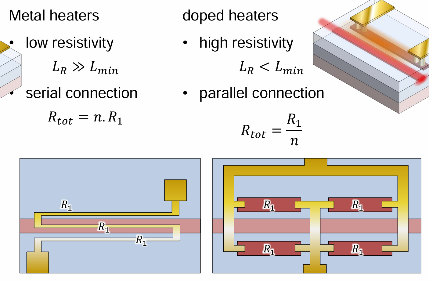
Optimize thermo-optics also minimize thermal leakage

Model thermal problem as RC circuit:

3D design – undercut insulation

Thermal modelling: 2D cross-section

Finite Elements – refractive index profile – - Heater efficiency

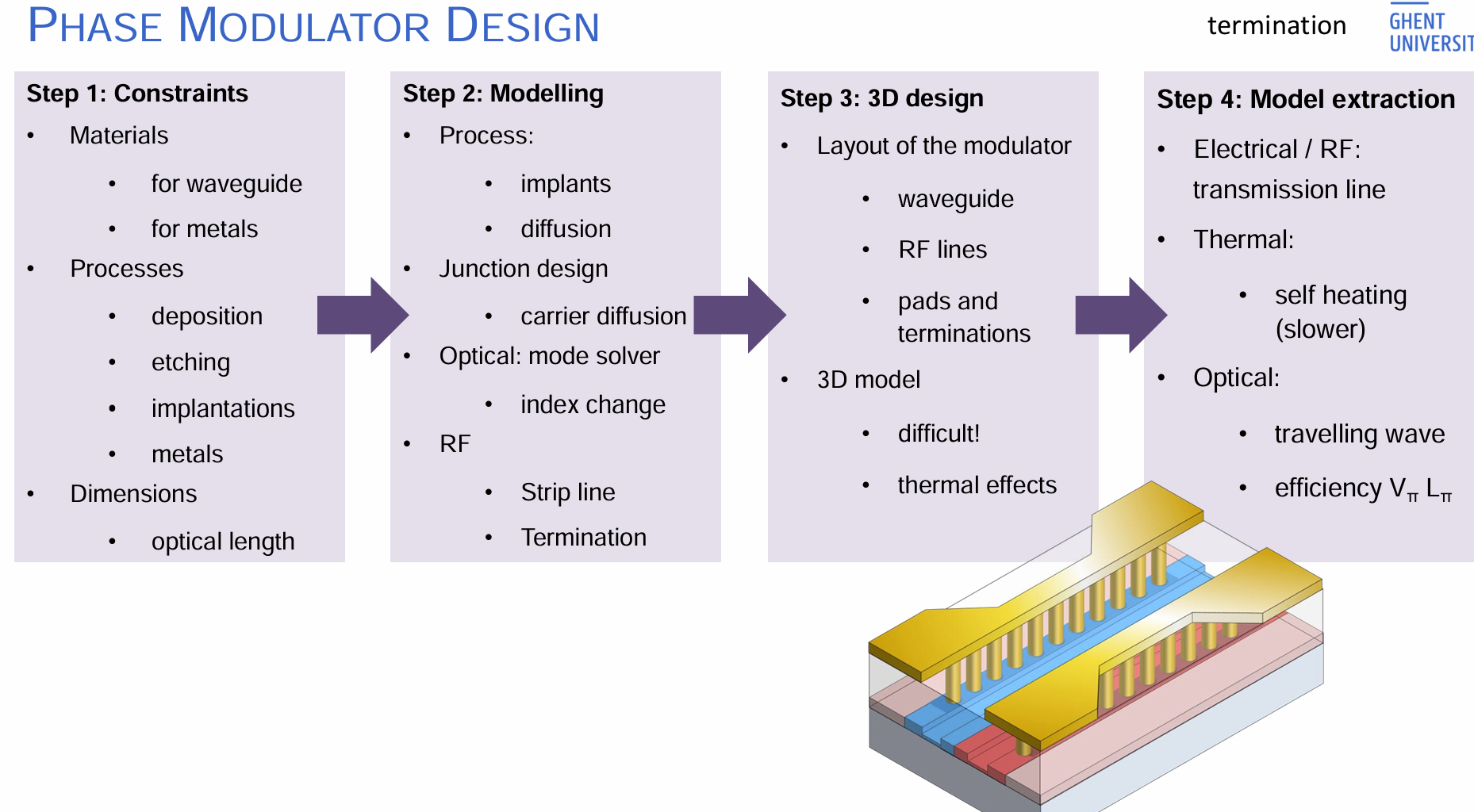


Electrical modelling: phase-shift – needed power

– with right resistance and resistor length under constraint

(zigzag works for low resistivity;

parallel for high resistivity)



Pn junction or pin junction selection:

- large overlap with waveguide mode; maximum change of carrier density;

- minimize optical absorption/capacitance

Process simulation of junction – ion implantation/annealing profile

Put into electrical simulator – carrier transport capability/recombination/space charge distribution (carrier profile -> refractive index profile)

Optical solver – from refractive index profile interpolated

Design rf line – simulate microwave modes (finite mode); design propagation constant

Choosing which simulator to use for a problem (+motivation) check the quiz

More efficient solvers for the specific scenario, motivation as well

# Circuit Simulation

Go to functional simulation, one level of abstraction up, build circuit model

Handover of a circuit model from physical simulation to circuit designers – model extraction

Correct mapping between input and output, in frequency and time domain,

Efficient for circuit simulation, has meaningful parameters that can be extracted from measurements

Describe as scatter matrices

## The difference between white-box and black-box models

White-box: knows the circuit, captures the physics (via equations)

Black-box: unknown internals, mathematical ‘fit’ or a machine learning model

Waveguide: -hard to measure, low order MZI

## The difference between scattering wave and effort-flow:

Electrical: nets with a voltage potential, current flowing through terms (Effort-Flow)

Optical: ports and links with a travelling wave, solve with wave scattering formalism

Effort-flow more suitable for RF systems, not suitable for photonics systems, mapping between duo (voltage and current) is not a perfect match for duo (E, H), neglects the vectorial nature of both field components;

## The difference between Waveguide Ports and Electrical Terms

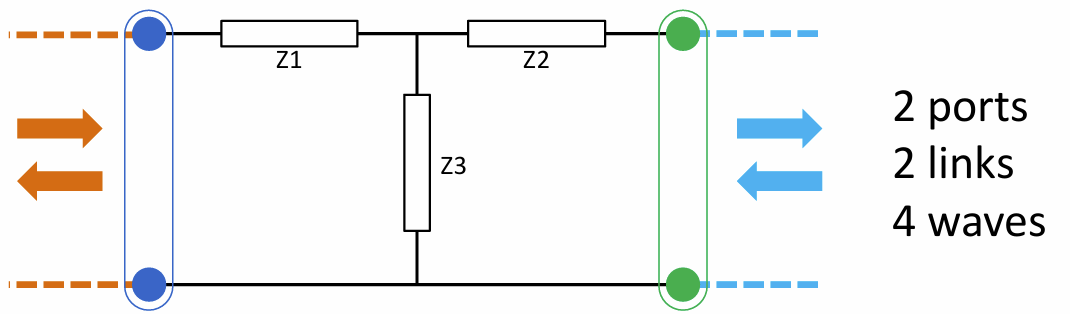
Terms (terminal): **single contact point** for an electrical wire, currents flowing through

Net: all locations connected at the same electrical potential

Ports: interface for propagating waves, needs **2 terms**, voltage and current over

Link: zero-length transmission line over which a wave propagates (bidirectional)

Characteristic impedance: Z = V/I



## The correspondence between transmission line and waveguides

Wave reflection caused by impedance mismatch – Fresnel’s Reflection

Impedance – refractive index^-1

Approximation requires modal overlap calculations (into multiple guided modes and radiated mode) and losses (scattering and reflection)

Same model for optical circuits simulation as electrical circuits – Modified nodal analysis

Using nets and Terms; Effort-Flow systems

## Optical signals (power, phase, modes, wavelengths)

Optical links carrying the signal:

two directions:各需要一个表征;

complex number (power & phase);

WDM->multiple carrier wavelength (channel): N channels;

mode/polarization: M modes

2\*2\*N\*M

## Different time-domain modelling schemes (ODE)

Scatter matrix: generalized reflection of a wave, Coupling between all ‘ports’(mode)

Time domain: not directly coupled

1, directly coupling, no delay – true for wavelength-independent device (large)

instantaneous response b\_i(t)=s\_{ij} \* a\_j(t), wrong time-step, takes steps to evolve

analytical signal modulated on w0, b\_i(t)=s\_{ij}(w0) \* a\_j(t)

approximation: time signal has a bandwidth around w0

2. for linear circuits – frequency-dependent S-parameter: S\_ji(w), integrate over whole band

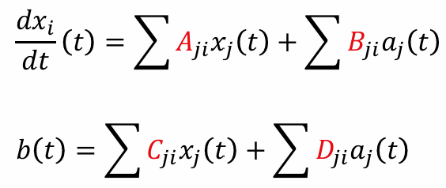
FT, a\_j(t) -> A\_j(w); B\_i(w)=S\_{ji}(w)\*A\_j(w); IFT, b\_i(t) <- B\_i(w)

Erroneous for circuits with loops (feedbacks), input depends on output,

no available FT for input, only works for sequential circuit

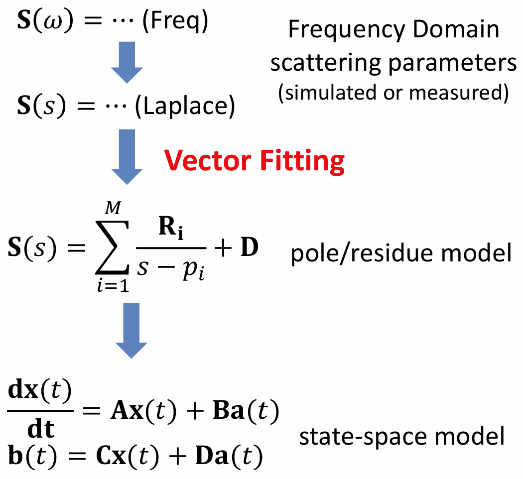
1. For linear circuits, add delay (memory) to time domain circuits,

Add finite number of delays (finite impulse), approximating a dispersive – computation intensive;

Add derivatives, allows basic control, but not useful when applied alone, but no real memory in the device;

* Add states into system: State-space model: internal states + PDE coupling, ABCD矩阵 - ODE

Incoming signals **a(t)** with states **x(t)**

– time evolution of states **dx(t)/dt**

– states **a(t)** with outgoing signals **b(t)**

Vector Fitting – fitting of S-parameters, 射频仿真

convert poles and residues to ABCD model (ODE)

really high frequency(超短步长，超长仿真时间，宽带)

-change to baseband(载波的幅度，相位，有限带宽)

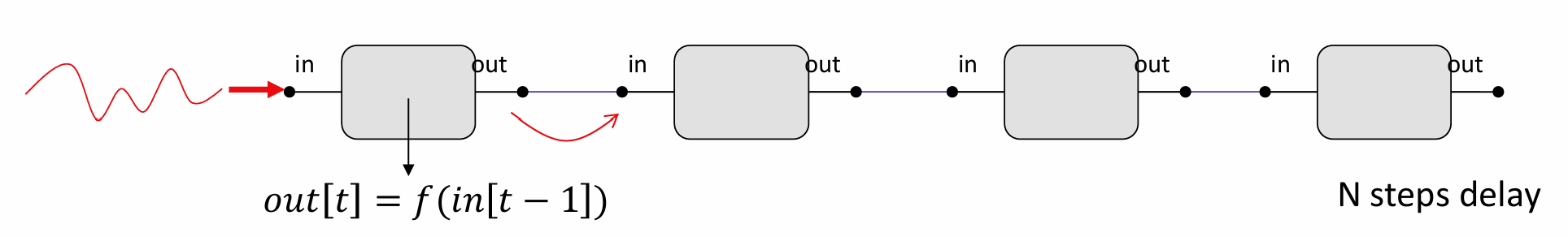
Complex envelope representation

Complex Vector Fitting (只fit正频率，移回基带)

Extract state-space model from this new transfer function, less poles – less simulation time

## Effect of the time step in time-domain circuit simulations:

Now the updating rules and input sources are defined, to iterate in time domain;



Define time steps (with sufficient accuracy):

Passing thru elements takes at least 1 time step;

Integration of differential equations is more accurate with smaller steps (更长仿真时间)

– express optical signal with prescribed number of parameters, could explode

## Options for Photonic-electronic co-simulations

Electrical: effort-flow/SPICE; Optical: Scattering waves/port.

Simulate in SPICE: treat photonics as electronics (effort-flow, use Verilog to describe)

Limited in scalability, compatible with current design flow

Simulate in Photonics simulator: custom models for photonic circuits

less mature for electronics, no verified fab models for electronics

Co-simulate with waveform exchange:

Photonics and electronics in optimized model, executed sequentially

Use output of 1 simulation as input of next simulation

Only works for unidirectional circuits, without feedback loops

Need co-simulator:

runs both simulator in parallel and exchange data at each step

## How to do abstractions, model delay, why domain transition is hard (incorporate delay)

# Wavelength Filters

## Basic operational principle of a wavelength filter:

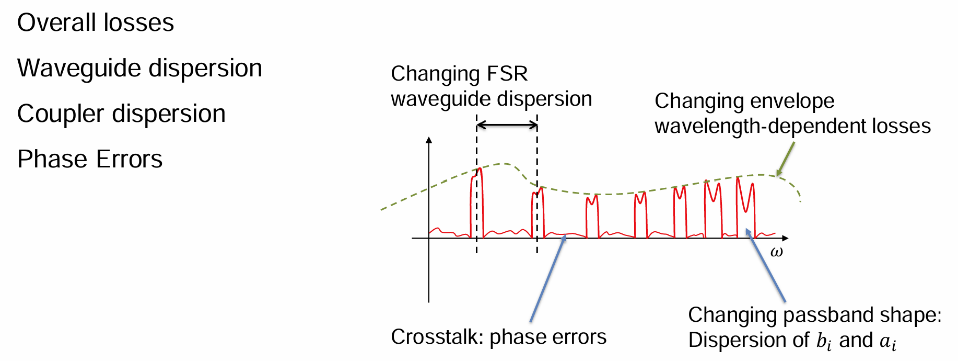
Split into multiple delay lines,

Different delay between lines

Combine together to form interference pattern

create wavelength-dependence phase shift

## Performance metrics of a filter (insertion loss, ER,…)

Insertion loss

Extinction ratio

Rolloff:

Ripple (intraband & out-of band)

FWHM:

Crosstalk：

FSR Free Spectral Range:

## Difference between FIR and IIR filters

IIR: feedback, has non-zero pole; FIR: feed forward, poles are all 0

## Basic concept of an MZI lattice filter

FSR = c/ (n\_g \* \Delta\_L)

In time domain: impulse response – exponential (delta function with different shift) – FIR

Fourier Transform – dirac pulse trains modulated by envelope (FT of uniform pulse train gives pulse trains)

Periodic trains – Laplace Transform (s=j\omega) / z-transform (z=\exp^{s\Delta t}) – polynomials (delay lines with periodic increments)

## All-pass and add-drop Ring resonators: linewidth, Q-factor, Finesse, critical coupling, decay time,…

## Basic concept of AWG and Echelle grating:

## Effect of imaging and overlap in an AWG/Echelle

## How to make a flat-top transmission in an AWG

## Different parameters of an AWG and how to choose them

## Effect of phase errors in Lattice filters and AWGs

Ring resonator

Q-factor go down if coupling goes up, formulae know by heart

AWG, echelle

# Programmable Photonics

## How does a 2\*2 photonic gate work? Implementations

## Forward-only meshes and linear transformation and matrix multiplication

## Recirculating meshes: how to implement filtering

## Layers in the technology stack

## Effect of parasitics

# Design for Manufacturability

High index contrast – compact geometry, sensitive to fabrication errors

CMOS technology is only option with sufficient nm-process control for SiPh

Within wafer uniformity: thickness

## Basic semiconductor manufacturing process,

* Photolithography

1. Spin-coat + pre-bake (uniform baking)
2. Exposure (exposure dosage)
3. Post-exposure bake (reduce standing-wave effect, ripple caused by interference of light; amplify chemical reactions (deprotection/crosslinking), improving pattern formation) + Development

* Etching (Full etch & Partial Etch)

1. Plasma etching the exposed silicon (pattern density)
2. Strip away the remaining resist

Better litho + etch -> loss and line width better controlled – affects – peak resonance shifts

* Doping (Modulators and heaters) (ion implantation)
* Deposition (uniform)
* Planarization (CMP bow of wafer)
* Epitaxial Growth (Ge, CMP)
* Damascene Process (For electrical contacts, dioxide - tungsten)

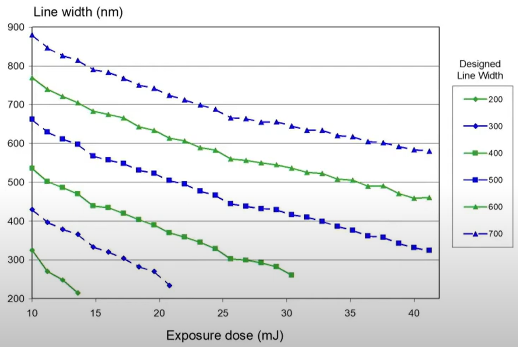
More metal layers: deposit dielectrics - litho. and etch tracks – fill with Cu – CMP

Metal Bondpads: Deposit dielectric layers – Deposit AlCu – Litho. and Etch pads

SiPh chips: passive ckts with multiple etch layers – modulators and photodetectors – metal wiring

## How these steps introduce variabilities (different contributions)

Sources of variation:

* Reticle/Mask
* Critical dimension uniformity
* Flatness
* Transmission (glass transparency)
* Litho. Tool
* Exposure dose
* Slit uniformity
* Chuck (substrate holder) flatness
* Focus stability
* Scan direction
* Source spectrum
* Resist process
* BARC (bottom AR coating) uniformity
* Resist uniformity (viscosity in the process of spincoat)
* PEB (post-exposure bake, amplify chemical reaction (deprotection/crosslinking)/) temperature uniformity
* Developer (surface tension of developing solvent)
* Metrology (?)
* Wafer
* Wafer flatness/bow
* Stack uniformity
* Topography
* Etch process
* Plasma chemistry
* Coil power stability (RIE)
* Bias stability
* Resist coverage
* Metrology
* Deposition
* Doping
* Planarization

**Bring these variations effect into design process**

Predict at design stage the effect of these process conditions brings, adjust the design to minimize these effect, three steps are taken:

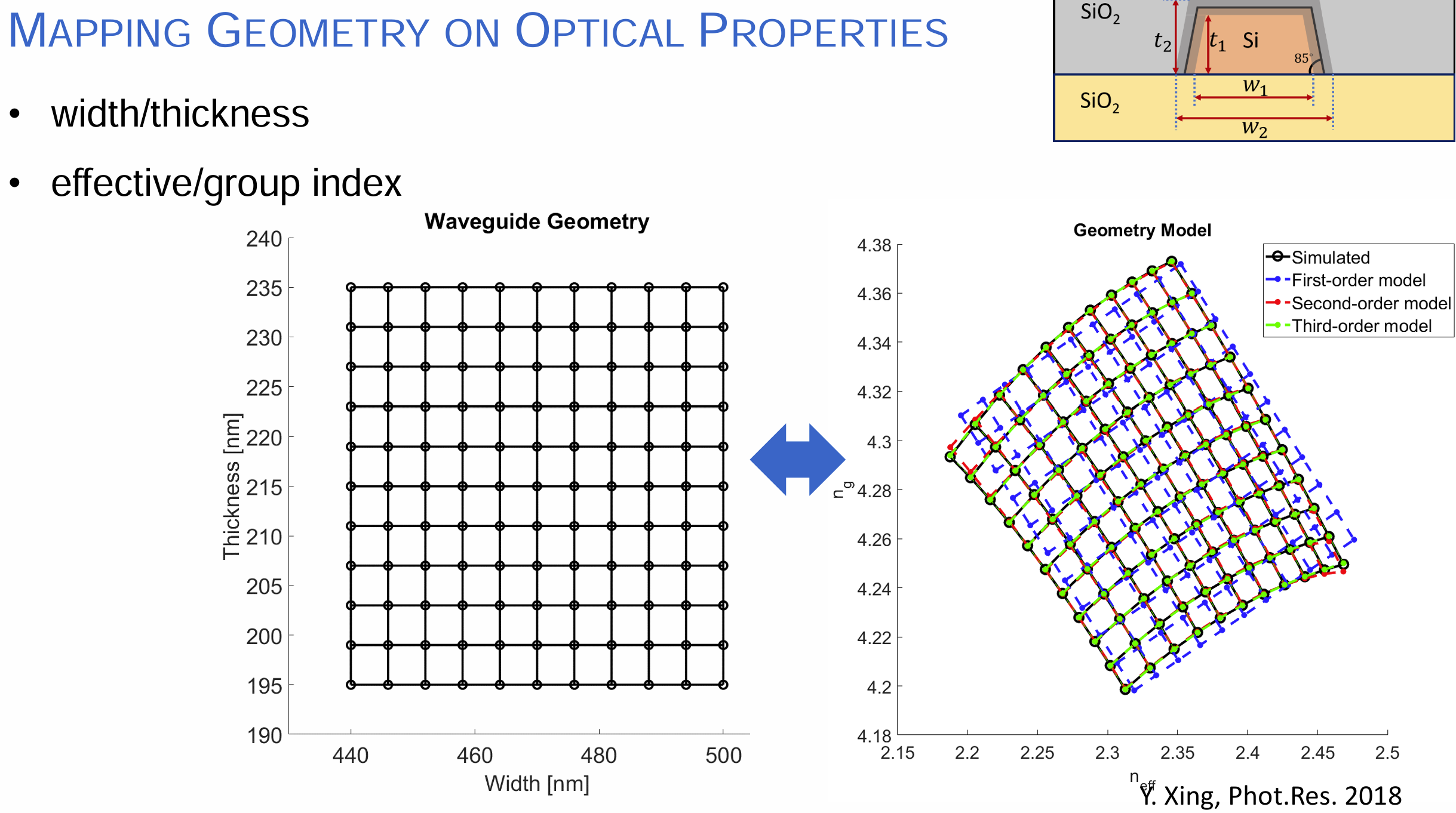
* Detailed parameter extraction
* Spatial Variation Model (translate into a parametrized model estimating the variations)
* Layout-Aware Yield Prediction (apply the model to predict)

**Detailed parameter extraction: direct measurements are raw, not collected directly**

**measure optically:**

model relation between **device geometry (linewidth, layer thickness)**

and **optical device properties () (mapping geometry on optical properties)**

****

**extract optically (using interference pattern, peaks&FSR)**

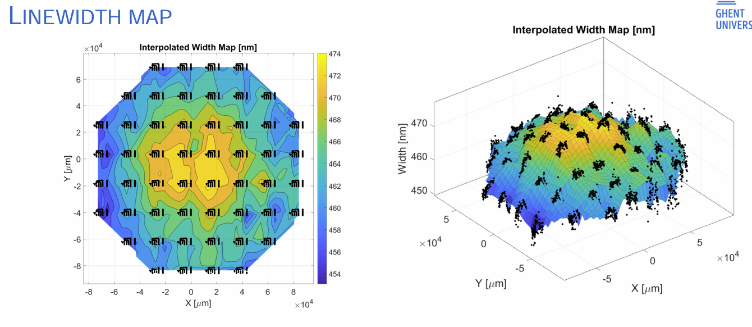
: low order MZI, (m known)

: high order MZI,

2 devices to characterize the 2 parameters- single device quantifying this, **place across the mask** to measure the variability of both parameters across the wafer

Use the mapping between geometry and optical properties to acquire the corresponding thickness and linewidth

Histogram of thickness and height (more variation (statistical spread) in width than height) – translate the extracted data into spatial variation model



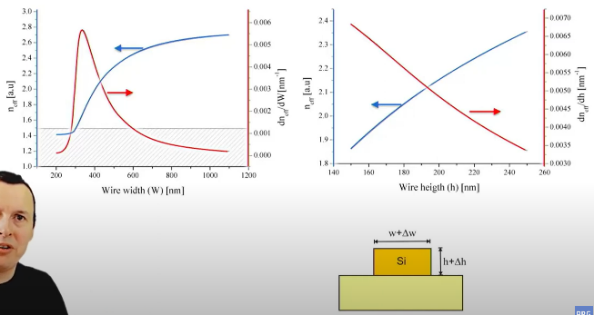
Etch&CMP has radial non-uniformity (plasms cloud), planarizing surface has certain bow, inducing dome shape profile

Translate the histogram into a model

**spatial variation model:**

extract the parameters measured into a model capturing different contribution of this statistical variation (histogram) – first, need to identify the origin (variability on different scales)

## Effect of variability in the geometry of silicon waveguides



Absolute linewidth control

(dimensional dependence of waveguide)

Blue: function of width and height

Red: sensitivity function of width and height

Changes the performance of wavelength filters in shifting operation/resonance wavelength

Directional couplers are affected by changing coupling ratio

Losses are dominated by scattering (Sidewall roughness), different litho.+etch - loss

## Effect of pattern density on variability

Adding dummies (little squares) to control pattern density, to maintain uniform pattern density across the entire mask, plasma etch affected by the pattern density can be maintained uniform here

In star coupler’s free propagation region, unpatterned region shows large perturbation (strong correlation) due to lack of dummy structure.

## Different levels of variability (process conditions -> circuit functionality)

Describing Variability at different levels (gradually translating over levels)

1. Process Conditions

* Exposure dose
* Resist age
* Plasma density
* Slurry composition (CMP)

1. Device Geometry

* Line width
* Layer thickness
* Sidewall angle
* Doping profile

1. Optical Device Properties

* Effective index
* Group index
* Coupling coefficients
* Center wavelength

1. Circuit Properties (combining multiple devices)

* Optical delay
* Path imbalance
* Tuning curve

1. System Performance

* Insertion loss
* Crosstalk
* Noise figure
* Power consumption

## Different scales of variability (local, die, wafer, lot)

Better lithography resolution ( illumination wavelength) gives better uniformity between devices (in a chip)

Within wafer: photoresist and silicon wire linewidth varies as well.

die (single chip, circuits/devices on different location)

-> intra wafer (chip replicated multiple times on a wafer, alignment variability, die-to-die)

-> wafer-to-wafer (in a lot, a group of wafers processed together as a single unit through the manufacturing line under same conditions)

-> lot-to-lot (fabricate over time)

these levels contribute in different way to overall variabilities, need to capture these

**intra-wafer (chip-to-chip, die-to-die):**

exposure dose; layer thickness and bow;

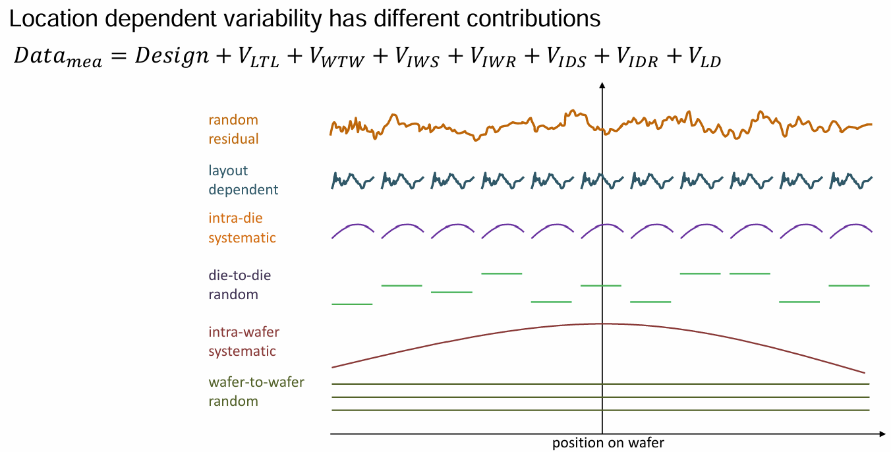
plasma density; CMP pattern; Photoresist spinning (uniformity)

**wafer-to-wafer (within a lot):** requires long-term monitoring

tool priming (effect of previous wafer); layer thickness; non-uniformity in the chamber

**lot-to-lot:** tool drift; resist aging, shelf time; wafer supply

**Positional variability on a wafer**



Intra-wafer: dome profile

Die-to-die: random offset

…

**Intra wafer:** dome profile (bow),

polishing of substrate wafer - affects layer thickness (taper)

plasma density during etching – affects linewidth and etch depth

**Residue: Die-to-die random,7nm**

What remains after subtracting intra-wafer dome

**Intra-die variation:**

* **Systematic: same for every die on the wafer, mask layout, lithography orign…**
* **Low frequency change in layer thickness**
* **Local pattern density (dummies added to maintain uniformity, FPR)**

**Star Coupler-correlate filter ‘radius’ with linewidth variation**

**Extremely high ~50-200nm, etch chemistry (residue products), CMP effects**

* **Error in photomask**

Subtracting Intra-die systematic, then intra-die random remains

* **Random**
* **Intrinsic randomness in layer thickness**
* **Roughness in sidewalls**

**Generate Models from these extracted statistics, from process conditions, device geometries, optical device properties (resonance), then predict yield in ‘system performance’ part:**

**Corner analysis:** normal/worst/best case scenario, used a lot in electronics, not necessarily good/bad case scenario

**Monte-Carlo analysis:** assign random parameters in circuit, run many circuit simulations

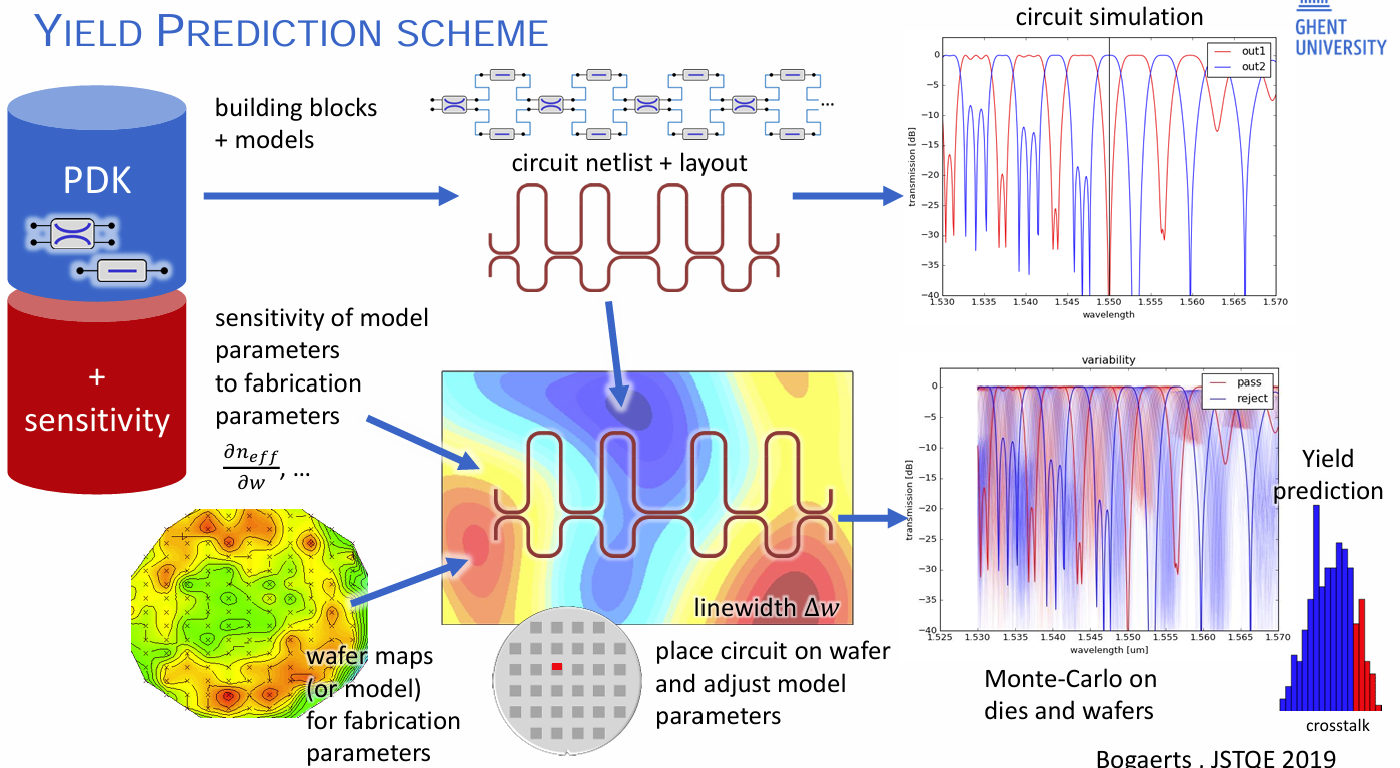
assign a Gaussian, however, parameters are not random, and computation expensive

**Variational methods (Polynomial chaos):** add statistical moments inside the circuirt, simulate the ‘extended circuit’ (not random distribution)

**Take actual layout (virtual wafer) into account**

## The need for statistical process monitoring

Yield prediction requires 3 components: detailed parameter extraction (of process), spatial variation model (translate parameters extracted into a model estimating the potential variations), layout-aware yield prediction (simulate the effect the variation have on performance)



Normal design flow: building blocks from pdk – circuit schematics – simulations

+ model of sensitivity (mapping width variation to , thickness variation to coupling)

+ wafer maps (fabrication parameters/variations, how much is changed)

🡪Project to actual maps of linewidth and thickness (statistics of intra-wafer, intra-die,…)

Place ckt on different positions of wafer for functional simulation (transmission spectrum)

🡪Analyze each and every curve, calculate the yield over the whole wafer

# Random variations versus deterministic/correlated variations 37:23

## Parasitic reflections in waveguides and circuits

## Methods to reduce parasitic reflections

## Methods to reduce circuit sensitivity.

how it translates into yield, how to model and predict the result,

change in photo resist – linewidth – effective index - function

variability in process flow not fully translated (not fully common practice) into yield prediction and functionality

Parasitics, back reflection, unwanted coupling

Improve circuit designs

# After Fabrication

## Understand measurement process

## How measurements can affect variability

Measurement process introduces variability as well. Sampling curve has resolution as well

Difficult of measuring phase

Id of the field, frame name, coupler ports

Angle, position of fiber (penalty of power loss), fit the upper contour of grating couplers, by a polynomial plotted in dB (4th order, dispersion also symmetry)

Fairly uniform grating coupler performance – jupyter notebook

Extract n\_{eff}: m is uncertain, fabrication and other factor introduces variability

Measurement procedure and grating coupler

Orders of peak tradeoff

Compact model: performance evaluation, variability

# Applications

## Basic knowledge of different application fields

## Communications: principles of WDM, coherent communication

Laser+modulator (indirect modulation)

Utilizing full bandwidth without direct electrical modulation/detection schemes – WDM modulate on wavelength fibers

Spatial modulation multiple waveguide/fiber core, multiple modes

IQ modulator

## Sensing: different mechanisms (index, spectroscopy)

Fingerprint of molecules, scanning range of tunable lasers, pre-diffract, post-diffract

## Principle of OCT, LDV, LiDAR

Optical Coherence Tomography:

Take broad band light with weak coherence or laser with spectrometer, depends on scanning range of laser

Measure depth profile of distributed reflection

Depth profile of material under the surface (diffused, scattering) retina-only touch with light

Laser Doppler Vibrometry:

Shoot a laser beam, moving-doppler shift, beating with original beam and gives oscillation pattern, blood pulse velocity,

measure pulses in carotid artery (shock ver)

Light Detection And Ranging: optical beamforming

Grating coupler – optical antenna, emits light in free space

Multiple- optical phased array, tune the phase can steer the beam angle to different angles, 1D array – 1 steering dimension; 2D – 2 steering dimensions

Close spacing - wide steering range,

Steer with different wavelength to tune in different dimensions (fast and slow steering with different delay lines)

Application – LiDAR

Laser communication between satellites (free-space communications) no absorption, only scattering

## Microwave filtering

Project microwave signal into optical domain and process in optical domain (filtering, equalizing, wavelength conversion, ) , transmitting over fiber

## Economics of wafer scale processing and generic chips

Very large scale (integration) of CMOS – SiPh must make use of CMOS-technology, instead of dedicated fab

Repeatable steps - CMOS

Larger wafer, higher volumes, massive parallelism, minimal marginal cost (450mm, largest)

Sweet spot: 330mm wafer

More expensive processing tools (robotics), higher volume, larger fixed costs

New fab

Develop dedicated process flow;

Fabrication run (25 wafers)

Fabrication run (shared, MPW)

Chip (high volume) very chip

This functionality/cost makes sense:

Large volume (millions of chips, high yield, low cost); High complexity (thousands of functions on a chip, large-scale integration, high cost)

Linear mathematics for information processing (matrix factor multiplication)

Quantum information processing are linear