DW8051 IP

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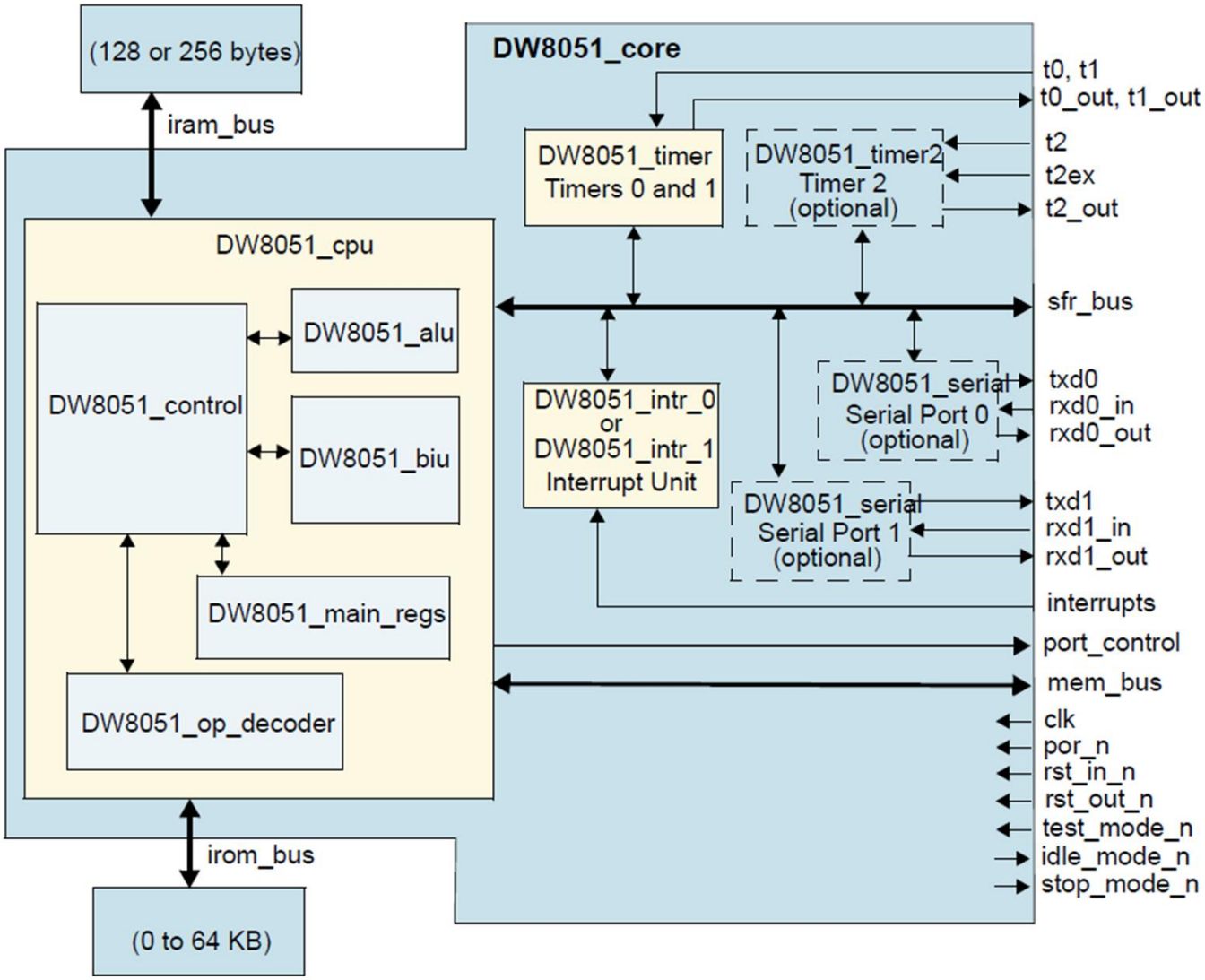
Block Diagram

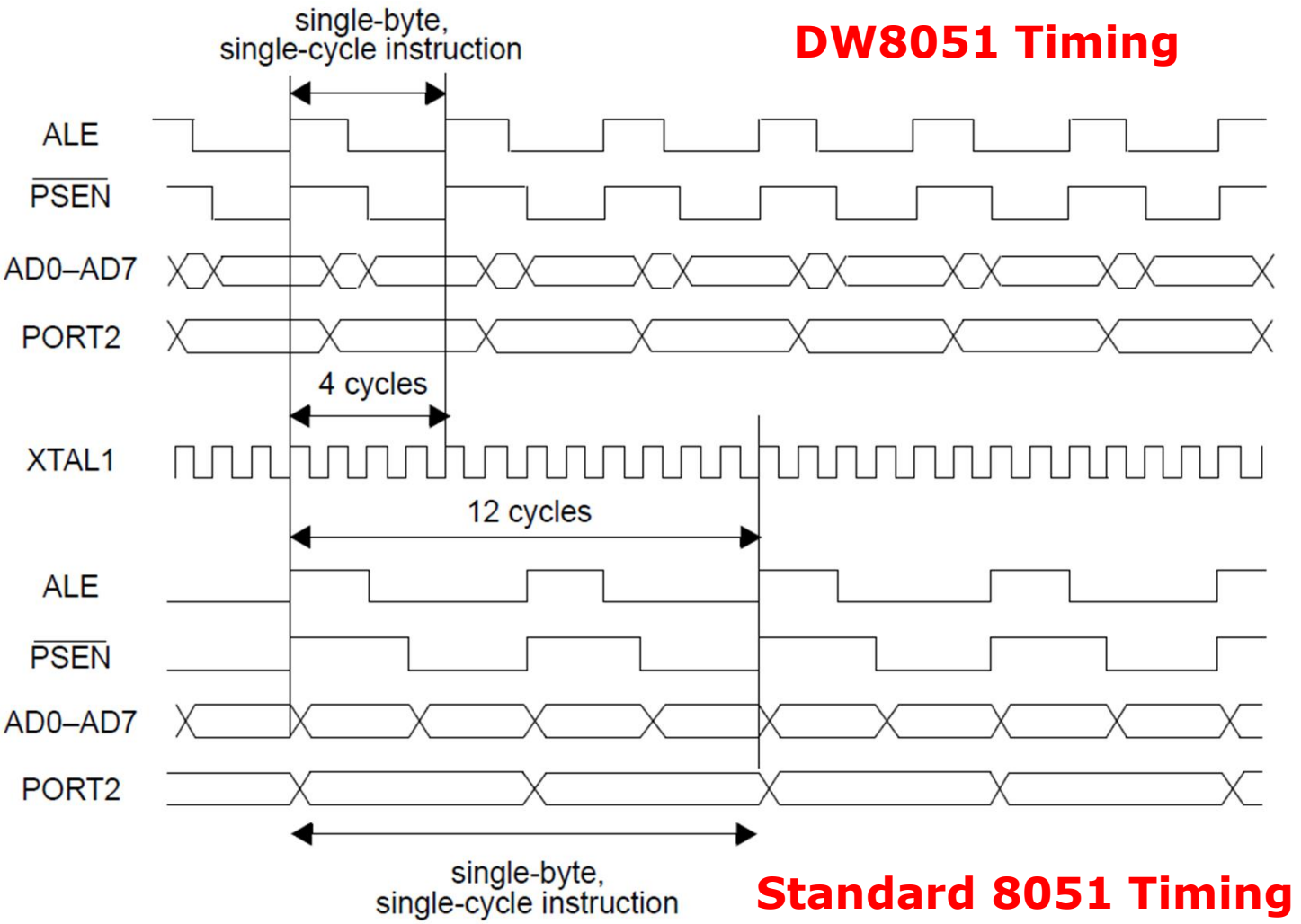


Feature summary

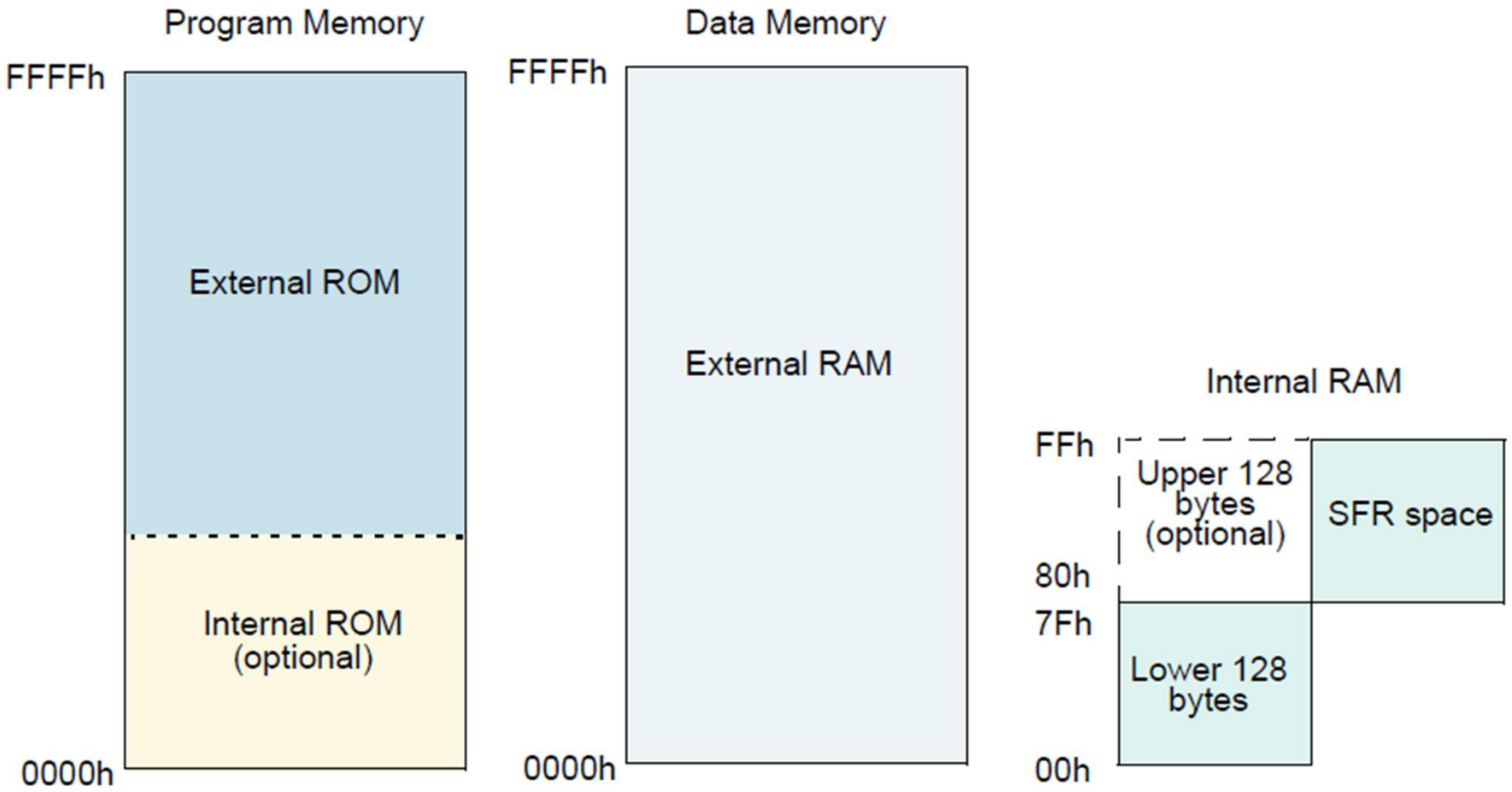
Feature	Intel				Dallas DS80C320	DesignWare DW8051
	8031	8051	80C32	80C52		
Clocks Per Instruction Cycle	12	12	12	12	4	4
Internal ROM (1)	—	4KB	—	8KB	—	Up to 64KB
Internal RAM (1)	128 bytes	128 bytes	256 bytes	256 bytes	256 bytes	128 bytes or 256 bytes
Data Pointers	1	1	1	1	2	2
Serial Ports	1	1	1	1	2	0,1, or 2
16-bit Timers	2	2	3	3	3	2 or 3
Interrupt Sources (total of int. and ext.)	5	5	6	6	13	6 or 13
Stretch Memory Cycle	No	No	No	No	Yes	Yes

(1) Internal ROM and RAM are located outside of DW8051_core.

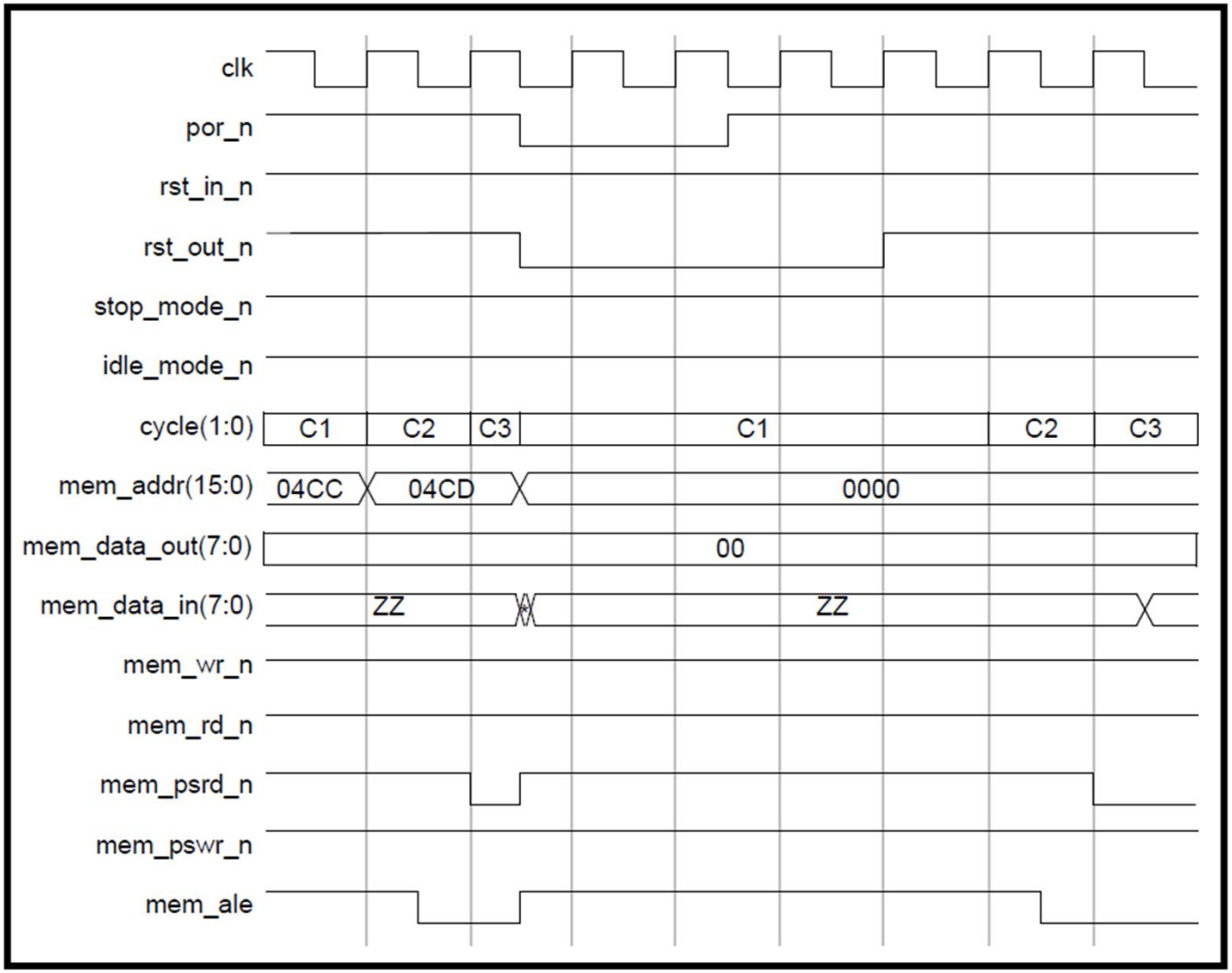
Instruction cycle timing



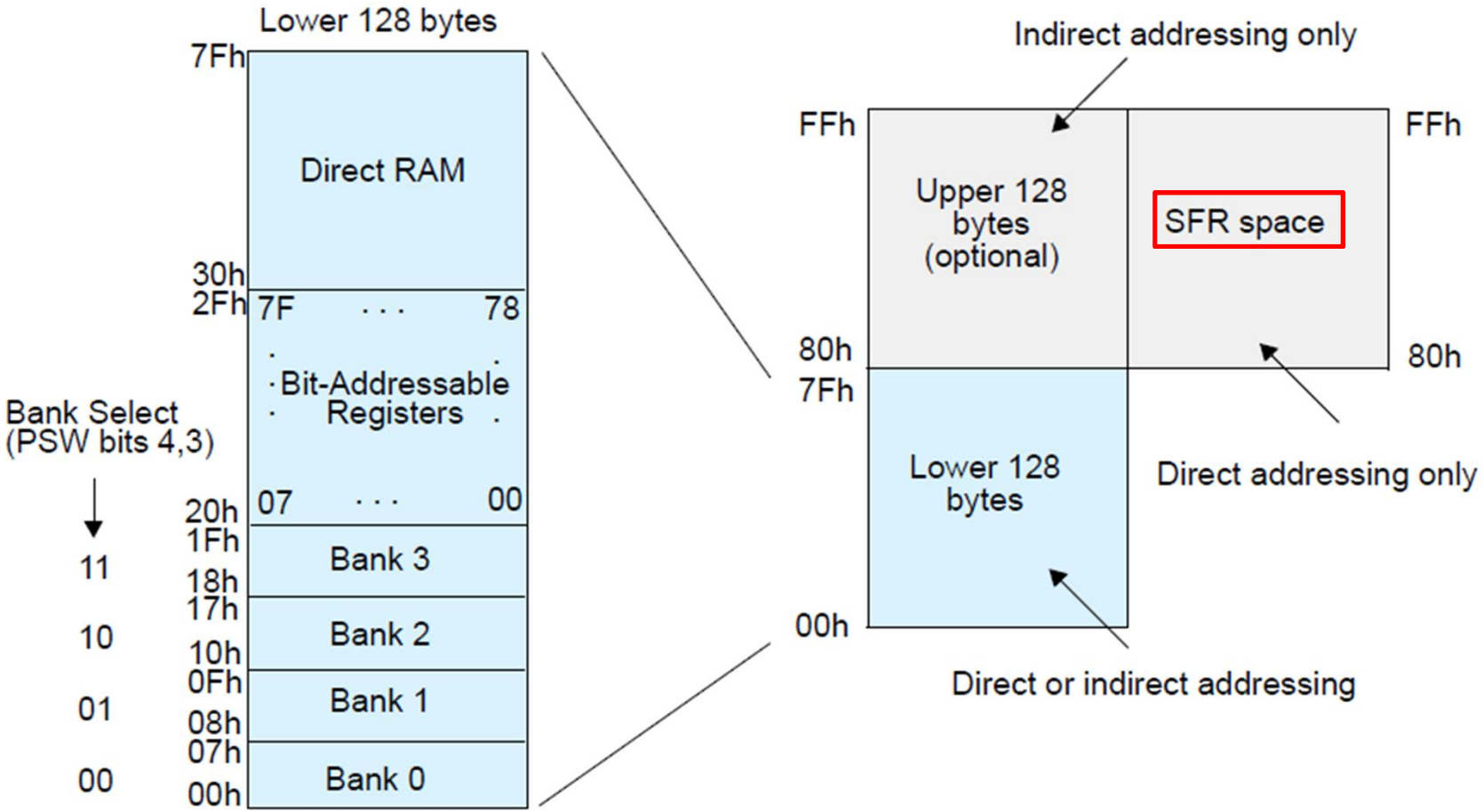
Memory Map


Program Memory
FFFFh
External ROM
Internal ROM
(optional)
0000h
Data Memory
FFFFh
External RAM
0000h
Internal RAM
FFh
Upper 128
bytes
(optional)
SFR space
80h
7Fh
Lower 128
bytes
00h

Timing of por_n Reset



Internal RAM Organization

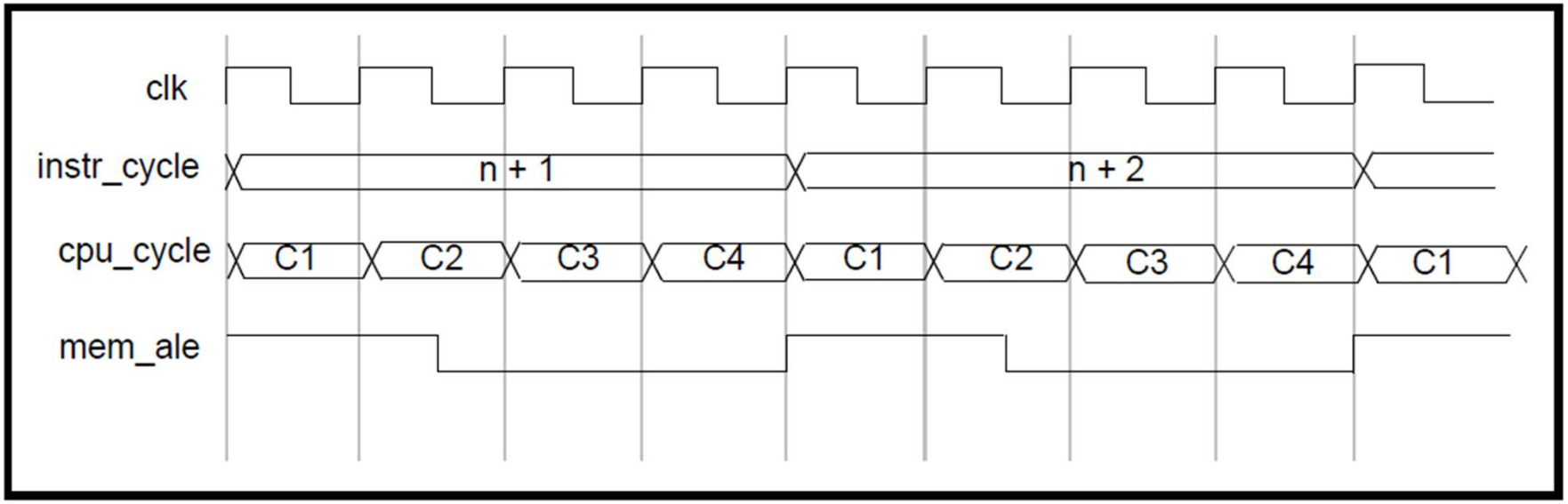


DW8051 Instruction Set

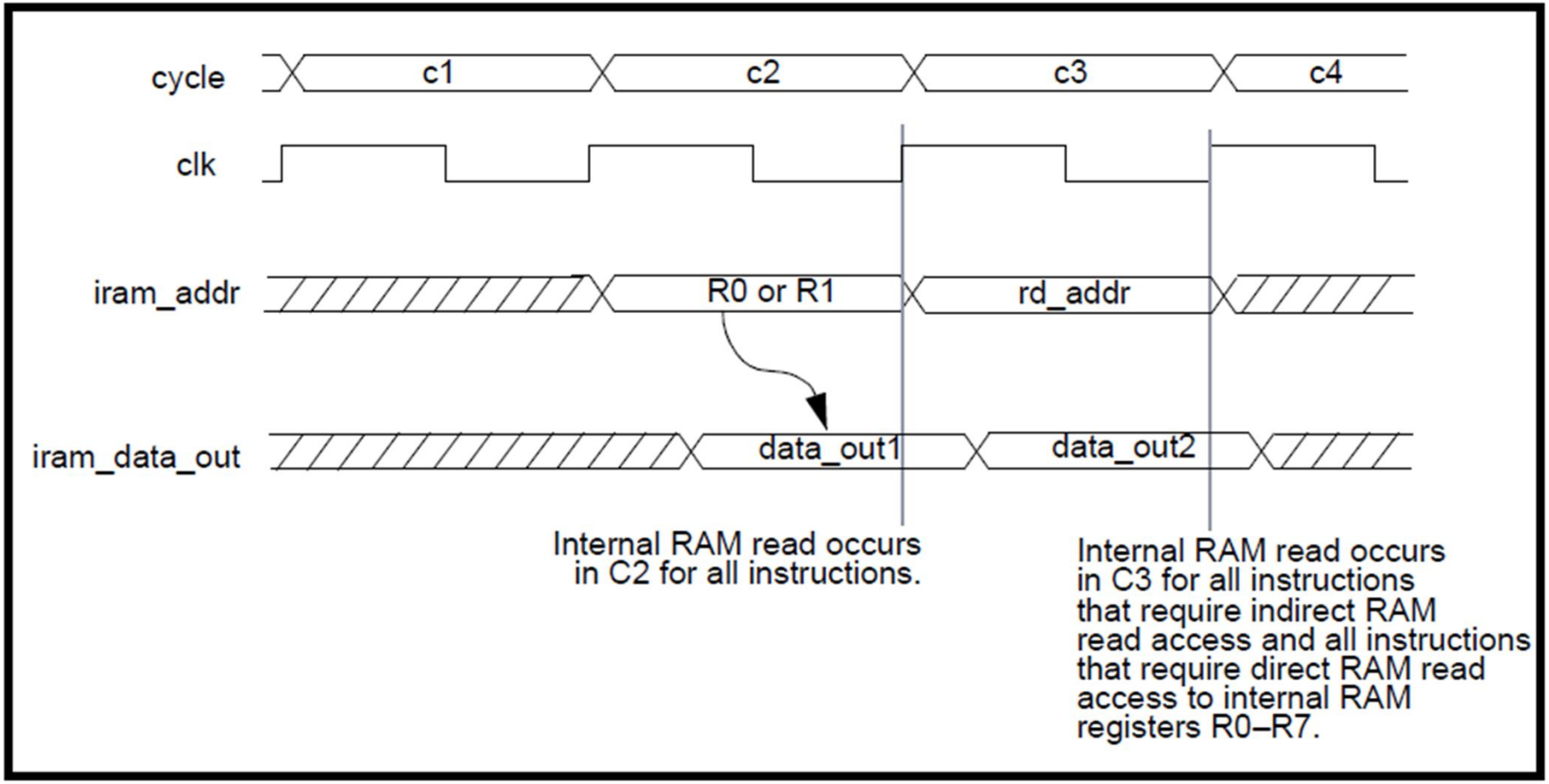
Mnemonic	Description	Byte	Instr. Cycles	Hex Code
Arithmetic				
ADD A, Rn	Add register to A	1	1	28–2F
ADD A, direct	Add direct byte to A	2	2	25
ADD A, @Ri	Add data memory to A	1	1	26–27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	1	38–3F
ADDC A, direct	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add data memory to A with carry	1	1	36–37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	1	98–9F

There is an additional reserved opcode (A5) that performs the same function as NOP.

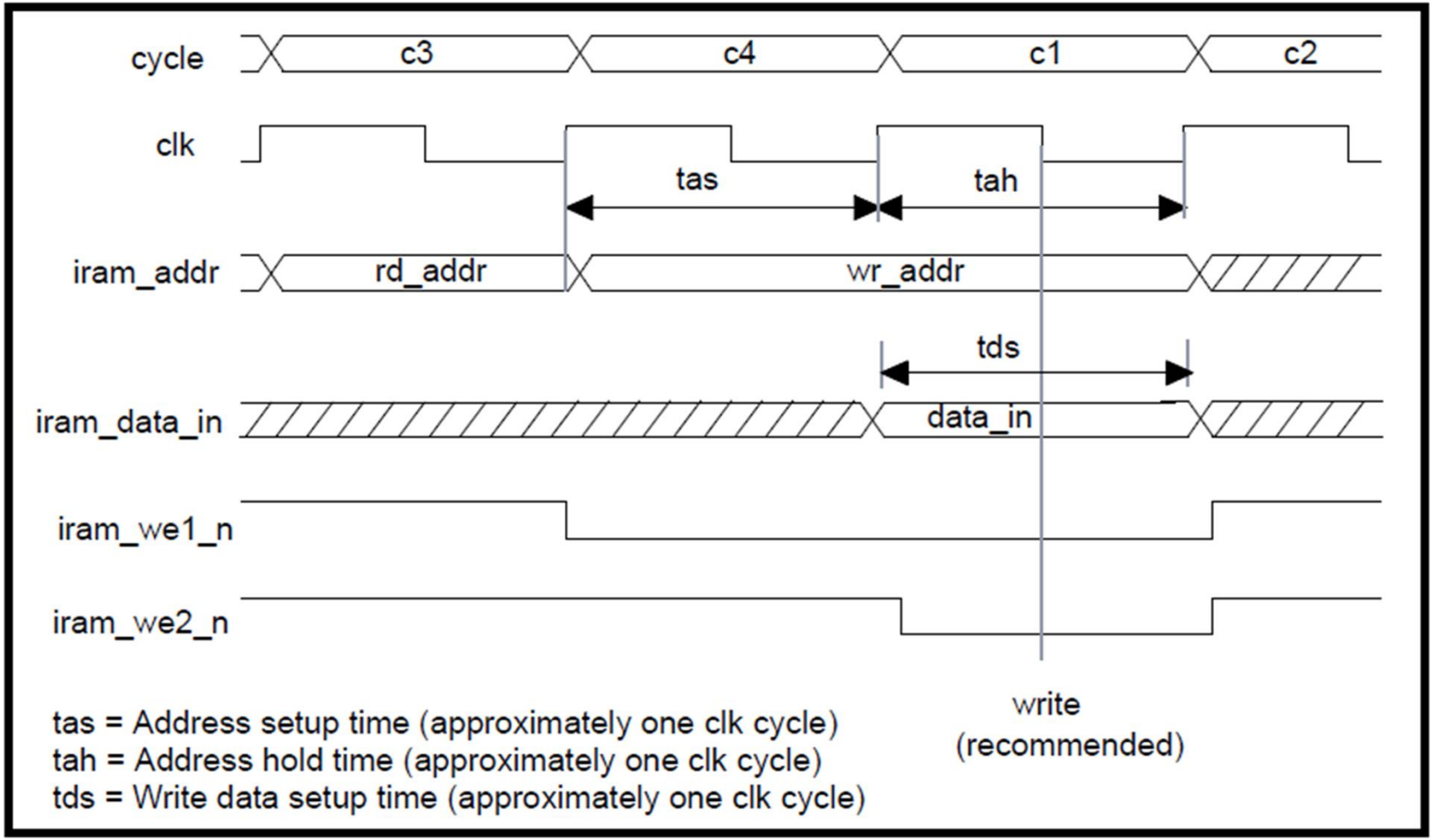
CPU Timing for Single-Cycle Instruction



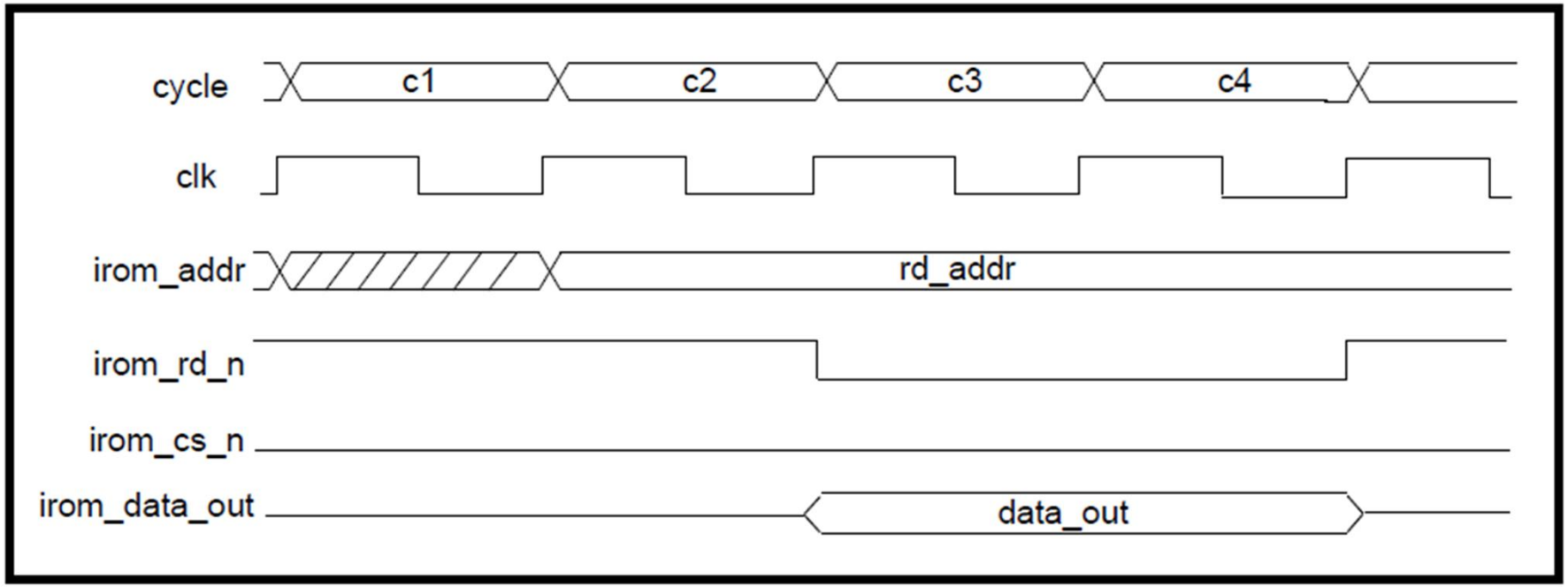
Internal RAM Read Signals and Timing



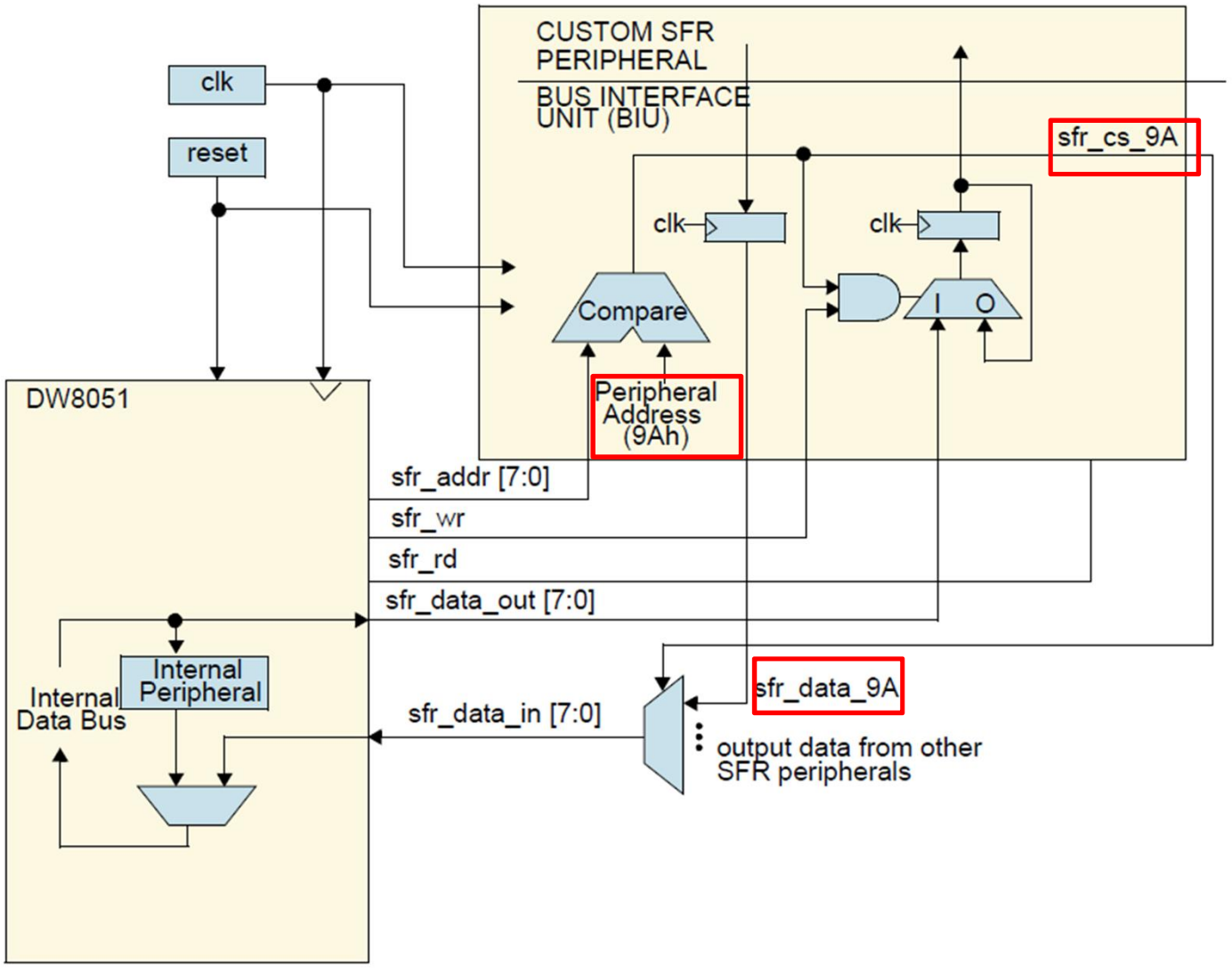
Internal RAM Write Signals and Timing



Internal ROM Interface Timing



SFR Peripheral Interfacing

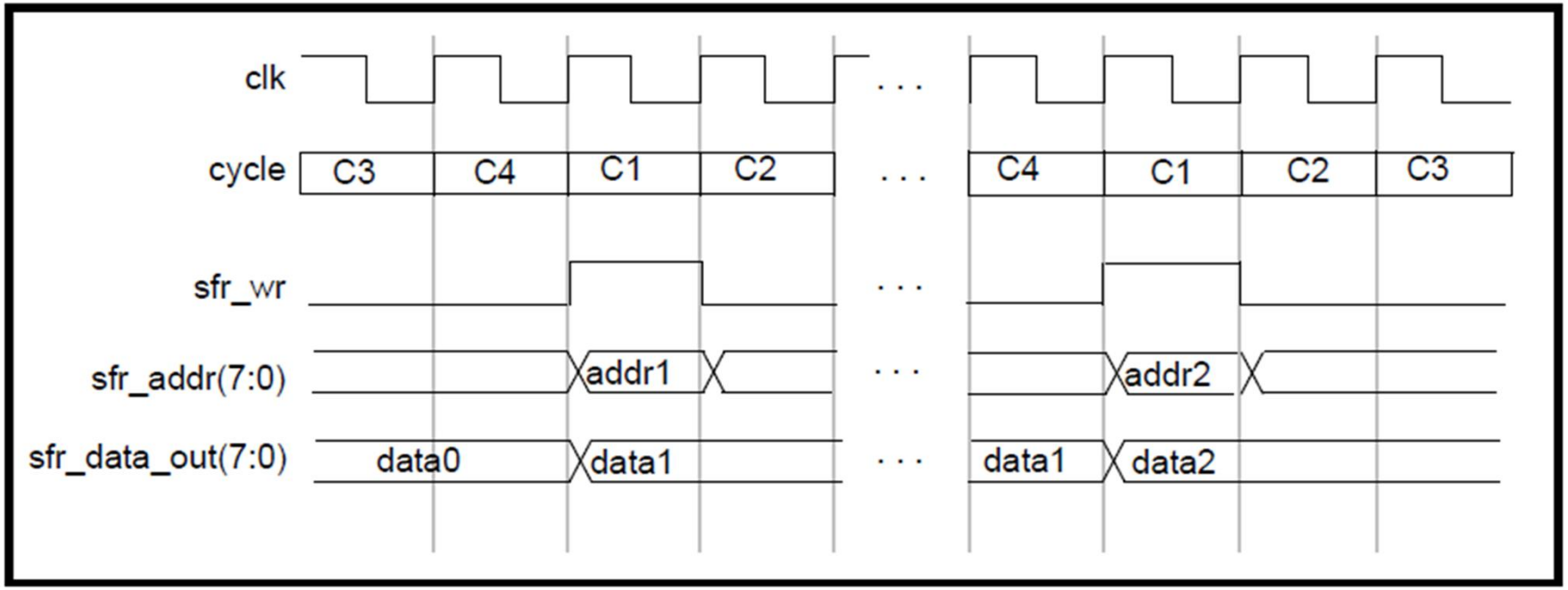


Unused SFR Addresses

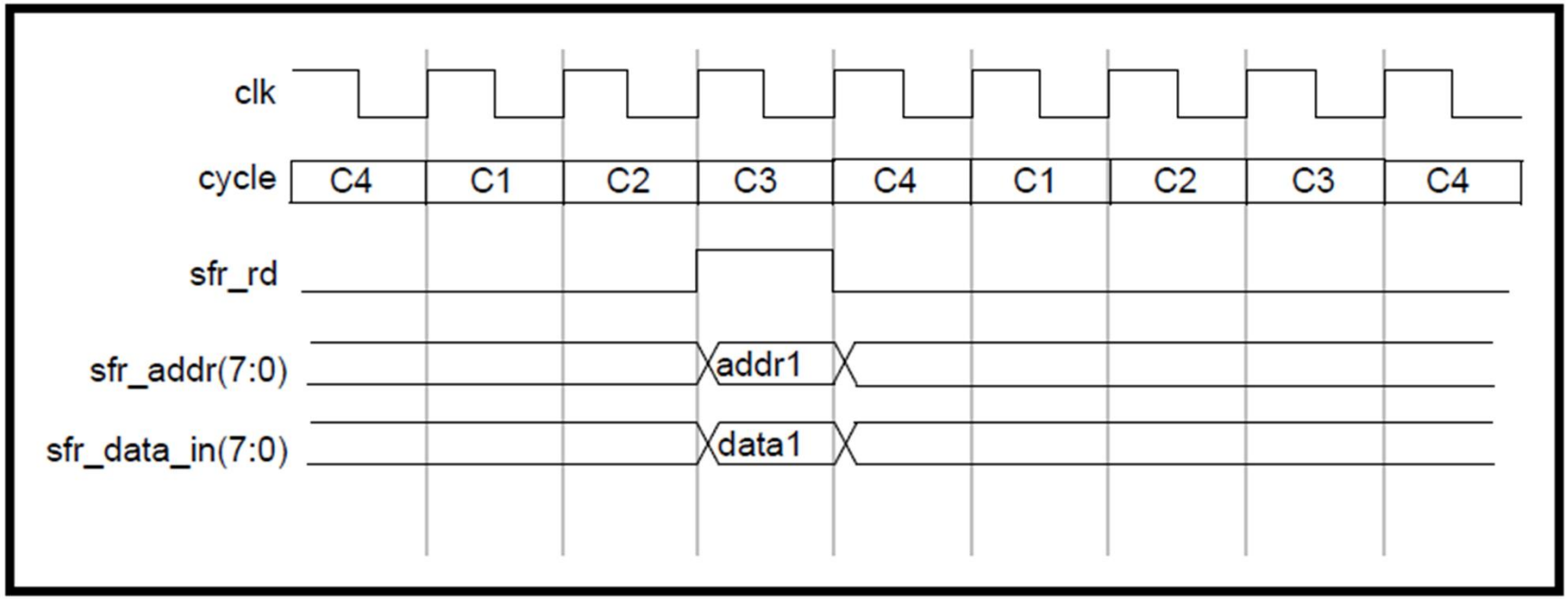
80h(1)	90h(1)	93h–97h	9Ah–9Fh	A0h(1)–A7h
A9h–AFh	B0h(1)–B7h	B9h–BFh	C2h–C7h	C9h
CEh	CFh	D1h–D7h	D9h	DAh–DFh
E1h–E7h	E9h	EAh–EFh	F1h–F7h	F9h–FFh

(1) Addresses 80h, 90h, A0h, and B0h are only available if you are not using the associated standard 8051 port module (P0, P1, P2, or P3).

SFR Bus Write Timing



SFR Bus Read Timing



DW8051_core to Standard Port Module Connections