POST-LAB

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One of the main challenges is to understand what is in the constraints file.
For this lab (Basys3_Master.xdc), other than pin / button / LED definitions, the only thing defined is the clock (10ns period & 5ns pulse width).

Things learned from this lab:

1) How to generate bitstreams for burning setup into real-world FPGAs
2) Helped to revise knowledge regarding timing analysis (e.g., checking worst negative slack & the datapath, etc.)