1. **Radiation Effects on Electronics and Materials:**

Effects on Electronics and Materials

Radiation doesn't just affect living things; it can wreak havoc on technology, especially in space or near nuclear reactors.

Effect Type	Description	Result
Total Ionizing Dose (TID)	Gradual accumulation of radiation over time.	Slow degradation; electronics eventually "wear out" and fail.
Displacement Damage	Particles physically knock atoms out of their crystal lattice.	Changes the electrical properties of semiconductors (like solar cells).
Single Event Effects (SEE)	A single high-energy particle strikes a sensitive spot.	"Bit flips" (changing a 0 to a 1 in a computer's memory) or permanent hardware burnout.

2. **Space radiation environment**

The space radiation environment is a complex, high-energy field that is significantly more intense and diverse than the radiation we experience on Earth. While our planet's atmosphere and magnetic field act as a "shield," space itself is filled with three primary types of ionizing radiation that pose a threat to both human biology and advanced electronics:

A. Galactic Cosmic Rays (GCRs)

Source: From outside our solar system (likely supernova explosions).

Composition: Highly energetic nuclei of atoms that have had their electrons stripped away. Mostly protons (85%) and helium nuclei (12%), but also include "Heavy Ions" (HZE) like Iron.

Nature: A constant, steady "background" flux. Because they travel at nearly the speed of light and are extremely heavy, they are almost impossible to block with current shielding technology.

B. Solar Particle Events (SPEs)

- **Source:** Our own Sun, specifically during solar flares and Coronal Mass Ejections (CMEs).

Composition: Primarily medium-energy protons.

Nature: Episodic and unpredictable. These are "storms" that can last for several days. While dangerous, they are lower in energy than GCRs, meaning lead or water shielding can effectively protect astronauts from them.

C. Trapped Radiation (Van Allen Belts)

- **Source:** Particles from the Sun and GCRs that get "caught" by Earth’s magnetic field.
- **Composition:** Protons (inner belt) and Electrons (outer belt).
- **Nature:** Concentrated donut-shaped regions around Earth. Spacecraft in Low Earth Orbit (LEO) mostly avoid these, but missions going to the Moon or Mars must pass through them.

---Effects:

Spacecraft Electronics

Modern microchips are so small that a single radiation particle can physically change a "0" to a "1" in a computer's memory.

- **Single Event Upsets (SEUs):** Temporary glitches or "bit flips" in software.

Total Ionizing Dose (TID): The gradual "wear and tear" that eventually kills a satellite's circuits.

Latch-up: A permanent short circuit caused by a particle that can destroy a chip instantly.

OMERE software

(Outil de Modélisation de l’Environnement Radiatif Externe) is a leading industrial software tool used to calculate the space radiation environment and its effects on electronic devices.

Goals: It allows engineers to predict how much radiation a satellite will encounter based on its specific orbit and how that radiation will impact its hardware.

1. Core Capabilities

OMERE acts as a bridge between complex physics models and practical engineering. It is divided into two main functional areas:

A. Environment Modeling

OMERE calculates the "flux" (the number of particles hitting a surface over time) for different types of radiation:

- **Trapped Particles:** Protons and electrons caught in the Van Allen belts (using models like AP8, AE8, and the newer AE9/AP9).
- **Solar Particles:** High-energy protons and ions from solar flares.
- **Galactic Cosmic Rays (GCR):** High-energy nuclei from outside our solar system.

B. Radiation Effects Analysis

Once the environment is defined, the software estimates the physical toll on the spacecraft:

- **Total Ionizing Dose (TID):** Calculates the cumulative energy absorbed by electronics, often represented as a "dose-depth curve."
- **Single Event Effects (SEE):** Predicts the rate of "bit flips" (upsets) or destructive latch-ups caused by individual heavy ions or protons.
- **Displacement Damage (TNID):** Estimates long-term structural damage to semiconductors and solar cells.
- **Solar Cell Degradation:** Specifically predicts how a satellite’s power output will drop over the mission's life.

2. Key Features for Engineers

- **Orbit Propagation:** Users can input orbital parameters (apogee, perigee, inclination) or import a specific trajectory file to see the exact environment the satellite will pass through.
- **Component Database:** It allows engineers to input "cross-section" data—essentially a profile of how sensitive a specific chip is to radiation—to calculate exact error rates for that mission.
- **Industry Standard Models:** It integrates international models (like CREME86 for cosmic rays) and ONERA models (like IGE-2006 for electrons).
- **Multi-Mission Analysis:** Engineers can run "batch mode" to compare different mission scenarios or shield thicknesses simultaneously.

3. How it Fits into Spacecraft Design

OMERE is typically the first step in a "Radiation Analysis" workflow. Engineers use it to determine the "Top-Level" environment. If the radiation levels are too high, they may then use a 3D modeling tool like **FASTRAD** to design specific lead or aluminum shielding for the most sensitive components.

Radiation effects on electronic components

When radiation interacts with electronic components, it doesn't just pass through—it leaves a trail of physical and electrical destruction. In space or nuclear environments, this damage is categorized into three main "modes" based on how the particles interact with the semiconductor material.

1. Total Ionizing Dose (TID)

TID is a cumulative effect. It is like the "sunburn" of a microchip—the damage builds up slowly over the lifetime of the mission until the component eventually fails.

The Mechanism: Ionizing radiation (like gamma rays or protons) creates electron-hole pairs in the insulating layers (usually Silicon Dioxide, SiO_2) of a transistor. While electrons move quickly, "holes" (positive charges) get trapped at the interface.

The Effect:

- **Threshold Voltage Shift:** The trapped positive charge makes it easier to turn on an N-channel transistor (leakage) and harder to turn on a P-channel transistor.
- **Increased Power Consumption:** As transistors become "leaky," the device draws more and more current even when idle.
- **Timing Failures:** The charge buildup slows down the switching speed of the transistors, eventually causing the chip's internal clock to fail.

2. Single Event Effects (SEE)

SEE are "random" strikes caused by a single, high-energy particle (like a heavy ion or proton) hitting a sensitive spot on a chip. Unlike TID, these can happen on day one of a mission.

They are divided into two categories:

A. Non-Destructive (Soft Errors)

- **Single Event Upset (SEU):** A particle strikes a memory cell and flips a bit from a "0" to a "1." This corrupts data but doesn't break the hardware.

Single Event Transient (SET): A temporary voltage spike or "glitch" that travels through a circuit. If it gets "caught" by a clock cycle, it becomes an SEU.

B. Destructive (Hard Errors)

- **Single Event Latch-up (SEL):** The particle triggers a "parasitic" circuit within the chip, creating a short circuit between power and ground. If the power isn't cut immediately, the chip will melt.
- **Single Event Burnout (SEB):** Typically occurs in power transistors. The particle strike triggers a massive current surge that destroys the device instantly.

In semiconductor physics, a **"parasitic" circuit** refers to an unintended and unavoidable electrical structure that exists as a byproduct of the way integrated circuits are manufactured.

While engineers design transistors (like MOSFETs) to perform logic, the overlapping layers of N-type and P-type silicon naturally create "hidden" components—mostly **Bipolar Junction Transistors (BJTs)**—that are usually dormant but can be "woken up" by radiation.

2. The "Latch-up" Feedback Loop

Under normal conditions, these parasitic transistors are "off" and don't affect the circuit. However, **ionizing radiation** (like a heavy ion strike) can inject enough charge to act as a "trigger."

- **The Trigger:** A heavy ion strikes the N-well, creating a burst of current.
- **Turning on Q1:** This current flows through the substrate resistance, creating a voltage drop that turns on the **parasitic PNP transistor**.
- **Turning on Q2:** The PNP then sends current into the base of the **parasitic NPN transistor**, turning it on as well.

Self-Sustaining Loop: Once both are on, they feed each other in a positive feedback loop. They create a "short circuit" directly between the power rail (VDD) and ground (VSS).

The Result: The chip "latches" in a high-current state. It will stay this way even after the radiation is gone. If the power isn't cut immediately, the heat generated by this short circuit will physically melt the silicon, causing permanent **burnout**.

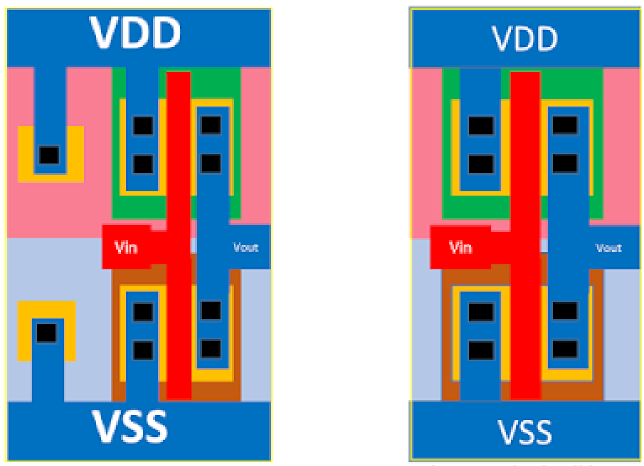
3. Why Radiation Makes it WorseWhile parasitic circuits can be triggered by electrical noise or heat, space radiation is particularly dangerous because:

- **Micro-local Activation:** A single ion can deposit a massive amount of charge in a tiny, specific area (the "gate" of the parasitic SCR), making it much easier to trigger than a general voltage spike on the power line.
- **Unpredictability:** You cannot predict when an ion will hit, meaning a satellite can be perfectly healthy one second and "latched up" the next.
-

How Engineers "Kill" Parasitic Circuits

Since you can't get rid of the silicon layers, engineers use **Radiation Hardening by Design (RHBD)** to make these parasitic circuits harder to trigger:

- **Guard Rings:** Adding extra "drain" regions (highly doped silicon) around transistors to soak up excess charge before it can trigger the parasitic BJTs.
- **Trench Isolation:** Etching deep physical trenches between the N and P regions and filling them with an insulator (like SiO_2) to physically break the parasitic path.
- **SOI (Silicon On Insulator):** Using a layer of glass (insulator) underneath the transistors so the parasitic NPN and PNP structures literally cannot form.



Traditional Standard Cell layout   Tapless Standard Cell layout

Figure-2: Traditional and Tapless standard cell structure

3. Displacement Damage (TNID)

Also called **Total Non-Ionizing Dose**, this is physical, structural damage to the crystal lattice of the semiconductor.

- **The Mechanism:** A heavy particle (like a neutron or high-energy proton) physically slams into a silicon atom and knocks it out of its place in the lattice (creating a "vacancy" and an "interstitial").
- **The Effect:**
- **Reduced Gain:** In bipolar transistors, the defects act as traps for electrons, reducing the efficiency of the signal.
- **Solar Cell Degradation:** This is the primary reason solar panels on satellites lose power over time; the lattice damage prevents electrons from flowing freely.
- **Dark Current:** In camera sensors (CCDs), displacement damage creates "hot pixels" and increased noise in images.

Effect	Type	Source	Primary Impact
TID	Cumulative	Gammas, Electrons, Protons	Leakage current, threshold shifts

SEE	Stochastic (Random)	Heavy Ions, Protons	Bit flips, Latch-up, Burnout
TNID	Cumulative	Neutrons, Protons	Reduced gain, solar cell power loss

In the context of space radiation and electronics, the choice between analyzing **Heavy Ions** versus **Protons** depends on the specific failure mechanism you are trying to predict.

While both are ionizing particles, they damage electronics in fundamentally different ways due to their mass and charge.

1. Heavy Ions: The "Direct" Killers

Heavy ions are nuclei of elements heavier than hydrogen (e.g., Carbon, Iron, Gold). In space, these are often referred to as **HZE particles** (High-Z and High Energy).

- **Mechanism: Direct Ionization.** A single heavy ion carries so much charge that as it passes through a transistor, it leaves a dense "wake" of electron-hole pairs. This track is often enough to flip a bit or blow a fuse instantly.
- **Metric:** Measured by **LET (Linear Energy Transfer)**. This describes how much energy the particle "drops" per unit of distance as it travels through the silicon.
-
- **Primary Effect: Single Event Effects (SEE)**. Heavy ions are the gold standard for testing "worst-case" bit flips (SEUs) and destructive latch-ups (SEL).

Note: The name is an acronym that describes their two most dangerous characteristics:

- **High-Z:** They have a high atomic number (Z>2). This means they are the nuclei of elements heavier than Hydrogen and Helium (such as Carbon, Oxygen, Magnesium, Silicon, and Iron).
- **High-Energy:** They travel at relativistic speeds (nearly the speed of light), giving them immense kinetic energy.

1. Why "Z" Matters (The Square Law)

In radiation physics, the amount of ionization (damage) a particle causes as it passes through a material is proportional to the **square of its charge** (Z2).

Particle	Atomic Number (Z)	Relative Ionizing Power (Z2)
Proton	1	1
Alpha (Helium)	2	4
Carbon	6	36
Iron	26	**676**

As shown above, a single **Iron nucleus** (Fe) causes nearly **700 times** more ionization damage than a single proton. Because they are so highly charged, they strip electrons away from atoms in a very dense, tight column, often described as a "microscopic bullet hole" through a cell or a microchip.

Key HZE Components

The most "famous" HZE particle in space mission planning is **Iron-56**. It is considered the worst-case scenario because it is relatively abundant in cosmic rays and has a very high charge (Z=26).

- **Source:** Supernova explosions outside our solar system.
- **Energy Range:** 100 MeV/nucleon to 10 GeV/nucleon.
- **Prevalence:** Constant background radiation; unlike solar flares, you cannot "wait out" HZE particles.
-

2. Protons: The "Sneaky" Disruptors

Protons are the nuclei of hydrogen atoms. They are the most abundant particles in the space environment (comprising ~85% of cosmic rays and nearly all of solar storms).

- **Mechanism: Indirect Ionization.** Protons are "light" and usually don't have enough charge to cause a bit flip by themselves. Instead, they act like a billiard ball:
  - The proton slams into a Silicon nucleus in the chip.
  - The Silicon nucleus recoils or shatters (spallation).
  - The **recoil fragment** (which is now a "heavy ion") is what actually causes the bit flip.
- **Primary Effect:** * **Total Ionizing Dose (TID):** Because there are so many protons, they are the main contributors to the slow "wear out" of electronics.
  - **Displacement Damage:** Protons are the primary cause of physical lattice defects that degrade solar cells and optical sensors.

Feature	Protons	Heavy Ions
Abundance in Space	Extremely High	Low (but constant)
Damage Type	Cumulative (TID) + Random (SEE)	Mostly Random (SEE)
Ionization Method	Indirect (via nuclear reaction)	Direct (via charge track)
Shielding	Relatively easy (aluminum/water)	Extremely difficult (high energy)
Test Goal	Check for "wear out" and solar storm survival	Check for "bit flip" thresholds

Engineering models & standards

To ensure that a satellite survives for years in the harsh space environment, engineers don't just "guess" the radiation levels. They use strictly regulated **engineering models** to predict the environment and **industry standards** to define how much safety margin must be added to the hardware.

1. Environment Models (The "Blueprints")

These models are mathematical simulations that tell you how many particles (protons, electrons, etc.) will hit your satellite at any given point in its orbit.

Trapped Radiation (Van Allen Belts)

- **AE8 / AP8:** The "classic" models (Aerospace Electron/Proton version 8). These have been the industry standard for 30 years. They are **static**, meaning they provide a long-term average but don't account for daily "space weather" fluctuations.
- **AE9 / AP9 / SPM (IRENE):** The modern successors developed by the US Air Force. Unlike the older versions, these are **probabilistic**. They can tell you the "95th percentile" worst-case scenario, allowing for much more precise risk management.

Solar & Cosmic Rays

- **CREME96:** The standard model for predicting **Single Event Effects (SEE)** from Galactic Cosmic Rays and Solar Heavy Ions.
- **ESP / PSYCHIC:** Models used specifically to predict the total fluence of solar protons over a mission’s lifetime, which is critical for solar panel degradation.

2. Key Industry Standards

Standards ensure that every company (like SpaceX, Airbus, or NASA) follows the same rules for safety and testing.

Standard Body	Major Standard	Description

ECSS (Europe)	**ECSS-E-ST-10-04C**	Defines the mandatory models for the **Space Environment** (e.g., using AP8/AE8 as the baseline).
ECSS (Europe)	**ECSS-E-ST-10-12C**	Defines **Design Margins**. It tells engineers: "If the model predicts 10 krad of radiation, you must design the chip to survive 20 krad" (a Radiation Design Margin of 2).
MIL-STD (USA)	**MIL-STD-883**	The "Bible" of testing. Method 1019 defines exactly how to perform **Total Ionizing Dose (TID)** testing in a lab.
JEDEC	**JESD57**	The standard procedures for testing integrated circuits for **Single Event Effects (SEE)** using heavy ion beams.

3. The RHA Process (Radiation Hardness Assurance)

The "Standard" way to build a satellite follows this engineering flow:

1. **Environment Specification:** Use **OMERE** or **SPENVIS** (using AE9/AP9 models) to calculate the radiation flux for your specific orbit (e.g., 500km LEO).
2. **Radiation Transport:** Use a tool like **FASTRAD** to see how much radiation actually makes it *inside* the satellite through the aluminum walls.
3. **Component Selection:** Compare the calculated dose against the "Rad-Hard" data sheets of your microchips.
4. **Application of Margins:** Following **ECSS-E-ST-10-12C**, apply a safety factor (usually 1.2 to 2.0) to account for model uncertainties.

4. Comparison: SPENVIS vs. OMERE

These are the two software ecosystems that implement these models and standards:

- **SPENVIS (ESA):** A web-based interface. It is excellent for quick mission analysis and follows European ECSS standards very strictly.
- **OMERE (TRAD/CNES):** A desktop application. It is highly favored by industrial engineers for creating detailed "Radiation Analysis Reports" required for mission reviews.

A **"Rad-Hard" data sheet** looks very similar to a standard electronic data sheet, but it includes an entirely separate section dedicated to **Radiation Performance**.

While a normal chip's data sheet focuses on speed and power, a rad-hard data sheet focuses on how the chip's performance **degrades** over time and its **threshold** for surviving high-energy particle strikes.

A. Total Ionizing Dose (TID)

This is the "life expectancy" of the chip.

- **Units:** krad(Si) or Gy(Si).
- **What to look for:** A typical "Space Grade" part is usually rated for **100 krad(Si)**.
- **Critical Note:** Look for the term **"ELDRS Free"** (Enhanced Low Dose Rate Sensitivity). This confirms the chip was tested at a slow radiation rate—mimicking actual space conditions—rather than just a fast "burst" in a lab, which can hide certain types of damage.

B. Single Event Latch-up (SEL) Immunity

This is a "pass/fail" metric for the most dangerous type of radiation failure.

- **Metric: LET Threshold** (LETth).
- **What to look for:** You want to see **"SEL Immune up to LET > 60 MeV·cm^2/mg"**.
- **Meaning:** Since the heaviest common ions in the solar system (like Iron) rarely exceed an LET of 60, a rating above this number means the chip is physically designed to never experience a parasitic latch-up in space.

C. Single Event Upset (SEU) Rate

This tells you how often the data on the chip will get corrupted (bit flips).

- **Metric: Cross-Section (σ)** vs. **LET**.
- **What to look for:** A graph showing a "Weibull Curve." This allows engineers to calculate exactly how many bit flips will occur per day in their specific orbit (e.g., "1 error every 1,000 days").

Feature	**Commercial (COTS)**	**Rad-Hard (Space Grade)**
Part Prefix	SN74, MAX, etc.	**5962-xxxx** (SMD Number)
TID Rating	Not guaranteed (usually < 5 krad)	Guaranteed (e.g., 100 krad to 1 Mrad)
SEL	Often susceptible	**Immune by Design**
Packaging	Plastic (prone to outgassing)	**Hermetic Ceramic** or Metal
Price	$1.00 - $10.00	$500 - $5,000+

In radiation effects, the **LET Threshold (LETth)** is the single most important number for determining if a microchip is "safe" from the random, high-energy particle strikes found in space.

It defines the **minimum** amount of energy a particle must deposit into a chip to trigger a malfunction, such as a bit flip (SEU) or a short circuit (SEL).

1. Defining the Metric

- **LET (Linear Energy Transfer):** This is the density of energy a particle loses as it travels through a material (usually Silicon). It is measured in **MeV·cm2/mg**.
- **The Threshold (LETth):** Think of this as the "activation energy."
  - If a particle hits the chip with an LET **lower** than the threshold, nothing happens.
  - If a particle hits with an LET **at or above** the threshold, the chip is susceptible to a "Single Event Effect."

2. Why the Number 37 is Famous

In the space industry, you will often hear engineers mention **37 MeV·cm2/mg**. This is a critical dividing line for mission risk:

- **If LETth >37:** The component is generally considered **immune to proton-induced bit flips**. Since protons are the most common particles in solar storms, having a threshold above 37 significantly simplifies the design, as you only need to worry about the much rarer heavy ions.
- **If LETth <15:** The component is very "soft" (sensitive). It will likely experience frequent bit flips even from background radiation.
- **If LETth >60:** The component is usually considered **"SEL Immune."** It is physically impossible for common space radiation to trigger a destructive latch-up in this chip.

3. The Weibull Curve

On a "Rad-Hard" data sheet, the LET threshold is found at the start of a **Weibull Curve**. This graph plots the "Cross-Section" (probability of an error) against the "LET" (energy of the particle).

1. **Onset (LETth):** The point on the x-axis where the curve first begins to rise above zero.
2. **Rising Slope:** As the particle energy increases, more areas of the chip become vulnerable, and the error rate goes up.
3. **Saturation:** Eventually, the curve levels off. This means the particle is now so energetic that *any* strike on a sensitive area will cause an error.

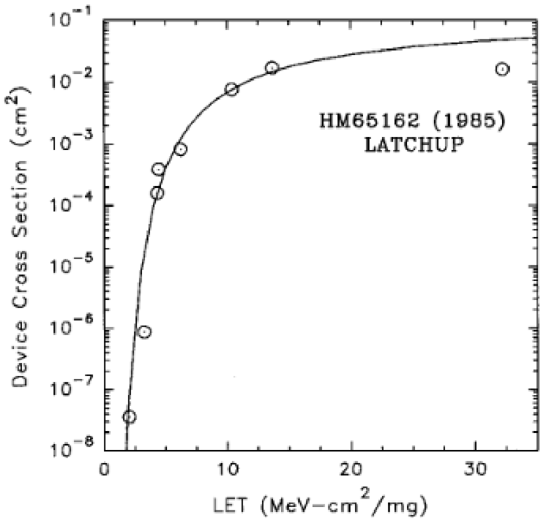
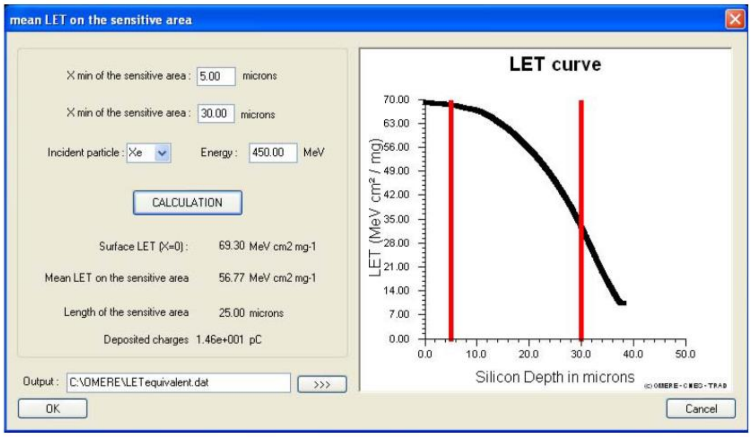


Fig. 1. Heavy-ion SEL cross section for the HM65162 SRAM produced in 1985. Data (points) are from Levinson *et al.* [14]. The curve is from (7) using $\sigma_0 = 0.116$ cm^2, $L_{1/e} = 28.3$ MeV-cm^2/mg.

- **X-Axis (LET):** This represents the energy "punch" of the particle. As you move to the right, the particles are heavier and more energetic (like Iron ions).
- **Y-Axis (Cross Section):** This represents the "target area" or probability of an error occurring. A higher value means the chip is more likely to experience a bit flip.
- **The Threshold (LETth):** Notice where the curve starts to lift off the zero line. This is the **LET Threshold**. Any particle with energy below this point is "safe" and will not cause an error.
- **The "Knee" and Saturation:** The curve eventually levels off at a maximum value. This is the **Saturation Cross Section**, which tells engineers the total physical area of all the sensitive nodes (like memory cells) inside the chip.

Engineers use the mathematical parameters of this Weibull fit (threshold, width, and shape) and plug them into software like **OMERE** or **CREME96** to predict exactly how many errors a satellite will have per day in a specific orbit.

For information, an equivalent LET calculation module is available on OMERE v3.2



Threshold Level	Classification	Action Required
< 10	Very Sensitive	Must use Triple Modular Redundancy (TMR) or error-correcting code (ECC).
15 to 37	Moderately Hard	Safe for most LEO missions with basic software watchdogs.
37 to 60	Hardened	Ideal for long-term GEO or deep space missions.
> 75	Ultra-Hard	Used for military or Jupiter missions (Europa Clipper level).

Analogy: If radiation is like "rain," the **LET Threshold** is the height of your doorstep. If the doorstep is low (LETth =2), even a light drizzle (low-energy protons) will flood your house. If the doorstep is high (LETth =80), only a massive tidal wave (heavy Iron ions) can get inside.

Environment calculations

"Environment calculations" are the mathematical process of predicting exactly what radiation a spacecraft will encounter. Engineers don't just calculate a single number; they build a **Mission Radiation Specification** by following a specific three-step workflow.

1. Defining the Orbit and Mission Duration

The first step is "Orbit Propagation." The software (like **OMERE** or **SPENVIS**) calculates the spacecraft's position in 3D space for every minute of its life.

- **Input:** Apogee, perigee, inclination, and launch date (to account for the 11-year solar cycle).
- **Calculation:** The tool maps these coordinates against the **Van Allen Belt models** (AP8/AE8 or AP9/AE9).
- **Key Result:** A "Mission Fluence" report—a giant list of every proton and electron the satellite will "see" while outside the vehicle.

2. Shielding and Transport Analysis

Once you know the environment *outside*, you must calculate how much gets *inside* to the electronics. This is called **Radiation Transport**.

- **The "Slab" Model:** For quick calculations, engineers assume the satellite is a simple aluminum sphere. They use the **SHIELDOSE-2** algorithm to see how radiation drops as it passes through different thicknesses of metal.
- **Sector Analysis (Ray Tracing):** For real satellites, engineers use 3D CAD models. The software shoots millions of "virtual rays" from a specific chip outward in every direction. It calculates exactly how much aluminum, copper, and circuit board material is blocking each ray.
- **Monte Carlo Simulations:** For complex missions (like Mars), tools like **Geant4** simulate individual particle collisions to see how they shatter and create "secondary" radiation inside the walls.

3. Calculating the Specific Effects

The final step converts those particles into engineering risks. This results in three critical outputs:

A. Total Ionizing Dose (TID) Curve

This is a **Dose-Depth Curve**. It tells the engineer: *"If you have 2mm of shielding, your chip will absorb 15 krad. If you increase it to 5mm, the dose drops to 5 krad."* ### B. Single Event Effect (SEE) Rates The software combines the environment data with the **Weibull Curve** from the chip's data sheet.

- **Formula:** Error Rate=∫(Particle Flux)×(Chip Sensitivity)dE
- **Result:** A prediction like *"This memory chip will have 1.2 bit-flips per day."*

C. Non-Ionizing Energy Loss (NIEL)

This calculates **Displacement Damage**. It is used primarily to predict how much a solar panel's power output will drop each year (e.g., "3% power loss per year due to lattice displacement").

Step	Input	Model/Tool	Output
1. Environment	Trajectory & Date	AP9 / AE9 / CREME96	External Particle Flux
2. Transport	3D CAD / Shielding	FASTRAD / NOVICE	Internal Particle Flux
3. Effects	Chip Data Sheets	OMERE / SPENVIS	TID (krad) & SEU Rates

SHIELDOSE-2 algorithm:

The **SHIELDOSE-2** algorithm is a specialized mathematical tool developed by NASA (specifically by Stephen Seltzer at NIST) to calculate how much radiation dose is absorbed by electronics or tissue behind a shield.

While advanced "Monte Carlo" simulations track every single particle like a video game, SHIELDOSE-2 uses a **lookup table approach**. This makes it incredibly fast—calculating a mission's total dose in seconds rather than hours.

1. How It Works: The "Lookup Table" Method

Instead of simulating particle physics from scratch every time, SHIELDOSE-2 relies on a massive database of pre-calculated "Depth-Dose" data.

1. **Pre-calculation:** Scientists used complex Monte Carlo codes (like ETRAN) to calculate how much energy mono-energetic protons and electrons lose as they travel through aluminum.
2. **Integration:** When you give SHIELDOSE-2 your satellite's specific radiation environment (the "input spectrum"), it looks up the corresponding data in its tables and performs a weighted integration.
3. **Result:** It outputs the absorbed dose (in Rads or Grays) for a specific material (like Silicon) located at a specific depth inside the shield.

2. The Three Standard Geometries

SHIELDOSE-2 is designed for "simple" geometries. It asks you to choose how your component is tucked away:

Geometry	Description	Visual Analogy
Semi-Infinite Plane	A detector buried in a massive wall.	A sensor inside the Great Wall of China.
Finite Slab	A detector sitting behind a flat plate of a specific thickness.	A sensor behind a single sheet of plywood.
Solid Sphere	A detector at the exact center of a solid ball of aluminum.	A seed inside the center of an apple.

3. Improvements in SHIELDOSE-2

The "2" in the name represents a major 1994 update over the original 1980 version. The key upgrades included:

- **Nuclear Interactions:** It now accounts for the fact that high-energy protons can hit aluminum nuclei and shatter them (spallation), creating secondary radiation.
- **Wider Energy Range:** It handles electrons from **5 keV to 50 MeV** and protons up to **10 GeV**.
- **More Materials:** While the shield is always aluminum, it can calculate the dose absorbed in different "target" materials, including:
    - **Silicon (Si) / Silicon Dioxide (SiO_2):** For microchips.
    - **Tissue / Water:** For astronaut safety.
    - **Gallium Arsenide (GaAs):** For solar cells.

4. Current Status: SHIELDOSE-2Q

If you use the European **SPENVIS** tool today, you are likely using **SHIELDOSE-2Q**.

- **The "Q":** Stands for "Extended."
- **What's new:** It adds more shielding materials beyond just aluminum (like Titanium, Tantalum, and Tungsten) and fixes a long-standing database bug involving how "bremsstrahlung" (secondary X-rays) were calculated for thin slabs.

When to use it: SHIELDOSE-2 is perfect for the **Preliminary Design Phase**. It gives you a "ballpark" idea of how much aluminum you need. Once the satellite's design is final and complex, you switch to 3D tools like **FASTRAD**.

A **SHIELDOSE-2** output file is essentially a data table that breaks down the total radiation dose into its individual contributors. This allows engineers to see exactly *what* is causing the damage—whether it's trapped electrons, solar protons, or secondary X-rays.

Here is a simplified example of what you would see in a standard .txt or .out report from a SHIELDOSE-2Q run:

Sample Output: Total Mission Dose (Silicon Target)

Mission Duration: 1.00 Year

Shield Geometry: Center of Solid Sphere

Target Material: Silicon (Si)

Depth (mm Al)	Trapped Protons (rads)	Solar Protons (rads)	Electrons (rads)	Bremsstrahlung (rads)	Total Dose (rads)
0.1	1.25×10^5	4.50×10^4	6.80×10^6	1.20×10^3	6.97×10^6
1	4.20×10^4	1.10×10^4	3.50×10^5	9.50×10^2	4.04×10^5
3	2.10×10^4	6.20×10^3	1.40×10^4	6.10×10^2	4.18×10^4
5	1.60×10^4	4.10×10^3	9.80×10^2	4.20×10^2	2.15×10^4
10	9.50×10^3	2.10×10^3	1.50×10^1	2.30×10^2	1.18×10^4

Dose-Depth Curve:

Deciding on the thickness of a satellite's aluminum "skin" is a balancing act between protecting the electronics and keeping the launch weight low. Engineers use a **Dose-Depth Curve** to find the "sweet spot" where the electronics are safe but the satellite isn't unnecessarily heavy.

Here is a step-by-step example of how this engineering decision is made.

Step 1: Establish the "Tolerance" of your Electronics

Before looking at the shielding, engineers look at the parts list. Every microchip has a **TID (Total Ionizing Dose)** limit.

- **The Component:** Let's say you are using a standard high-quality microprocessor rated for **30 krad**.
- **The Safety Margin (RDM):** Space agencies (like NASA or ESA) require a **Radiation Design Margin (RDM)**, typically **2**.
- **The Target Dose:** This means the dose *inside* the satellite must be no more than **15 krad** (30÷2) to ensure the chip is safe even if the radiation models have some error.

Step 2: Read the Dose-Depth Curve

The engineer runs an environment simulation (like **SHIELDOSE-2**) for the specific mission orbit (e.g., a 5-year mission in a high-radiation polar orbit). This produces the **Dose-Depth Curve**.

Shielding Thickness (mm Al)	Predicted Dose (krad)
1 mm	80 krad
2 mm	35 krad
3 mm	18 krad
4 mm	**12 krad**
5 mm	9 krad

Step 3: Find the "Knee" of the Curve

Engineers look for the **"Knee"**—the point where the curve stops dropping sharply and starts to level off.

- **1 mm to 2 mm:** Adding 1mm of aluminum cuts the dose in half (from 80 to 35). This is a "cheap" way to get a lot of protection.
- **4 mm to 5 mm:** Adding another 1mm only drops the dose by 3 krad. At this point, you are adding a lot of weight for very little benefit.

Step 4: The Final Decision

Based on our **15 krad target** (from Step 1), the engineer looks at the table:

- **2 mm** (35 krad) is way too high; the chip will fail.
- **3 mm** (18 krad) is close, but doesn't quite meet our 15 krad safety target.
- **4 mm** (12 krad) meets the target with room to spare.

The Decision: The satellite skin will be designed at **4 mm**.

Step 5: "Spot Shielding" (Weight Optimization)

Wait! Making the *entire* satellite 4 mm thick is incredibly heavy and expensive to launch. To save money, engineers use a trick:

1. **Chassis:** Build the main satellite body with a thin **2 mm** skin (saving weight).
2. **The Environment:** At 2 mm, the internal dose is 35 krad.
3. **Spot Shielding:** Take just that one sensitive microprocessor and glue a small, 2 mm thick **tantalum or lead "hat"** directly onto the chip or its box.
4. **Result:** The chip now has effectively 4 mm of protection (2 mm skin + 2 mm "hat"), while the rest of the satellite stays lightweight.

Action	Result
Target Dose	15 krad (includes a margin of 2).
Required Thickness	4 mm (based on the curve).
Strategy	2 mm Aluminum skin + 2 mm Tantalum spot shield.

Sector Analysis:

In a real satellite, your electronics aren't just sitting behind a simple sheet of aluminum. They are buried inside boxes, surrounded by wire harnesses, and shielded by other parts like the battery or the structural frame.

To account for this, engineers move beyond simple "slab" models and use **Sector Analysis** (also called Sector Shielding Analysis).

To account for this, engineers use **Sector Analysis** (also known as Ray Tracing). This method moves beyond simple "flat wall" math and treats the entire satellite as a complex, 3D shield.

1. The Concept: "Self-Shielding"

Sector analysis assumes that the best shielding is the satellite itself. If a sensitive chip is located in the center of the spacecraft, a radiation particle coming from the "left" might have to pass through the outer skin, a structural bracket, and a solid battery pack before hitting the chip. However, a particle coming from the "right" might only have to pass through a thin access panel.

2. How the Ray-Tracing Process Works

Engineers use 3D software (like **FASTRAD** or the **SSAT** tool in SPENVIS) to perform the following steps:

1. **Define the "Target":** The engineer selects a specific point in the 3D CAD model (like the silicon die inside a microprocessor).
2. **Shoot Virtual Rays:** The software shoots thousands of "virtual rays" (sometimes called "geantinos") out from that point in every possible direction, covering a full sphere (4π steradians).
3. **Calculate "Areal Density":** For every single ray, the software calculates every object it hits. It multiplies the thickness of that object by its material density (Thickness×Density=g/cm2).
   a. *Example:* A 2mm aluminum plate is roughly 0.54 g/cm2.

The Math: If a ray passes through 2mm of Aluminum and then 5cm of a plastic battery casing, the software calculates:

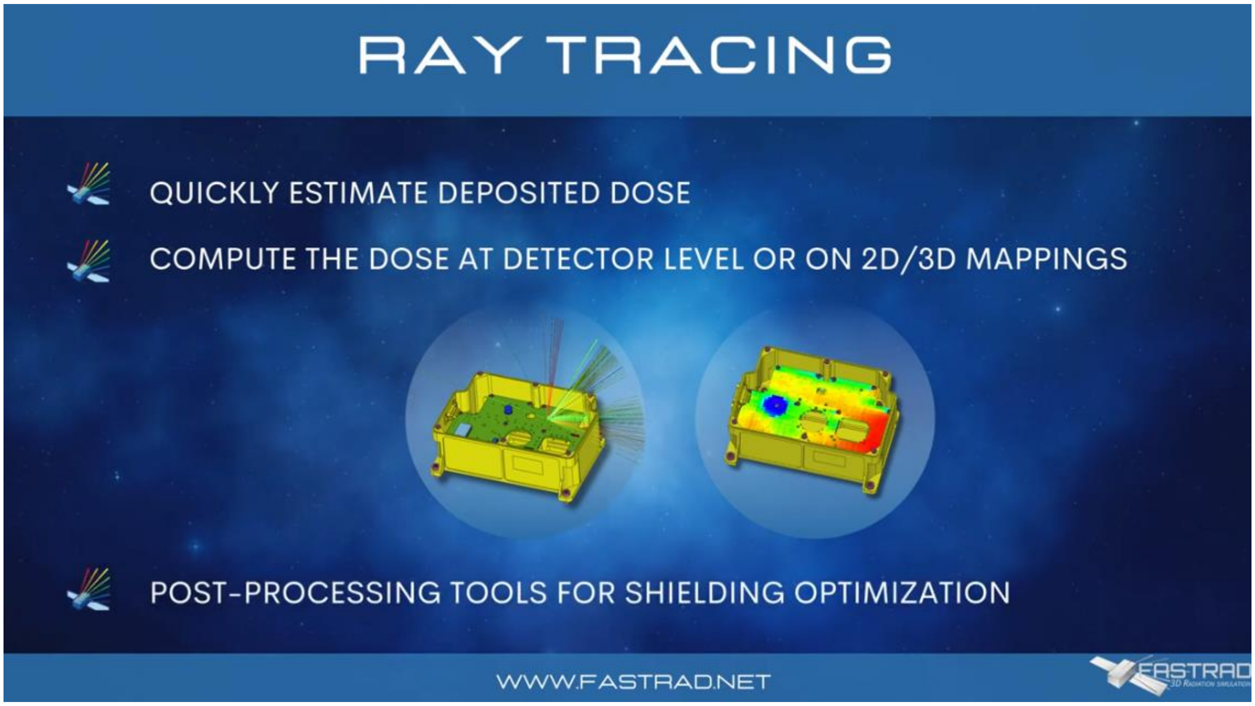
$$(\text{Thickness}_{Al} \times \text{Density}_{Al}) + (\text{Thickness}_{Plastic} \times \text{Density}_{Plastic}) = \text{Total Areal Density for that Ray}$$

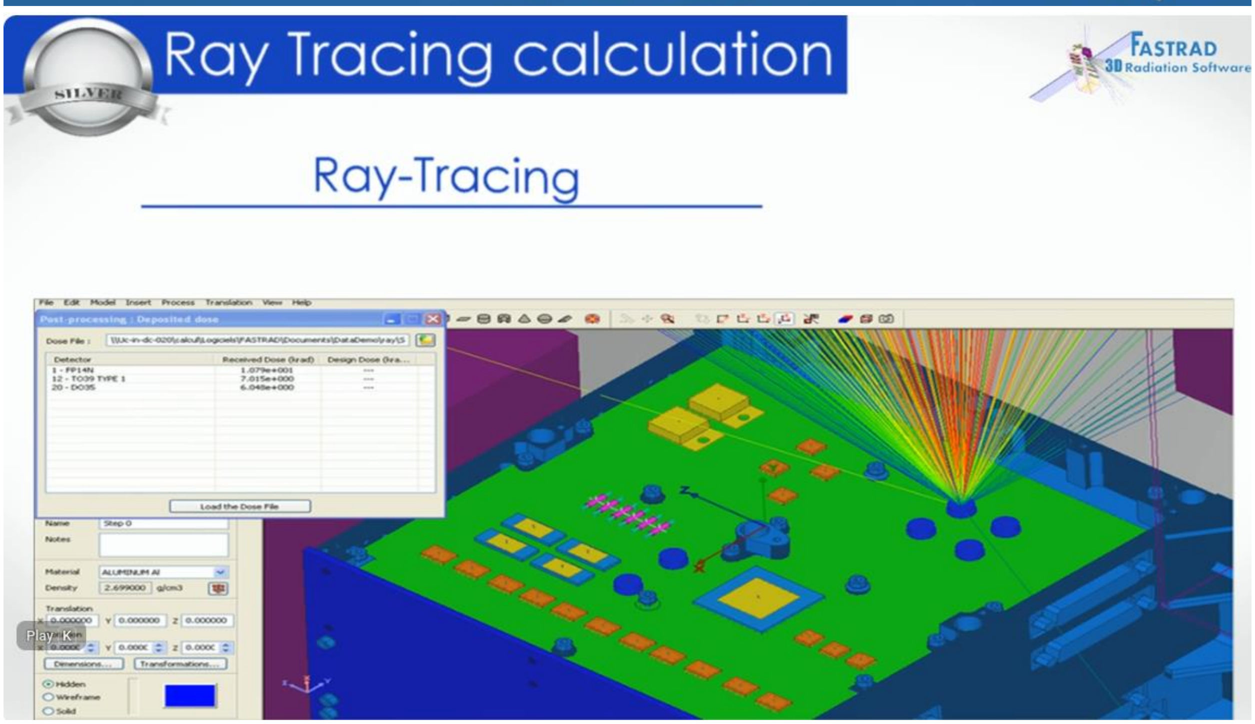
3. Creating the Shielding Distribution

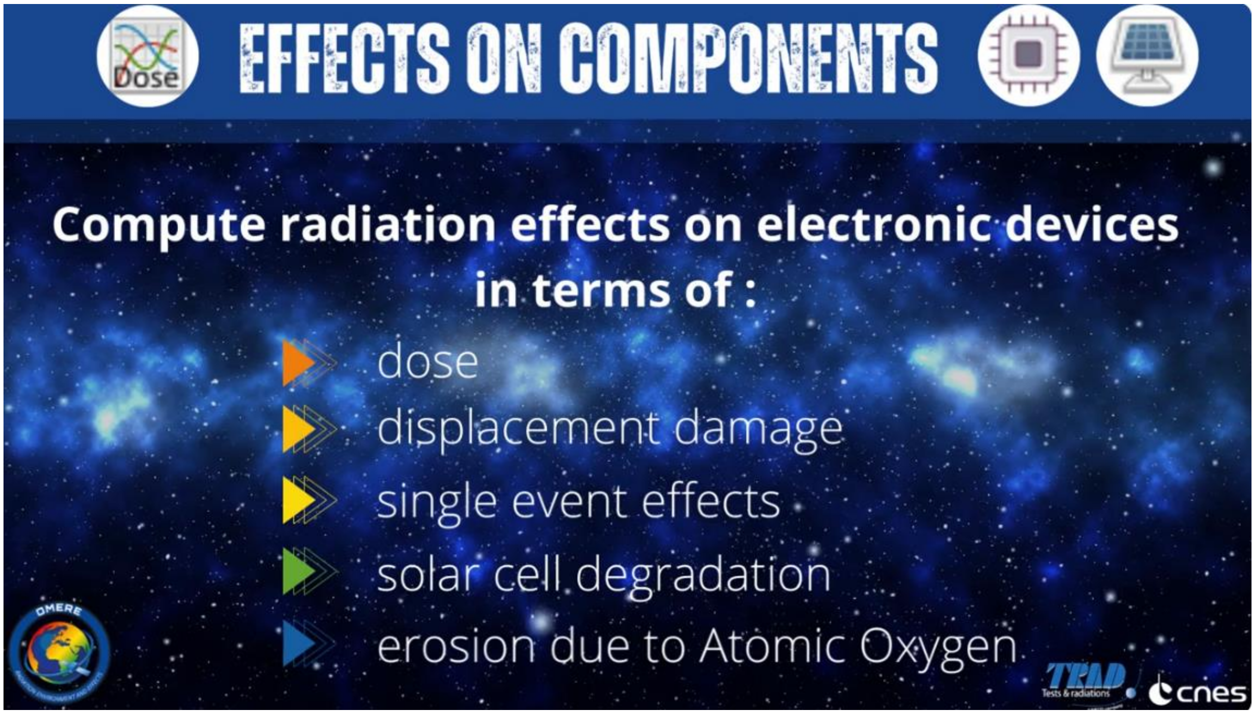
After shooting thousands of rays, the software creates a **Shielding Distribution Histogram**. This is essentially a "map" of the satellite's protection.

Thin Sectors: Directions where rays only hit the outer skin (shown as low density on the histogram).

Thick Sectors: Directions where rays pass through the battery or the main frame (shown as high density).







4. Converting Rays to Dose

Once the software has the shielding map, it combines it with the **Dose-Depth Curve** we calculated earlier:

- For a "thin" sector (like a window or a thin panel), the software assigns a **high dose**.
- For a "thick" sector (where the ray passes through the battery), it assigns a **very low dose**.
- **The Result:** The software performs a "weighted average" of all these sectors to give you the **Total Sector Integrated Dose**.

5. Optimized "Spot Shielding"

If the Sector Analysis shows that the dose is still too high, the engineer doesn't thicken the whole satellite. Instead, they look at the 3D map to find the **"Weak Sectors"** (the directions where the shielding is thinnest).

They then apply **Spot Shielding**:

- They place a small, heavy "slug" of **Tantalum** or **Tungsten** directly in the path of those weak rays.
- This provides maximum protection for minimum weight.

Radiation Design Margin (RDM):

The **Radiation Design Margin (RDM)** is the final "pass/fail" number presented at a satellite's Mission Review. It represents the safety buffer between what a chip *can* survive and what the environment will actually *throw* at it.

Once the Sector Analysis provides the final dose, engineers use the following steps to calculate and report the margin.

1. The RDM Formula

The calculation is straightforward but critical:

RDM=Calculated Sector Integrated Dose (SID)Radiation Tolerance of the Component (TID)

The calculation is straightforward but critical:

$$RDM = \frac{\text{Radiation Tolerance of the Component (TID)}}{\text{Calculated Sector Integrated Dose (SID)}}$$

- **TID:** Taken from the "Rad-Hard" Data Sheet (the point where the chip actually fails).
- **SID:** Taken from your 3D Sector Analysis (the realistic dose behind the satellite's structure).

2. Industry Standards for Margins

Space agencies like NASA and ESA have strict rules about what RDM is acceptable. These rules exist because radiation models (like AP9/AE9) are statistical predictions and have a margin of error.

RDM Value	Status	Engineering Action
RDM > 2.0	**Green (Safe)**	No further action needed. The part is significantly tougher than the environment.
1.0 < RDM < 2.0	**Yellow (At Risk)**	Requires a "Radiation Waiver" or more shielding. The buffer is too thin for high-reliability missions.
RDM < 1.0	**Red (Fail)**	**The part will likely fail.** You must change the part or drastically increase shielding.

The "RDM = 2" Rule: Most high-reliability missions (Class A/B) require a margin of at least 2. This means that even if the space weather is twice as bad as predicted, the satellite will still survive.

3. A Real-World Calculation Example

Imagine you are reviewing a **Microcontroller** for a 5-year mission:

1. **From the Data Sheet:** The chip is rated for **50 krad**.
2. **From Sector Analysis:** The calculated dose at the chip's location is **18 krad**.
3. **Calculation:** $50 \div 18 = 2.77$.
4. **Verdict:** Since $2.77 > 2.0$, the part is approved for flight.

4. The Radiation Analysis Report (RAR)

At a formal mission review (like a Critical Design Review or CDR), engineers present a **Radiation Analysis Report**. It usually features a "Stoplight" chart:

- **Green Parts:** Parts that naturally meet RDM>2.
- **Yellow Parts:** Parts that required "Spot Shielding" (like a tantalum lid) to move from an RDM of 0.8 to 2.2.
- **Waivers:** If a part is mission-critical (like a unique high-speed sensor) but only has an RDM of 1.5, the engineers must write a formal document explaining why they believe the mission is still safe.

5. What if the RDM is too low?

If the RDM comes back at **0.5**, the engineering team has three options:

1. **Shielding:** Add more aluminum or tantalum (Mass penalty).
2. **Part Swap:** Find a more expensive "Rad-Hard" version of the chip (Cost penalty).
3. **Relocation:** Move the chip deeper into the satellite to take advantage of the shielding from the battery or frame (Design complexity).

ELDRS (Enhanced Low Dose Rate Sensitivity):

ELDRS (Enhanced Low Dose Rate Sensitivity) is a phenomenon that primarily affects **bipolar technology** (like operational amplifiers, voltage regulators, and transistors).

It is considered a "silent killer" because it can make a component look perfectly safe in a lab test, only for it to fail miserably once it gets into the slow, steady radiation of space.

1. The Lab vs. Space Mismatch

Normally, in engineering, if you want to see if something will break, you hit it hard and fast.

- **High Dose Rate (HDR):** In a lab, we use a Cobalt-60 source to give a chip its 5-year radiation dose in just a few **hours**.
- **Low Dose Rate (LDR):** In space, that same dose is spread out over **5 to 10 years**.

For most CMOS chips, HDR testing is "worst-case," so if it passes the lab, it passes in space. But for **ELDRS-sensitive parts**, the opposite is true: the slower the radiation comes in, the **more damage** it does.

2. Why Does This Happen?

Without getting too deep into the physics, it comes down to "space charge" in the thick oxides of bipolar transistors:

- **In the Lab (Fast):** The radiation creates so many ions so quickly that they build up a "wall" of electric charge. This wall actually **protects** the rest of the chip by repelling further ions.
- **In Space (Slow):** The ions trickle in slowly. No "wall" forms, allowing the ions to migrate deep into the sensitive interfaces of the transistor, where they destroy the gain and increase leakage current.

3. How ELDRS Ruins your RDM

This is where the engineering danger lies. If an engineer doesn't know a part is ELDRS-sensitive, their **Radiation Design Margin (RDM)** calculation will be a lie.

The "Fake" RDM (Based on Lab HDR Testing):

- Chip survives **100 krad** in the lab.
- Mission dose is **20 krad**.
- **Calculated RDM = 5.0 (Looks very safe!)**

The "Real" RDM (What actually happens in Space):

- Because of ELDRS, the chip actually fails at **10 krad** when irradiated slowly.
- Mission dose is still **20 krad**.
- **Actual RDM = 0.5 (The mission will fail!)**

4. How Engineers Protect the Mission

To prevent this, industry standards like **MIL-STD-883, Method 1019** require specialized testing for bipolar parts.

1. **Look for "ELDRS Free" Parts:** Engineers prioritize parts that have been tested at very low dose rates (e.g., 10 mrad(Si)/s) and shown no enhanced sensitivity.
2. **The "Over-Test" Rule:** If a part is known to be ELDRS-sensitive but must be used, NASA often requires it to be tested to **4 to 10 times** the mission dose in the lab to "guess" the slow-rate damage.
3. **Check the Data Sheet:** A true rad-hard data sheet will explicitly state: *"Tested at both High and Low Dose Rates (ELDRS characterized)."*

Summary: The RDM Safety Checklist

When you are looking at a final Radiation Analysis Report, you must ask:

- Was the RDM calculated using HDR or LDR data?
- Are there any bipolar parts in the system?
- If yes, are they "ELDRS Free"?

SEE rate calculation

Calculating the **SEE (Single Event Effect) rate** is the process of predicting how many "random" events—like bit flips (SEUs) or latch-ups (SELs)—will occur in a specific microchip during a mission.

Unlike TID (which is a steady wear-out), SEE rates are expressed as a probability, typically in **Errors per Device-Day**.

1. The Three Ingredients

To calculate the rate, you need to combine three distinct sets of data:

A. The Environment (Particle Flux)

You use models (like **CREME96**) to generate an **LET Spectrum**. This tells you exactly how many particles of each "strength" (LET) will hit your satellite per square centimeter, per second, in your specific orbit.

B. The Chip Sensitivity (Weibull Curve)

This comes from ground testing at a cyclotron. It tells the software the "target area" (σ) of the chip for every energy level.

- **Threshold (LETth):** Where errors start.
- **Saturation (σsat):** The maximum sensitive area.

C. The Geometry (Sensitive Volume)

The software needs to know the physical dimensions of the transistor's sensitive region (usually a tiny 3D box of silicon) because a particle hitting at an angle travels a longer path and deposits more charge.

2. The Math: The Convolution Integral

The calculation is essentially a "mapping" of the environment onto the chip's sensitivity. The simplified formula is:

$$\text{SEE Rate} = \int_{LET_{th}}^{LET_{max}} \Phi(L) \cdot \sigma(L) \, dL$$

-
- **Φ(L)**: The flux of particles at a specific LET.

- **σ(L)**: The cross-section (sensitivity) of the chip at that same LET.
- The software performs this math for every type of particle (protons, heavy ions) and every energy level.

3. Industry Standard Tools

Engineers rarely do this by hand. They use specialized software suites:

- **CREME96:** The classic tool for Galactic Cosmic Ray (GCR) and solar flare SEE rates. It is the "gold standard" for deep space missions.
- **OMERE / SPENVIS:** These tools allow you to import your mission's trajectory and the chip's Weibull parameters to generate a report in seconds.

4. How to Interpret the Result

Once the calculation is done, you get a number like: **1.2×10−5 errors/bit-day**.

Engineers then scale this up to the system level:

1. **Bit to Chip:** If your memory chip has 1 Gigabit (109 bits), that's 1.2×10−5×109=12,000 errors per day.
2. **Mitigation Check:** If your system uses **ECC (Error Correcting Code)**, it might be able to fix 12,000 single-bit errors instantly.
3. **Criticality:** However, if the calculation is for a **Latch-up (SEL)** and the rate is 1×10−4 per year, you know that over a 10-year mission, there is a very real chance (0.1%) the satellite will experience a destructive short-circuit.

5. Worst-Case vs. Average Rates

Reports usually provide two different rates:

- **Quiet Environment:** The background rate from cosmic rays (GCR). This is what happens on a "normal" day.
- **Worst-Week (Solar Flare):** The rate during a massive solar particle event. The SEE rate can jump by **1,000x to 10,000x** during a flare.

The Design Rule: Your satellite must be able to "keep its head above water" (clear its error logs) faster than the **Worst-Week** rate, or the memory will overflow and the computer will crash during a solar storm.

Worst-Case Analysis (WCA):

Worst-Case Analysis (WCA) is the mathematical proof that a circuit will still function at the very end of a mission, even after radiation has "degraded" every single component.

While a satellite is in orbit, radiation doesn't just cause bit flips; it physically changes the electrical properties of the parts. WCA ensures these changes don't lead to a "functional failure" (e.g., a power supply providing 4V instead of 5V).

1. The "Big Three" Radiation Drifts

In a WCA, engineers apply "Post-Rad" values to their circuit simulations. We look for three primary degradations:

- **Threshold Voltage Shift (Vth):** In MOSFETs, radiation causes the gate to require more (or less) voltage to turn on. This can make a switch "leaky" or prevent it from turning on entirely.
- **Gain Degradation (hFE):** In bipolar transistors, the gain drops significantly. If a circuit relies on a transistor to amplify a signal 100x, but radiation drops the gain to 20x, the circuit may stop working.
- **Leakage Current (Icc):** As TID (Total Ionizing Dose) increases, chips pull more current from the power supply even when they are "off." If every chip on a board starts leaking, the power supply might overheat.

2. The Calculation Methods: EVA vs. RSS

Engineers use two different mathematical approaches to combine these radiation drifts with standard aging and temperature effects.

A. Extreme Value Analysis (EVA) - "The Absolute Worst Case"

This method assumes that **everything** that could go wrong happens at the same time: the part is at its maximum temperature, it's 10 years old, and it has hit its maximum radiation limit.

- **Formula:** ValueWorst =ValueNominal +ΔTemp +ΔAging +ΔRadiation
  - **Formula:** $Value_{Worst} = Value_{Nominal} + \Delta_{Temp} + \Delta_{Aging} + \Delta_{Radiation}$
- **Use Case:** Critical safety systems (fuses, pyrotechnics, main processors).

B. Root Sum Square (RSS) - "The Statistical Reality"

This assumes that it is statistically unlikely for every component to be at its absolute worst limit simultaneously.

- **Formula:** ValueWorst =
  - **Formula:** $Value_{Worst} = Value_{Nominal} + \sqrt{\Delta^2_{Temp} + \Delta^2_{Aging} + \Delta^2_{Radiation}}$
-
- **Use Case:** Non-critical telemetry or sensors where a small error is acceptable.

3. Example: A Voltage Reference Circuit

Imagine a circuit that needs to provide a steady **2.50V** to an Analog-to-Digital Converter.

1. **Beginning of Life (BOL):** The circuit is tested and outputs exactly **2.50V**.
2. **The Radiation Factor:** Radiation data shows the internal transistors will shift, causing the output to drift by **± 100mV**.
3. **The Aging Factor:** 10 years in space adds another **± 50mV** of drift.
4. **The WCA Result (EVA):** The engineer calculates that at EOL, the voltage could be as low as **2.35V**.
5. **The Decision:** The engineer checks the ADC data sheet. If the ADC requires at least **2.40V** to function, the design **fails WCA**.

The Fix: The engineer must either find a more stable "Rad-Hard" reference or add a trim circuit to calibrate the voltage mid-mission.

4. The WCA Flow Chart

A formal WCA is a massive document (often hundreds of pages) that follows this logic for every single resistor, capacitor, and chip on the spacecraft.

Summary: BOL vs. EOL

The most important thing to remember in space engineering is that **Beginning of Life (BOL)** performance is almost irrelevant.

Feature	**Beginning of Life (BOL)**	**End of Life (EOL)**
Component Values	Precise (1% resistors)	Drifted (5% to 10%)
Power Consumption	Low (Nominal)	High (Radiation Leakage)
Circuit Speed	Fast	Slower (Transistor degradation)
Reliability	High	Defined by WCA Margins

Characterisation of radiation effects on electronic components

1. Single Events

1-1. Physical phenomena and SEE types:

When a high-energy particle (like a heavy ion or a proton) strikes a semiconductor, it doesn't just hit it like a bullet; it interacts electrically. These interactions cause **Single Event Effects (SEE)**, which are divided into "Soft" (recoverable) and "Hard" (destructive) errors.

1. The Physical Phenomenon: Charge Collection

The fundamental cause of every SEE is **Ionization**.

As a particle travels through silicon, it loses energy by stripping electrons away from silicon atoms. This creates a "track" of **electron-hole pairs**. If this track occurs near a sensitive part of a transistor (like a PN junction), the electric field "sweeps" these charges into the circuit.

- **Critical Charge (Qcrit):** Every circuit node has a threshold. If the particle deposits more charge than Qcrit , the circuit will "misinterpret" that noise as a legitimate signal.
- **Linear Energy Transfer (LET):** This is the measure of how much energy the particle deposits per unit of distance. Higher LET = more charge = higher chance of an SEE.

2. Non-Destructive "Soft" Errors

These errors cause the data to be wrong, but the hardware remains physically healthy.

Single Event Upset (SEU)

This is a "bit flip." A digital 0 becomes a 1, or vice-versa. This happens in memory cells (SRAM, DRAM) or flip-flops inside a processor.

Single Event Transient (SET)

A momentary voltage spike or "glitch" in an analog circuit or combinational logic. If this spike arrives at a clock edge, it can be "latched" into memory, turning into an SEU.

Single Event Functional Interruption (SEFI)

A "super-error." The particle hits a critical control circuit (like a reset line or a mode-select register), causing the entire chip to freeze, go into a test mode, or stop communicating. A power-cycle usually fixes it.

3. Destructive "Hard" Errors

These effects cause permanent physical damage. The chip may melt, short-circuit, or develop a "permanent bit" that can never be changed.

Single Event Latch-up (SEL)

In CMOS circuits, there are "parasitic" transistors that are usually dormant. A particle strike can "turn on" these hidden paths, creating a low-impedance short-circuit between Power and Ground. The chip will pull massive current until it literally melts itself.

Single Event Burnout (SEB)

Primarily affects **Power MOSFETs**. When the transistor is "OFF" (holding back high voltage), a particle strike can trigger a "second breakdown." The high voltage rushes through the ion track, causing localized melting.

Single Event Gate Rupture (SEGR)

A particle strikes the thin **Gate Oxide** while a high voltage is applied. The ion track acts like a conductive needle, allowing a plasma discharge to punch a permanent hole through the insulation.

Summary of SEE Types

Effect	Type	Result	Recovery
SEU	Soft	Bit Flip	Rewrite data
SET	Soft	Voltage Glitch	Filter or wait
SEFI	Soft	Chip Hang/Freeze	Reset or Power Cycle
SEL	Hard/Destructive	High-Current Short	Must cycle power fast or chip dies
SEB/SEGR	Hard/Destructive	Physical Rupture	Permanent Failure

1-2. Elements for mitigation of SET, SEU, etc:

Since shielding can never block 100% of high-energy particles, engineers must build "fault-tolerant" designs. Mitigation for **SEUs (bit flips)** and **SETs (glitches)** follows two different paths: one focuses on **data integrity**, and the other focuses on **signal timing**.

1. SEU Mitigation (Digital & Data Level)

Single Event Upsets are "bit flips" in memory or logic. The goal is to detect the flip and correct it before the system executes a wrong command.

- **Triple Modular Redundancy (TMR):** The most robust digital defense. The logic is implemented three times in parallel, and a **Majority Voter** compares the outputs. If one bit flips, the other two "outvote" it.
- **Error Correcting Code (ECC):** Used for large memory banks (RAM/Flash). Extra "check bits" are stored with every data word. **SEC-DED** (Single Error Correction, Double Error Detection) allows the hardware to automatically fix a bit flip "on the fly" as it is read.
- **Memory Scrubbing:** This is a background task that constantly "walks" through the memory, checks for errors using ECC, fixes them, and writes the clean data back. This prevents SEUs from accumulating into unfixable double-bit errors over time.

2. SET Mitigation (Signal & Timing Level)

Single Event Transients are momentary voltage glitches. The goal is to prevent a 1 nanosecond pulse from being misinterpreted as a real digital pulse.

- **Temporal Filtering (Time-Domain Voting):** Instead of three physical copies (like TMR), the system samples the same signal at three slightly different times. Since a radiation-induced glitch is almost always shorter than the delay between samples, the voter will see the glitch in only one sample and ignore it.

- **Low-Pass Filtering:** In analog circuits or slow control lines, adding a small capacitor acts as a "speed bump." The high-frequency energy of an SET spike is absorbed by the capacitor, smoothing the signal before it reaches the next component.
- **Gate Sizing:** At the chip design level, engineers can use larger transistors for critical clock lines. Larger transistors have a higher **Critical Charge (Qcrit)**, meaning a particle must be much more powerful to cause a glitch.

3. Summary of Mitigation Elements

Feature	**Mitigation Element**	**Benefit**	**Trade-off**
Logic	**TMR**	Instant correction	3x Power & Area
Memory	**ECC / Scrubbing**	High reliability for mass data	Small latency penalty
I/O Lines	**Capacitors / Filters**	Blocks glitches (SET)	Slows signal speed
Global	**Temporal Voting**	Filters timing glitches	Reduced clock frequency

4. Elements for "Hard" and "Functional" Errors (SEL, SEFI, SEB)

While SEU/SET are about data, these elements protect the hardware itself:

- **Watchdog Timers (for SEFI):** An independent timer that resets the processor if it "hangs" or freezes due to a functional interrupt.
- **Current Limiters (for SEL):** Fast-acting switches that cut power in microseconds if they detect the high-current state of a Latch-up, saving the chip from melting.
- **Voltage Derating (for SEB/SEGR):** Running a power MOSFET at only 50% of its rated voltage to reduce the internal electric field, preventing catastrophic breakdown.

1-3. Experimental characterization:

Experimental characterization is the process of physically proving how a component reacts to radiation. Since simulation models have limits, engineers take real hardware to specialized facilities to create "Ground Truth" data.

This characterization is divided into two distinct campaigns: **TID (Total Ionizing Dose)** testing and **SEE (Single Event Effects)** testing.

1. TID Characterization (Wear-out Testing)

The goal is to determine the "failure point" of a component as it slowly degrades.

- **The Source:** Usually a **Cobalt-60 (Co60)** pool or cell. It emits high-energy gamma rays that provide a uniform ionization field.
- **The Setup:** Parts are placed on a "bias board" so they are powered on and toggling during irradiation. This is critical because "off" chips often degrade differently than "on" chips.
- **The Measurement:** At specific dose steps (e.g., 10 krad, 30 krad), the parts are removed and tested in an Automated Test Equipment (ATE) suite to check for parameter drift.

2. SEE Characterization (Random Event Testing)

This tests the chip's vulnerability to "strikes" from heavy ions and protons.

- **The Source:** A **Cyclotron** or **Particle Accelerator** (e.g., Texas A&M, Lawrence Berkeley, or CERN). These machines fire specific ions (like Argon, Krypton, or Xenon) at a fraction of the speed of light.
- **The Method:** The chip's plastic packaging must be removed (**decapsulated**) because heavy ions cannot penetrate the plastic to reach the silicon die.
- **The Goal:** To build a **Weibull Curve**. Engineers vary the angle of the chip and the type of ion to change the **LET (Linear Energy Transfer)**. They count how many errors (SEUs, SELs) occur at each energy level.

3. Key Data Output: The Weibull Curve

The result of an SEE campaign is the **Cross-Section (σ) vs. LET** graph. This is the "DNA" of the chip's radiation sensitivity.

- **Threshold (L_{th}):** The minimum energy required to cause the first error.
- **Saturated Cross-Section (σ_{sat}):** The point where increasing the particle energy no longer increases the error rate (effectively the physical "target size" of the sensitive transistors).

4. Characterization Levels (The "Test-as-you-Fly" Principle)

Engineers characterize at different levels of integration to capture different failure modes:

Level	Goal	Example
Component	Find the raw silicon limits.	Testing a single Transistor or Op-Amp.
Board Level	See how circuit design mitigates errors.	Testing a CPU with its filtering capacitors.
System Level	Verify software recovery (Watchdogs/TMR).	Testing the entire Flight Computer while it runs code.

5. Standardized Protocols

To ensure the data is valid for flight, experiments must follow strict international standards:

- **MIL-STD-883, Method 1019:** The "Bible" for TID testing.
- **ESCC 25100:** The European standard for Single Event Effect testing.
- **JESD57:** The standard for heavy ion procedures.

2. Dose & Displacement Damage

2-1. Effects related to specific technologies

In space radiation physics, we divide "Total Dose" into two distinct physical mechanisms: **Total Ionizing Dose (TID)** and **Displacement Damage Dose (DDD)**. While both degrade electronics, they attack the silicon lattice in fundamentally different ways.

1. Total Ionizing Dose (TID)

TID is caused by the accumulation of **charged pairs** (electrons and holes) created by ionizing radiation (electrons and protons) in the insulating layers of a chip.

- **The Physics:** Radiation hits the **Silicon Dioxide (SiO_2)** gate insulator. Electrons are mobile and move out, but "holes" (positive charges) get trapped at the interface.
- **The Effect:** This buildup of positive charge creates a "phantom" electric field.
- **Symptoms:** * **Threshold Voltage Shift (V_{th}):** Transistors turn on too early or won't turn off.
 - **Leakage Current:** The chip pulls more power even when idle, eventually leading to a thermal burnout.

2. Displacement Damage Dose (DDD)

DDD, also known as **Non-Ionizing Energy Loss (NIEL)**, is caused primarily by heavy particles like **protons and neutrons**.

- **The Physics:** Instead of just stripping electrons, the particle physically "kicks" a silicon atom out of its position in the crystal lattice. This creates a **Vacancy** or a "Frenkel Pair."
- **The Effect:** These "holes" in the crystal lattice create new energy levels that trap charge carriers or act as "recombination centers."
- **Symptoms:**
    - **Reduced Minority Carrier Lifetime:** This is catastrophic for optics and bipolars.

3. Effects Related to Specific Technologies

Different semiconductor "recipes" respond differently to these two threats.

A. CMOS (Processors, RAM, FPGAs)

- **Primary Threat: TID**.
- **Behavior:** Modern CMOS is actually quite resistant to DDD because it is a "majority carrier" device. However, as transistors get smaller (5nm, 7nm), the insulating layers get thinner, which actually *helps* TID resistance but increases the risk of **Single Event Effects (SEE)**.

B. Bipolar (Op-Amps, Voltage Regulators)

- **Primary Threat: TID & ELDRS**.
- **Behavior:** Bipolar parts are highly sensitive to the **Dose Rate**. As we discussed earlier, they often fail faster at the low dose rates found in space than in high-speed lab tests.

C. Optoelectronics (CCDs, CMOS Sensors, LEDs, Solar Cells)

- **Primary Threat: DDD (Displacement Damage)**.
- **Behavior:** These are the most DDD-sensitive parts on a satellite.

- **Solar Cells:** Lose efficiency as the lattice damage prevents electrons from reaching the contacts.
- **CCDs:** Develop "Dark Current" (white spots on the image) because the lattice vacancies "leak" electrons into the pixels even when the lens cap is on.

D. Compound Semiconductors (GaN, SiC)

- **Primary Threat: SEE (Single Event Effects)**.
- **Behavior:** Wide-bandgap materials like Gallium Nitride (GaN) are incredibly "Rad-Hard" against TID (often surviving > 1 Mrad). However, they can be prone to **Single Event Burnout (SEB)** because they operate at very high voltages and power densities.

Summary Table: Technology vs. Vulnerability

Technology	TID Sensitivity	DDD Sensitivity	Primary Failure Mode
CMOS (Digital)	High	Low	Leakage Current / Vth shift
Bipolar (Analog)	High (ELDRS)	Medium	Gain Loss (hFE)
Optics (Sensors)	Medium	**Very High**	Dark Current / CTE Loss
Power (MOSFETs)	High	Low	Gate Rupture / Burnout
GaN / SiC	**Very Low**	Medium	Heavy Ion Burnout

2-2. Dose computation methodologies:

To calculate the radiation dose a satellite will receive, engineers move from broad environmental models to specific 3D shielding math. Dose computation is generally categorized into three methodologies, increasing in complexity and accuracy.

1. The Kernel Integration Method (Point Dose)

This is the fastest method and is used during the preliminary design phase. It treats the shielding as a simple geometric shape (usually a sphere or a slab).

- **The Process:** The software takes the particle flux from an environment model (like AE9/AP9) and "transports" those particles through a specific thickness of aluminum.
- **The Math:** It uses **Dose-Depth Kernels**—pre-calculated tables that define how much energy is lost per millimeter of material.

Tool Example: SHIELDOSE-2.

Output: A curve showing Dose vs. Thickness. This tells you the "worst-case" dose for a component behind a specific shield.

2. Sector Shielding Analysis (Ray Tracing)

As discussed earlier, once you have a 3D CAD model of the satellite, you move to **Sector Analysis**. This is the standard methodology for modern spacecraft engineering.

- **The Process:** Instead of assuming a uniform sphere, the software shoots thousands of rays from a specific chip out into the 3D model.
- **The Calculation:**
    - For each ray (i), calculate the total path length and density of all materials it hits to find the **Areal Density** (ti).
    - Look up the dose (D) for that specific thickness (ti) from the SHIELDOSE-2 kernel.
    - Sum the doses from all rays (N) based on the solid angle (Ω) they represent:

$$D_{total} = \frac{1}{4\pi} \sum_{i=1}^{N} D(t_i) \Delta\Omega_i$$

Tool Example: FASTRAD, **SSAT (SPENVIS)**.

3. Monte Carlo Simulation (Particle Transport)

This is the most computationally expensive but most physically accurate method. It is used for complex missions (like Mars or Jupiter) or when secondary particles (like neutrons) are a major concern.

- **The Process:** Unlike Ray Tracing, which uses pre-calculated "averages," Monte Carlo simulates the life of **every single particle** individually.
- **The Physics:** It tracks a particle as it enters the satellite, bounces off atoms (scattering), creates secondary particles (Bremsstrahlung or spallation), and eventually stops or leaves.
- **The Result:** It captures physics that Ray Tracing misses, such as **backscattering** (radiation bouncing off a heavy internal component back into the chip) or **nuclear interactions**.
- **Tool Example: Geant4**, **MCNP**, **NOVICE**.

Summary: Which Methodology to Use

Methodology	Data Required	Speed	Best Use Case
Point Dose	Shield thickness	Seconds	Initial part selection & "ballpark" margins.
Sector Analysis	3D CAD Model	Minutes	Finalizing component placement & spot shielding.
Monte Carlo	Material Physics	Hours/Days	Deep space missions or sensitive science instruments.

The "Total Dose" Summation

Regardless of the method used, the final **Dose Computation** is the sum of three distinct contributors:

1. **Direct Ionizing Dose:** From electrons and protons.
2. **Bremsstrahlung Dose:** Secondary X-rays created when electrons slow down in the shield.
3. **Non-Ionizing Energy Loss (NIEL):** The dose contributing specifically to **Displacement Damage**.

2-3. Total dose testing:

Total Dose Testing is the experimental process used to verify how an electronic component will degrade over time under the steady "wear-out" of ionizing radiation. For most space missions, this specifically refers to **Total Ionizing Dose (TID)** testing.

The standard "Bible" for this process in the aerospace industry is **MIL-STD-883, Method 1019**.

1. The Radiation Source: Cobalt-60

To simulate years of space radiation in a few days, engineers use a **Gamma Source**, typically **Cobalt-60 (60Co)**.

- **Why Gamma?** Gamma rays provide a very uniform dose throughout the entire body of the chip, simulating the deep ionization caused by high-energy electrons and protons in space.
- **The Facility:** Parts are placed in a lead-shielded room (or a water-shielded pool) where the source is raised to expose the hardware.

2. The Test Setup: "Bias" is Critical

You cannot simply throw a chip into a radiation chamber while it's sitting in a box. It must be **Biased** (powered on).

- **Worst-Case Bias:** Most chips are more sensitive when they are powered on because the internal electric fields help "trap" the radiation-induced charges in the oxides.
- **The Load Board:** Engineers design custom circuit boards that power the chips and, in some cases, toggle their logic states during the entire irradiation process.

3. Step-Stress Testing Procedure

Testing is rarely done in one single shot. Instead, it follows a "Step-Stress" pattern:

1. **Pre-Rad Characterization:** Every electrical parameter (leakage current, timing, supply current) is measured to create a baseline.
2. **Irradiation Step:** The parts are exposed to a specific dose (e.g., 10 krad).
3. **Intermediate Testing:** The parts are removed and re-measured. Engineers look for **parameter drift**.
4. **Repeat:** This continues until the part either reaches the mission requirement (with margin) or suffers a **Functional Failure**.

4. Post-Radiation: The "Rebound" Effect

One of the most complex parts of TID testing is what happens *after* the radiation stops.

- **Annealing:** Some chips "heal" when the radiation stops as trapped charges leak out.

- **Reverse Annealing:** Some chips actually get **worse** after the radiation stops (often seen in interface states).
- **The 168-Hour Bake:** To simulate long-term space effects, Method 1019 often requires a "Burn-in" or "Bake" at 100∘C after irradiation to see if the chip fails during the recovery period.

5. High Dose Rate (HDR) vs. Low Dose Rate (LDR)

This is a critical distinction in the test report:

- **HDR (Standard):** Delivers the dose at 50–300 rad(Si)/s. This is fast and efficient for CMOS parts.
- **LDR (ELDRS Testing):** Delivers the dose at 0.01 rad(Si)/s. This is required for **Bipolar** parts (like op-amps) because they are often much more sensitive to slow radiation than fast radiation.

6. The Final Data Output

The output of a Total Dose Test is a set of **Drift Curves**. These curves are then handed to the circuit designers to perform the **Worst-Case Analysis (WCA)** we discussed earlier.

Parameter	Pre-Rad Value	Post-100krad Value	Drift %
Supply Current (Icc)	50 mA	85 mA	+70%
Output Voltage (Vout)	2.501 V	2.480 V	-0.80%
Propagation Delay	10 ns	14 ns	+40%

3. Radiation Hardness Assurance

3-1. Space standards & industrial approach:

Radiation Hardness Assurance (RHA) is the organized engineering process of ensuring that a spacecraft's electronics will perform as required throughout the mission lifetime despite the harsh radiation environment. It is the bridge between raw physics and mission success.

1. The RHA Life Cycle

In an industrial approach, RHA is not a single test, but a loop that follows the spacecraft development phases:

1. **Environment Definition:** Using models like **AE9/AP9** (for trapped particles) and **CREME96** (for cosmic rays) to define what the satellite will face.
2. **Part Selection:** Comparing mission requirements against known radiation data (databases like NASA's GSFC or ESA's ESCIES).
3. **Analysis:** Performing the **Sector Shielding Analysis** and **Worst-Case Analysis** to calculate the **Radiation Design Margin (RDM)**.
4. **Testing:** Conducting **RLAT** (Lot Acceptance) and **SEE** testing for any parts with "unknown" heritage.
5. **Design for Mitigation:** Implementing TMR, ECC, or spot shielding for any parts that don't meet the RDM > 2 requirement.

2. Space Standards (The Rules of the Road)

Standards ensure that every company uses the same "language" and safety factors.

Military and International Standards:

- **MIL-STD-883, Method 1019 (TID):** The global baseline for Total Ionizing Dose testing.
- **MIL-STD-750:** The standard for discrete semiconductors (transistors, diodes).

ECSS-Q-ST-60-15C (ESA): The European standard that defines exactly how to perform radiation shielding and analysis.

ASTM F1192: The standard guide for the measurement of Single Event Phenomena.

Quality Levels:

- **Class S (Space):** Fully "Rad-Hard" parts from the factory. Very expensive, long lead times, but highest reliability.

- **Class B (Military):** High quality but may require additional "upscreening" for radiation.
- **COTS (Commercial Off-The-Shelf):** Standard industrial parts (like those from a car or phone). Using these requires a massive RHA effort to prove they won't fail in orbit.

3. Industrial Approaches: NewSpace vs. Traditional

The industry is currently split into two philosophies regarding RHA:

The Traditional Approach (NASA, ESA, Large Prime Contractors)

- **Philosophy:** "Failure is not an option."
- **Method:** Use only **Qualified Manufacturers List (QML)** parts that are radiation-hardened by design (RHBD).
- **Margin:** Strictly requires **RDM > 2**.
- **Cost:** High ($100,000+ for a single flight processor).

The NewSpace Approach (SpaceX, Planet, SmallSat Startups)

- **Philosophy:** "Fail fast, iterate, and use redundancy."
- **Method:** Use high-performance **COTS parts**. Instead of buying one $100k "Rad-Hard" computer, they might fly three $1,000 industrial computers in a voting (TMR) configuration.
- **Testing:** They perform "Board-Level" testing (putting an entire finished board in the beam) rather than testing every individual transistor.

4. The Radiation Design Margin (RDM) Goal

For a mission to be "Approved," the industrial standard is to achieve an RDM of at least 2.0.

$$RDM = \frac{\text{Component Failure Threshold}}{\text{Predicted Mission Dose}} \geq 2$$

If the RDM is below 2, the "Industrial Approach" dictates a **Radiation Exception** or a **Mitigation Plan** (such as adding a tantalum shield or changing the circuit design).

5. Summary of RHA Deliverables

At the end of the RHA process, the engineer must produce these four documents for the launch authorities:

- **Radiation Environment Report:** What is the threat?
- **Radiation Analysis Report (RAR):** How does the shielding protect the chips?
- **Single Event Effects (SEE) Report:** How often will the system crash/reset?
- **The Approved Parts List (APL):** A list showing that every chip has been verified via testing or heritage.

3-2. Component qualification system:

In the space industry, **Component Qualification** is the rigorous sequence of tests used to prove that a specific part can survive the launch and the multi-year environment of space. It is the process that turns a "part" into a "flight-qualified component."

Engineers follow a hierarchical system to move from a raw industrial part to a space-rated asset.

1. The Qualification Levels

Not every part on a satellite needs the same level of scrutiny. The system is usually divided based on the mission's risk tolerance:

- **Level 1 (Class S/V):** Highest reliability. Every single part is tested. Used for multi-billion dollar missions (e.g., James Webb Telescope).
- **Level 2 (Class B/Q):** High reliability. Parts are tested in batches (lots). Standard for most military and communication satellites.
- **Level 3 (COTS/Industrial):** High-performance parts from the automotive or medical industry. These require "Upscreening"—a custom qualification campaign designed by the satellite builder.

2. The Qualification Flow (The "Test-as-you-Fly" System)

A typical qualification campaign follows a specific order, as one type of stress (like vibration) can make a part more susceptible to another (like radiation).

A. Visual and Mechanical Inspection

Before testing, parts undergo **External Visual Inspection** and **DPA (Destructive Physical Analysis)**. Engineers break open a sample of the parts to inspect the quality of the internal wire bonds and the silicon die itself.

B. Environmental Stress Screening (ESS)

- **Thermal Cycling:** Parts are cycled between extreme temperatures (e.g., −55°C to +125°C) hundreds of times to check for cracks in the packaging.
- **Burn-In:** The parts are powered on at maximum voltage and temperature for 168 hours to catch "infant mortality" failures.

C. Radiation Qualification (TID & SEE)

This is the most critical phase for electronics.

1. **TID (Total Ionizing Dose):** Verifies the long-term wear-out.
2. **SEE (Single Event Effects):** Uses a cyclotron to check for random bit-flips or latch-ups.

D. Mechanical Qualification

- **Vibration/Shock:** Simulates the violent forces of a rocket launch.
- **Vacuum/Outgassing:** Parts are placed in a vacuum chamber to ensure materials don't release gases that could fog up satellite lenses.

3. The Concept of "Heritage"

In the qualification system, **Heritage** is gold. If a specific part from a specific manufacturer has already flown on five successful missions, the "qualification" requirements may be reduced. However, if the manufacturer changes the "recipe" of the silicon, the heritage is lost, and the part must be re-qualified.

4. Summary: Industrial vs. Space-Qualified

Feature	**Industrial (COTS)**	**Space-Qualified (QML-V)**
Testing	Sample testing at factory	100% testing and traceability
Radiation	Unknown (requires testing)	Guaranteed (Rad-Hard by design)
Traceability	Limited (Date codes)	Full (Wafer-level tracking)
Cost	$5.00	$5,000.00

5. Final Approval: The PAD

The result of this system is the **Part Approval Document (PAD)**. This document contains all the test data, radiation reports, and inspection results. It must be signed by the Radiation Engineer, the Parts Engineer, and the Quality Manager before the part is allowed on the flight board.

3-3. Radiation analyses:

In the space industry, **Radiation Analysis** is the formal process used to determine if a satellite's electronics will survive the mission. It moves from broad orbital predictions to high-fidelity 3D simulations of the spacecraft's interior.

1. The Three Pillars of Radiation Analysis

A complete analysis package must address three distinct threats, each requiring a different mathematical approach.

A. Total Ionizing Dose (TID) Analysis

This predicts the long-term "wear-out" of electronics. The analysis calculates how many "rads" (radiation absorbed dose) each component will absorb over the mission life (e.g., 5 years).

- **Goal:** Ensure parts don't suffer from leakage current or threshold shifts that cause the system to drift out of specification.
- **The Math:** Typically uses **Dose-Depth Curves** integrated over the satellite's 3D geometry.

B. Displacement Damage Dose (DDD) Analysis

This focuses on physical damage to the crystal lattice of semiconductors, caused primarily by protons.

- **Goal:** Predict the "End-of-Life" efficiency for solar cells and the "dark current" (noise) in cameras/optical sensors.
- **The Math:** Uses **NIEL (Non-Ionizing Energy Loss)** scaling to convert proton flux into an equivalent displacement dose.

C. Single Event Effects (SEE) Analysis

This is a statistical probability analysis of "random" strikes (bit flips or latch-ups).

- **Goal:** Determine the **Error Rate** (e.g., "The system will have 1 bit-flip every 4 days").
- **The Math:** Convolves the orbital **LET Spectrum** (Linear Energy Transfer) with the component's **Weibull Curve** (sensitivity measured in a lab).

2. Methodology Levels

Analysis is performed in stages, becoming more accurate as the satellite design matures.

Level	Method	Tools	Accuracy
Level 1	**Slab/Sphere Model**	SHIELDOSE-2	Conservative (Worst-case)
Level 2	**Sector Analysis**	FASTRAD, SSAT	High (Uses real 3D CAD)
Level 3	**Monte Carlo**	Geant4, NOVICE	Highest (Tracks every particle)

3. The Analysis Workflow: From Orbit to Report

Step 1: Environment Modeling

The engineer inputs the orbit parameters (Altitude, Inclination) into models like **AP9/AE9** (for trapped particles) and **ESP/PSYCHIC** (for solar flares). This generates the "Free Space" radiation flux.

Step 2: 3D Shielding Evaluation (Sector Analysis)

The software "shoots" thousands of virtual rays from the center of a sensitive chip out through the satellite's CAD model. It calculates how much "free" shielding is provided by the aluminum frame, the battery, and other components.

Step 3: Dose Summation & Margin Calculation

The software combines the shielding data with the environment data to produce a **Sector Integrated Dose (SID)**. The engineer then compares this to the chip's known failure limit to find the **Radiation Design Margin (RDM)**.

$$RDM = \frac{\text{Component Test Limit}}{\text{Calculated Mission Dose}}$$

4. The Final Deliverable: The Analysis Report

At a **Critical Design Review (CDR)**, the results are summarized in a "Stoplight" table. Any part with an **RDM < 2.0** is flagged.

- **Green (RDM > 2):** Safe to fly.
- **Yellow (1 < RDM < 2):** Requires more shielding or a specialized "spot shield."
- **Red (RDM < 1):** The part will likely fail; it must be replaced with a harder version.