FAST CONVOLUTIONAL NETS WITH fbfft: A GPU PERFORMANCE EVALUATION

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ABSTRACT

We examine the performance profile of Convolutional Neural Network (CNN) training on the current generation of NVIDIA Graphics Processing Units (GPUs). We introduce two new Fast Fourier Transform convolution implementations: one based on NVIDIA's cuFFT library, and another based on a Facebook authored FFT implementation, fbfft, that provides significant speedups over cuFFT (over $1.5\times$) for whole CNNs. Both of these convolution implementations are available in open source, and are faster than NVIDIA's cuDNN implementation for many common convolutional layers (up to $23.5\times$ for a synthetic kernel configuration). We discuss different performance regimes of convolutions, comparing areas where straightforward time domain convolutions outperform Fourier frequency domain convolutions. Details on algorithmic applications of NVIDIA GPU hardware specifics in the implementation of fbfft are also provided.

1 Introduction

Deep convolutional neural networks (CNNs) have emerged as one of the most promising techniques to tackle large scale learning problems, whether in image and face recognition, audio and speech processing or natural language understanding. A convolutional layer within these networks provides useful properties such as translation equivariance of activations. A limiting factor for use of convolutional nets on large data sets was, until recently, their computational expense.

Krizhevsky et al. (2012) demonstrated that training of large CNNs with millions of weights and massive data sets is tractable when graphics processing units (GPUs) are properly put to use. Since then, renewed interest in CNNs insufflated a fresh breath in various frameworks and implementations, including Torch (Collobert et al. (2011a)), Theano (Bergstra et al. (2010)), cuda-convnet (Krizhevsky (2014)) and Caffe (Jia et al. (2014)). Many of these frameworks are based around codes for NVIDIA GPUs using CUDA (Garland et al. (2008)).

We discuss our contributions to convolution performance on these GPUs, namely using Fast Fourier Transform (FFT) implementations within the Torch framework. We summarize the theory behind training convolutional layers both in the time and frequency domain in Section 2. We then detail our implementations. The first is based on NVIDIA's cuFFT and cuBLAS libraries (Section 3). We evaluate our relative performance to NVIDIA's cuDNN library (Chetlur et al. (2014)) on over 8,000 different configurations (Section 4). We significantly outperform cuDNN and other time domain convolution implementations for a wide range of problem sizes.

Our second implementation is motivated by limitations in using a black box library such as cuFFT in our application domain, which we describe. In reaction, we implemented a from-scratch open-source implementation of batched 1-D FFT and batched 2-D FFT, called Facebook FFT (fbfft), which achieves over $1.5\times$ speedup over cuFFT for the sizes of interest in our application domain. This implementation achieves GPU efficiency ratios of over 75% in certain cases. We describe an ongoing effort to further improve the performance of our solution based on algorithmic tiling (Section 6) before we conclude. Our implementation is released as part of the fbcuda and fbcunn open-source libraries at http://github.com/facebook.

2 Convolution

Discrete convolution and cross-correlation are used in CNNs. We quickly summarize these and their implementation, with a formulation mirroring Mathieu et al. (2013). Forward propagation (fprop) inputs are a set f of input feature planes $x_i, i \in f$. These are cross-correlated with $f' \times f$ different filter kernel weights $w_{(j,i)}, j \in f', i \in f$, producing output feature planes $y_j, j \in f'$. Each input and output feature can be part of a minibatch S, so we have $x_{(s,i)}$ and $y_{(s,j)}, i \in f, j \in f', s \in S$:

$$y_{(s,j)} = \sum_{i \in f} x_{(s,i)} \star w_{(j,i)}$$

The feature planes f are *reduced* (summed) pointwise. For back-propagation (*bprop*), the gradient of the loss with respect to outputs are convolved with the kernels:

$$\frac{\partial L}{\partial x_{(s,i)}} = \sum_{j \in f'} \frac{\partial L}{\partial y_{(s,j)}} * w_{(j,i)}$$

Reduction is over f' here. Finally, the kernel weights are updated using the gradient of the loss with respect to the weights (accGrad):

$$\frac{\partial L}{\partial w_{(j,i)}} = \sum_{s \in S} \frac{\partial L}{\partial y_{(s,j)}} \star x_{(s,i)}$$

Reduction is over S here. For purposes of this paper, we use set symbols interchangeably to refer to their size: each input plane is a 2-D matrix of size $h \times w$, and each filter kernel is a 2-D matrix of size $k_h \times k_w^2$. The output planes $y_{(s,i)}$ are of size $(h-k_h+1) \times (w-k_w+1)$, and implement valid-only convolution, as per MATLAB terminology. Input zero padding and input mirror padding around the margins of the input (p_h, p_w) can be optionally added.³

A popular convolution implementation is to *unroll* the data until the computation is in the form of a large matrix multiplication (Chellapilla et al. (2006)). This is the strategy followed by many implementors, since matrix multiplication is a well-tuned linear algebra primitive available on virtually any platform. While it is possible to provide instances of direct calculation that are faster than matrix unrolling (*e.g.*, for large *S*, Krizhevsky (2014)), it is challenging to provide an implementation that is faster for more than just a small subset of possible convolution problems.

Introducing strides in this form of convolution (i.e., performing the convolution at every d_h, d_w -th offset) is a popular way to reduce the computational cost at the expense of precision. The memory accesses required are very similar but with fewer reuse opportunities. On the other hand, by the convolution theorem, a convolution of two discrete signals can be performed with lower asymptotic complexity by performing the multiplication in the frequency domain. Applied to the forward pass, it becomes:

$$y_{(s,j)} = \sum_{i \in f} x_{(s,i)} \star w_{(j,i)} = \sum_{i \in f} \mathcal{F}^{-1} \left(\mathcal{F}(x_{(s,i)}) \circ \mathcal{F}(w_{(j,i)})^* \right)$$

where * denotes complex conjugation and \circ is the pointwise product. The discrete Fourier basis used is the largest of the two components convolved and the output. Linearity of the DFT allows one to perform the sum above in the Fourier domain if desired. Applying the FFT then yields a $\mathcal{O}(Sff'n^2 + (Sf + ff' + Sf')n^2\log n)$ procedure in lieu of the original $\mathcal{O}(Sff'n^2k^2)$, $n = h = w, k = k_h = k_w$. Similar transformations apply for the other two passes. We call this a frequency domain convolution, in contrast to time domain convolution via direct computation.

¹Torch practice is that the forward pass is cross-correlation, hence the ★.

²2-D can be extended to n-D, $n \ge 1$.

³Input size $(h + p_h) \times (w + p_w)$, output size $(h + p_h - k_h + 1) \times (w + p_w - k_w + 1)$.

 $^{^4(}h \times w)$ -dimensional or even bigger for performance (Section 3.2).

Strided convolutions via FFT can be implemented efficiently to obtain good performance Brosch & Tam (2015). We do not consider those in this paper.

CUFFT CONVOLUTION IMPLEMENTATION

In this section we discuss implementation strategies using the NVIDIA cuFFT libraries and their efficiency.

3.1 FFT CONVOLUTION DETAILS

We described the general formulation for the three types of convolutions in section 2. Here, we borrow the Torch naming convention: input for $x_{(s,i)}$; weight for $w_{(j,i)}$; output for $y_{(s,j)}$; gradOutput for $\partial L/\partial y_{(s,j)}$; gradInput for $\partial L/\partial x_{(s,i)}$; and gradWeight for $\partial L/\partial w_{(j,i)}$. All are stored as singleprecision floating point 4-D tensors in row-major layout, and are stored in memory using the socalled BDHW format. This is explicit in the expression $In_{S \times f \times h \times w}$, with input image row data as the *innermost* or *most varying* dimension.

Table 1 describes the in-order operations for FFT computation of the forward pass, using the FFT2D and IFFT2D operators and Comm matrix multiplication. Similar implementations follow for the other two passes. The G prefix denotes gradients. The F suffix denotes \mathbb{C} -valued frequency domain tensors; the rest are over \mathbb{R} . The T suffix denotes transposed tensors.

Table 1: Implementation detail for forward propagation

INPUT		OUTPUT
$In_{S \times f \times h \times w}$ $Wei_{f' \times f \times k_h \times k_w}$	$ \begin{array}{c} FFT2D \\ \hline FFT2D \\ \hline Trans2D \end{array} $	$InF_{S\times f\times (h+p_h)\times (\lfloor\frac{w+p_w}{2}\rfloor+1)}$ $WeiF_{f'\times f\times (h+p_h)\times (\lfloor\frac{w+p_w}{2}\rfloor+1)}$
$InF_{S \times f \times (h+p_h) \times (\lfloor \frac{w+p_w}{2} \rfloor + 1)}$ $WeiF_{f' \times f \times (h+p_h) \times (\lfloor \frac{w+p_w}{2} \rfloor + 1)}$	$\xrightarrow{Trans2D}$	$InFT_{(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)\times S\times f}$ $WeiFT_{(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)\times f'\times f}$
$\begin{cases} InFT_{(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)\times S\times f} \\ WeiFT_{(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)\times f'\times f} \end{cases}$ $OutFT_{(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)\times S\times f'}$	$\xrightarrow{\text{Cgemm}}$ $\xrightarrow{Trans2D}$	$OutFT_{(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)\times S\times f'}$ $OutF_{S\times f'\times(h+p_h)\times(\lfloor\frac{w+p_w}{2}\rfloor+1)}$
$OutF_{S\times f'\times (h+p_h)\times (\lfloor \frac{w+p_w}{2}\rfloor+1)}$	$\xrightarrow{IFFT2D}$	$Out_{S\times f'\times (h-k_h+1)\times (w-k_w+1)}$

Exact tensor dimensions are also given above. By taking advantage of the Hermitian symmetry property of the 2-D DFT for R-valued inputs we only store about half the complex entries; the remaining can be obtained by complex conjugation. This results in array sizes such as $\lfloor \frac{w+p_w}{2} \rfloor + 1$. We also perform interpolation by zero-padding, which serves multiple purposes. First, it is necessary to handle boundary conditions.⁵ Second, it is required to interpolate all operands over the same Fourier basis.⁶ Finally, padding has an impact on the FFT algorithm used in practice, as well as on the floating point operation count of non-FFT operations (Section 3.2).

Following the conversion into frequency domain, we perform transpositions to prepare the tensors for Cgemm matrix multiplication library calls. The transposition converts the BDHW layout into HWBD. The transposition is currently out-of-place and implemented using the Cgeam routine; we are also considering our own, in-place transposition routine. Cgemm library calls are performed on transposed tensors in the frequency domain. Casting the operation as a Cgemm call allows us to benefit from the heavily tuned cuBLAS routine. Eventually, we transpose the result back into the BDHW format and perform a 2-D inverse FFT. At this point, the resulting real tensor, always

⁵In this case, we typically have $p_h = \lfloor \frac{k_h}{2} \rfloor$ and $p_w = \lfloor \frac{k_w}{2} \rfloor$. ⁶All tensors are zero-padded to $(h+p_h) \times (w+p_w)$ before FFT2D.

 $(h+p_h)\times (w+p_w)$, is clipped to the appropriate final size: $(h-k_h+1)\times (w-k_w+1)$ for fprop, $h\times w$ for bprop, $k_h\times k_w$ for accGrad.

3.2 CUFFT DESIGN SPACE

We now discuss implementation aspects we explored. Multiple factors influence the computational efficiency of FFTs: transform size n, n's prime factor decomposition, and whether batched or iterated single transforms are applied. In the deep learning domain, it is commonplace to deal with small sizes, $n \neq 2^k$. If n has undesirable properties, efficiency can drop by an order of magnitude.⁷

cuFFT implements FFTs with the ubiquitous Cooley-Tukey algorithm (Cooley & Tukey (1965)) which takes advantage of trigonometric equalities to recursively decompose and reuse computations. This is further discussed in the Supplement. Decomposition is built on specialized kernels of fixed sizes which correspond to the prime factor decomposition of n. cuFFT implements specialized building blocks for radix sizes 2,3,5,7, and for sizes n where 4|n, it can use more efficient kernels exploiting the conjugate symmetry property. When n does not admit a prime factor decomposition using those radices only, the expensive Bluestein algorithm is used (Bluestein (1970)). Because our results are used in the time domain, we can in fact zero-pad the image and kernel to perform the FFT at any larger size that may be handled more efficiently. Exploiting more efficient, larger sizes should be balanced against the extra cost introduced in the subsequent transposition and matrix multiplication steps. Table 4's last case is one in which the best tradeoff is not easily guessed. cuFFT also has batched mode optimizations when multiple FFTs of the same size are being performed.

3.3 CUBLAS DESIGN SPACE

The cuBLAS library also comes with different implementations for batched and single operation modes. We had the choice between 3 implementation options:

- for larger batches over small matrices, the cublasCgemmBatched library call;
- for smaller batches over larger matrices, multiple cublasCgemm calls from the host;
- for intermediate batch and matrix sizes, devices of compute capability 3.5 and higher support dynamic parallelism which allows CUDA kernels to launch other kernels. This can be beneficial for many launches over small matrices.

Note that the discussion above applies to multiplications after transposition. So the matrix size is either $S \times f$, $S \times f'$ or $f \times f'$ and the number of such matrices is $h \times w$. Vendor libraries are usually optimized for throughput and not latency, so we expect it to be more efficient for larger sizes along critical dimensions (i.e., image size for the batch case and $S \times f$, $S \times f'$ or $f \times f'$ for the multiple kernel case). Due to build system limitations we were not able to experiment with the dynamic parallelism strategy; we leave this for future work.

At the system level, we use CUDA streams and buffering of all CUDA resources and intermediate buffers to remove synchronization points across convolutions. We are mindful of memory consumption; to address this we keep one single buffered copy of each type of tensor involved. This behavior is tailored for a bulk synchronous execution of layers on a GPU and is not adapted for multiple asynchronous convolutions on the same GPU. The buffers are automatically expanded as required and reused as much as possible.

3.4 AUTOTUNING

We combine the above implementation with a simple autotuning strategy. We devise a strategy selection mechanism that runs once for each problem size and caches the fastest strategy out of a few dozen for later reuse. The autotuning strategy explores different possible Fourier basis sizes that can be decomposed in powers for which cuFFT has an efficient implementation. In other words, for an FFT dimension of size n, we explore the sizes $i \in [n, 2\lfloor \log_2 n \rfloor]$ where $i = 2^a 3^b 5^c 7^d$. When the input size is a power of 2, the search space is reduced to a single point. In addition to Fourier basis sizes, we weigh in various cuBLAS calls and asynchronous modes.

⁷http://docs.nvidia.com/cuda/cufft/index.html#accuracy-and-performance

4 CUFFT CONVOLUTION PERFORMANCE

4.1 Performance versus cuDNN: 8,232 configurations

We compare our cuFFT convolution results against NVIDIA's cuDNN 1.0 library (Chetlur et al. (2014)), which contains one of the fastest, general purpose convolution methods for the GPU, using matrix unrolling. It has decent performance for many problem sizes thanks to heavy autotuning of cuBLAS codes for different problems. It is a strong baseline for this reason.

Image CNNs to date have for the most part used square input images and filters, though rectangular filters are valid for other problems (notably text CNNs, Collobert et al. (2011b)). Thus, we restrict ourselves to a 5-D problem domain $\{S, f, f', n(=h=w), k(=k_h=k_w)\}$. Much of this space is not used in practice. Some areas are perhaps over-emphasized (large S, small k) due to current engineering concerns. We evaluate cuDNN vs cuFFT-based convolution for Table 2's 8,232 configurations.⁸

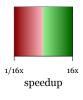
Table 2: Configuration elements evaluated

DIMENSION	SIZES EVALUATED
Minibatch size (S)	1, 16, 64, 128
Input filters (f)	1, 4, 16, 64, 96, 128, 256
Output filters (f')	1, 4, 16, 64, 96, 128, 256
Kernel h/w $(k = k_h = k_w)$	3, 5, 7, 9, 11, 13
Output h/w $(y = h - k_h + 1 = w - k_w + 1)$	1, 2, 4, 8, 16, 32, 64

Figures 1-6 are performance summaries of cuFFT convolution versus cuDNN on a NVIDIA Tesla K40m, averaged across all three passes. The y-axis problem size corresponds to the minibatch size multiplied by number of input and output planes (Sff'); each one of these is a pass reduction dimension. Many possible combinations of S, f, f' may map to the same problem size. cuDNN performance varies to a greater degree than cuFFT across passes. This is due to the asymmetry of convolution sizes in each pass, and the fact that a larger convolution kernel (as seen with gradient accumulation) is essentially free in the Fourier domain. Averaging the three passes together provides a proxy for overall performance. The x-axis corresponds to output height/width. For deeper layers in image CNNs, output size will decrease while f, f' will increase, so depth corresponds to moving from the upper right to the lower left of the graph. Black areas in the chart are due to failed cuFFT runs, due to memory pressure or undetermined potential cuFFT 6.5 issues.

FFT convolutions make large kernel sizes inexpensive, which make the performance of all three passes roughly equal (Table 4). On the other hand, zero-padding $k_h \times k_w$ to $h \times w$ penalizes smaller kernels compared to cuDNN. For 3×3 kernels (Figure 1), cuFFT performance is poor compared to cuDNN. The overhead of multiple kernel launches, streaming memory in and out multiple times, and zero-padding to the input size often outweigh the algorithmic advantage of FFT. However, for the largest problem sizes, 3×3 convolution via FFT can still be advantageous, with top speed 1.84×6 faster than cuDNN. 5×5 kernels (Figure 2) show an increasing dominance of the FFT strategy, with top speed 5.33×6 faster. The tendency is confirmed for larger kernel sizes: at 13×13 , maximum speedup is 23.54×6 over cuDNN.

⁸Parameterized on output rather than input size h, w because the implied $h = y + k_h - 1, w = y + k_w - 1$ will be valid for any choice of k_h, k_w .



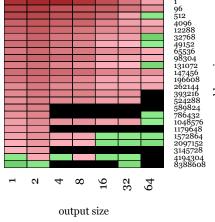
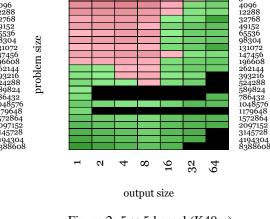


Figure 1: 3×3 kernel (K40m)



problem size

Figure 2: 5×5 kernel (K40m)

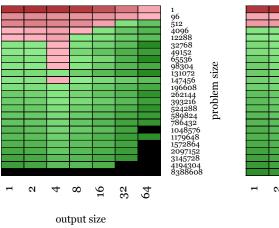


Figure 3: 7×7 kernel (K40m)

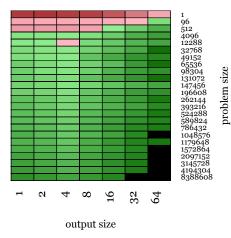


Figure 4: 9×9 kernel (K40m)

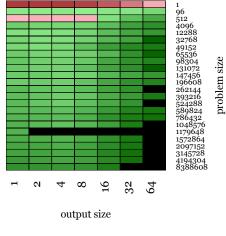


Figure 5: 11×11 kernel (K40m)

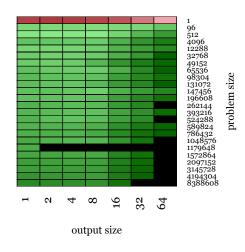


Figure 6: 13×13 kernel (K40m)

4.2 CNN PERFORMANCE

In table 3, we show performance for real CNNs, AlexNet (Krizhevsky et al. (2012)) and OverFeat *fast* (Sermanet et al. (2014)), comparing against cuDNN and cuda-convnet2 (ccn2) kernels in Torch. The first layer uses cuDNN for the cuFFT runs because it is strided, but all other layers use cuFFT. The timings include all convolutional layers of the network.

NETWORK	KERNEL	FPROP	BPROP	ACCGRAD	TOTAL
AlexNet	cuFFT cuDNN ccn2	94.34 147.32 99.03	96.69 167.79 104.59	93.20 153.96 103.29	284.23 469.07 306.91
OverFeat fast	cuFFT cuDNN ccn2	375.65 459.06 433.11	460.48 634.26 398.87	397.85 508.02 450.82	1233.98 1601.35 1282.80

Table 3: AlexNet and OverFeat fast performance (K40, ms)

Table 4 shows the performance of the cuDNN and our cuFFT convolution implementation for some representative layer sizes, assuming all the data is present on the GPU. Our speedups range from $1.4\times$ to $14.5\times$ over cuDNN. Unsurprisingly, larger h,w, smaller S,f,f',k_h,k_w all contribute to reduced efficiency with the FFT. More surprisingly, we experience noticeable speedups on small 3×3 kernels as long as the input tensor remains of small size. The optimal FFT sizes that autotuning finds are reported in columns 2 and 3; note L5 padding being found by the autotuner. Column 7 has the trillion equivalent time-domain reductions per second (single-precision floating point multiply-adds) achieved by our implementation on a NVIDIA Tesla K40m on CUDA 6.5. This number represents the throughput a time-domain kernel needs to achieve in order to match our implementation; it is computed as $(Sff'k_hk_w(h-k_h+1)(w-k_w+1))/time$. This is a metric to compare relative efficiency across problem and padding sizes. In the cases L2, L3 and L4, a time domain convolution would need to exceed the K40m peak of 4.29 Tflop/sec in order to match our throughput.

5 fbfft Implementation

This section presumes familiarity with GPU architecture. Refer to the Supplement for details.

When designing high-performance libraries, multiple objectives must be balanced against each other: memory latency/bandwidth tradeoffs, maximizing locality without sacrificing too much parallelism, good instruction mix, register usage and mapping strategy of computation and data to memories and compute elements. A key principle is to design a set of leaf kernels with well-tuned in-register performance and reduce the larger problem to a combination of these kernels by data and loop tiling (Irigoin & Triolet (1988)) and recursive decompositions (Gunnels et al. (2001)). Since vendors have to sustain high performance for a large class of application domains, there exist parameter configurations for which a carefully tuned approach significantly outperforms vendor-tuned libraries (Shin et al. (2010)). For common deep learning use, convolutional layers consist of many batched small 2-D convolutions. These are tiny relative to DSP and HPC standards and put us in a regime where (a) we fall outside of the highly tuned regime, (b) feature dimensions are often smaller than GPU warp sizes and can often fit exclusively in registers rather than in shared memory (SMEM), and (c) we are very sensitive to latencies. We determined that it is possible to obtain better efficiency than the existing batched cuFFT mode for CNNs.

5.1 LIMITATIONS OF CUFFT

Because the cuFFT library is a black box, zero-padding⁹ has to be explicitly embedded in the input and output arrays. The consequence is that one may need to allocate a duplicate, larger memory

⁹This is different from the FFTW compatibility padding mode for in-place transforms.

LAYER	$h + p_h$	$p_h w + p_w \textbf{cuDN}$		cuFFT	SPEEDUP	TRED/s
L1	Doroma	f _ 9 f/	- 06 b - au -	_ 190 <i>l</i> a _	<i>l</i> ₂ = 11	
			= 96, h = w =			0.0
fprop	128	128	$125.11 \ ms$		$1.54 \times$	0.9
bprop	128	128	$153.39 \ ms$	$66.49 \ ms$	$2.30 \times$	1.1
accGrad		128	$155.07\ ms$			1.05
$\overline{L2}$ = = =	Params:	$\overline{f} = \overline{64}, \overline{f'}$	$\overline{=64, h} = \overline{w}$	$=64, \overline{k_h}=$	$k_w = 9$	
fprop	64	64	$354.83 \ ms$	$46.44\ ms$	$7.64 \times$	7.49
bprop	64	64	$579.37 \ ms$	$46.25\ ms$	$12.5 \times$	7.52
accGrad	64	64	$416.34\ ms$	47.03~ms	$8.85 \times$	7.40
$\overline{L3}$ – – –	Params:	$\overline{f} = \overline{128}, \overline{f}$	$\overline{h} = \overline{128}, \overline{h} = \overline{128}$	$\overline{w} = \overline{32}, \overline{k_h}$	$=\overline{k_w}=9$	
fprop	32	32	$130.89 \ ms$	$17.77\ ms$	$7.36 \times$	9.90
bprop	32	32	$245.57 \ ms$	$16.97\ ms$	$14.5 \times$	10.37
accGrad	-	32	$154.96\ ms$			10.34
<u>L</u> 4 – – –	Params:	$\overline{f} = \overline{128}, \overline{f}$	$\overline{h} = \overline{128}, \overline{h} = \overline{128}$	$\overline{w} = \overline{16}, \overline{k_h}$	$= k_w = 7$	
fprop	16	16	15.13~ms	4.88~ms	$3.10 \times$	5.54
bprop	16	16	20.80~ms	4.71~ms	$4.41 \times$	5.76
accGrad	16	16	18.17~ms	4.70~ms	$3.86 \times$	5.75
<u>L5</u> – – –	Params:	$\overline{f} = 384, \overline{f}$	$\overline{b}' = 384, \overline{h} = 0$	$\overline{w} = \overline{13}, \overline{k_h}$	$=\overline{k_w}=3$	
fprop	13	14	$39.82 \ ms$	21.35~ms	$1.86 \times$	1.34
bprop	13	14	$28.33\ ms$	$20.22\ ms$	$1.40 \times$	1.42
accGrad	13	14	$47.84\ ms$	$21.26\ ms$	$2.25 \times$	1.35

Table 4: Representative layer performance (S = 128, K40m)

region (only once) and copy data from non-padded tensors to padded tensors. This memory consumption and spurious copies affect latency significantly. Instead, we devised an implementation for batched 1-D FFT and 2-D FFT of sizes 2-256 and *reaches up to 78% efficiency at 97.5% occupancy*. We also implemented an IFFT kernel based on our FFT kernel.

In our implementation we use *clipping* to conditionally load a value if reading within bounds or a constant (0) otherwise. This is an approach used in automatic code generation tools such as Halide (Ragan-Kelley et al. (2013)) and relies on aggressive if-conversion properties of the CUDA compiler. It allows for more efficient control flow rather than using explicit loop prologues and epilogues. This mechanism does not require any additional memory allocation and is zero-copy; this is particularly desirable in the latency sensitive mode.

Additionally, since cuFFT and cuBLAS are closed source, it is impossible to take advantage of algorithmic simplifications that may be available. For instance, in the forward pass of our computation as shown in Table 1, the result of the first cuFFT call is of the form $S \times f \times (h+p_h) \times (\lfloor (w+p_w)/2 \rfloor +1)$. With fbfft we return it in the form $S \times f \times (\lfloor (w+p_w)/2 \rfloor +1) \times (h+p_h)$ where the two innermost data dimensions are transposed. This allows us to remove a full data transposition from each of the FFT kernels. Another domain-specific optimization we have yet to explore is eliminating bit reversal portions of the FFT and IFFT. This can be done by performing the FFT with *decimation in frequency* (DIF) and the IFFT with *decimation in time* (DIT), discussed in the Supplement.

5.2 Warp-level 1-D FFT and 2-D FFT for size $n \le 32$

For batched FFT of power of two sizes we view a single warp as a small distributed system with lockstep collective communication capabilities and we program it in a bulk-synchronous fashion (Valiant (1990)). We implement DIF and enforce the following invariants for the $\log_2 n$ steps:

- each warp thread originally loads one real element of the input vector and locally computes one complex twiddle factor (i.e. a root of unity);
- at each step, all warp threads exchange data with another thread in the warp in parallel and produce a new value;

 then, all warp threads exchange twiddle factors with another thread in the warp in parallel, and produce a new value.

The two bulk-synchronous exchanges can be written each with one warp-wide instruction. After the $\log_2 n$ steps, the FFT is computed and stored in a distributed and bit reversed manner within 1 register across a warp. For sizes $n \leq 32$, bit reversal can be implemented with a single warp shuffle.

We either load twiddle factors from device memory or compute them with the sincosf function only once, and subsequently swap them within registers. This greatly reduces the reliance on either memory bandwidth or on the special functional unit at the expense of a few additional registers. The decision between explicitly loading twiddle factors from device memory or computing them is a tradeoff between arithmetic intensity and memory bandwidth. For sizes 16 and 32 the arithmetic pipeline is the bottleneck. Loading twiddle factors from memory for these two special sizes results in a performance increase of 15% and 20% respectively.

The discussion above applies to 1-D FFT and to each independent FFT within a larger 2-D FFT. A n-D Fourier transform is separable and can be implemented with sets of multiple 1-D FFT with transpositions between each of these sets. In 2-D FFT \mathbb{R} -to- \mathbb{C} , the first set comprises n FFTs and the second set comprises n/2+1 FFTs by Hermitian symmetry. Following standard techniques Lyons (1996) we further pack 2 real FFTs into a single complex FFT . The extra 1 term in the quantity n/2+1 makes the computation ill-balanced and can bring down performance by lowering occupancy. We chose to dimension our kernels to have size $n \times (n/2)$ and introduce additional control flow to handle the border case. This results in 30% additional performance. We implement the transposition in SMEM across warps following Ruetsch & Micikevicius (2009). Data is already resident in registers so our main concerns are limiting SMEM usage to keep occupancy high, and limiting load/stores by using vector instructions to avoid saturating the load-store unit (LSU).

5.3 1-D FFT and 2-D FFT for size $32 < n \le 256$

With size 32 as our building block, we extend our strategy to larger sizes. We use the same single warp approach to compute a full 1-D FFT. The main difference is that the computation is now distributed across multiple registers across threads in a warp ($\lceil n/32 \rceil$ Fourier coefficients and twiddle factors in registers per thread). Because we perform a full FFT per warp, a performance cross-over where cuFFT wins happens after register usage limits occupancy too much. We outperform 1-D cuFFT for $n \le 256$, with a hard register limit at n = 512 (128 and 256 similarly for 2-D FFT). This is still well within our application domain. The following modifications handle multiple registers per thread:

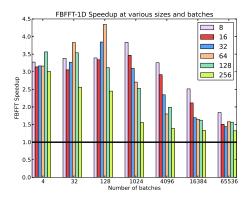
- Hermitian symmetry allows us to perform half the computation. There is a tradeoff between adding control-flow divergence and performing less work. At n ≥ 64, benefits from reduced computations dominate divergence losses;
- we take advantage of trigonometric symmetries and twiddle factor distribution to compute only a fraction of the roots of unity needed for each FFT, distributed with register to register copies;
- twiddle factor re-balancing across a warp and across registers requires a different implementation. We managed to implement it fully within registers;
- bit reversal occurs across registers and across warps. The high-order bits represent the register while the low-order bits represent the warp. Without a sophisticated implementation, this results in indirect addressing of registers which is costly. We implement a simple bit reversal in SMEM, which is an occupancy bottleneck at $n \ge 256$ for 1-D FFT.

In the 2-D FFT case, the intermediate transpose becomes significantly more expensive. We experimented with various strategies to keep occupancy high, including partial transpositions within a warp to use minimal amounts of SMEM.

5.4 DISCUSSION

We report the relative performance of our implementation fbfft compared to cuFFT for various batch and input sizes of interest. The number of batches to consider depends on the dimension of

CNN layers as well as any multi-GPU parallelization strategy that may be involved. At typical sizes of interest, fbfft is between $1.5 \times$ and $5 \times$ faster. We tried up to 4 million batches and at larger sizes gains stabilize around $1.4 \times$ but efficiency goes down as more and more memory is used.



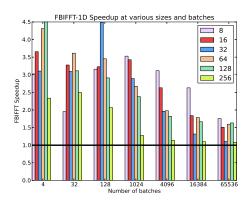
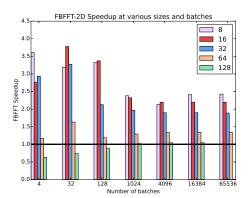


Figure 7: fbfft-1D FFT and IFFT (K40m, cuFFT 6.5 @ 1x)



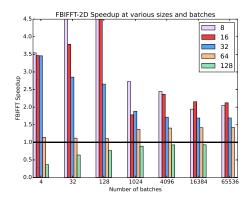


Figure 8: fbfft-2D FFT and IFFT (K40m, cuFFT 6.5 @ 1x)

Figure 7 shows the performance in the 1-D case. These numbers do not exercise our implicit zero-copy padding, so we expect additional gains when we incorporate our FFT in the convolution. Our implementation outperforms cuFFT for all cases of interest, more dramatically so for smaller batch sizes. Small batch sizes also correspond to the latency sensitive regime in Figures 1-6 for which the cuFFT based implementation performs quite worse than cuDNN. We achieve 78% efficiency at 97.5% occupancy for size 64 at batch size 16,384, as reported by nvvp.

Figure 8 shows the performance in the 2-D case. Relative performance gains for sizes 64 are more modest than in the 1-D case, even losing to cuFFT at size 128 and small batch sizes. The magnitude of the relative gains at various batch sizes drops faster than in the 1-D case. Looking at the performance of the 32×32 FFT, we obtain $1.6 \times$ speedup over cuFFT at 1,024 batches. The same ratio is not obtained until 16,384 batches in 1-D FFT. When coupled with the tiling strategy in Section 6, we emphasize that the sizes of interest are actually 8-64, and depend on k_h, k_w but not input h, w. Batch sizes can vary on the whole spectrum.

We interfaced fbfft into our convolution module and ran experiments with 3×3 kernels for the 3 different convolution passes over inputs of sizes $x=h=w, x\in\{13,16,27,32,57,64\}$. For problem size, we used $p=S=f=f', p\in\{16,32,64,128\}$. By swapping our FFT implementation we observed an overall mean speedup of $1.51\times$ with standard deviation 0.21 and geometric mean $1.49\times$. The minimum speedup was $1.21\times$, despite sometimes performing more computations

¹⁰This is not unexpected because these two computations perform the same number of flops when accounting for Hermitian symmetry, plus the fact that the efficiency of cuFFT increases while fbfft remains high but almost constant.

with fbfft which can only interpolate to a power of 2. These experiments exercise the zero-copy padding and lower memory footprints of fbfft compared to cuFFT but do not yet reflect additional optimizations such as tiling and bit twiddling elision.

6 CURRENT LIMITATIONS AND FUTURE WORK

In our current implementation, fbfft heavily relies on shuffle instructions. In spite of a good efficiency, we only utilize 60% of the available memory bandwidth. This is due to the load and store instructions in our kernel competing with the shuffle instructions for the Load-Store Unit (LSU). As a consequence, our first bottleneck is the number of instructions issued on the LSU. For instance, on Kepler (capability 3.5), the throughput for 32-bit floating point multiply-add operations is 192 per cycle but the throughput for shuffles is only 32. In the future we will investigate and release faster implementations as they become available.

Temporary memory overhead requirements are a common issue when performing convolutions in the Fourier domain. In this first implementation, we introduced the following memory buffers to support our implementation:

- for each of input, output and weight tensors we store 1 buffer for the frequency array and 1 buffer for its complex transpose. These buffers store the Fourier representation and are generally limited by the weight tensor which is independent of the mini-batch size. Because of the global memory pressure we introduce, we reuse buffers at each layer and pass on the opportunity to (1) reuse 2 FFT results in each hidden layer, reducing the cost of forward FFTs by 33%; and (2) asynchronously precompute FFTs of the weight tensors and their gradients to better fill the gpu utilization pipeline,
- when using cuFFT we additionally pad the input, weight and output tensors explicitly to the best performing common fft size
- when using cuFFT additional temporary memory is reserved by each cufftPlan
- with fbfft padding is implicit but and no temporary memory buffer is needed until we reach size 64. On the other hand, fbfft only supports square convolutions whose size is a power of 2. As a consequence, too much padding could occur and adversely affect both performance and memory consumption. The tiling strategy we describe next is a good way to circumvent the problem.

Additionally, we recently developed an in-place transposed batched CGEMM which permits the removal of the complex transposed buffer. For this problem, a tool like MaxAS Lavin (2015) could be valuable.

fbfft provides the most gains over cuFFT at sizes 8-64. A tiling strategy for the input can be used to exploit this advantage. When the kernel is significantly smaller than the input, we can decompose a large convolution into several smaller ones. For simplicity, we consider 1D convolution on a single input plane, as it can trivially be extended. Let x be an input of size n, c a kernel of size w and $y = x \star c$. We write $x_{[i,j]}$ for the vector formed by contiguous elements of x: $\{x_i, x_{i+1}, ..., x_{j-1}\}$. Let $d \leq n$. From the definition of the convolution, we have:

$$y_{[i,i+d]} = x_{[i,i+d+w]} \star c$$

So the convolution of the input of size n can be computed with $\lfloor n/d \rfloor$ convolutions with inputs of size d+w. The cost of the convolution goes down from $\mathcal{O}(n\log(n))$ to $\mathcal{O}(\lfloor n/d \rfloor(d+w)\log(d+w)) = \mathcal{O}((n+w/d)\log(d+w))$. From this formula, we see that the optimal d is of the order of w, to get the complexity $\mathcal{O}(n\log(w))$. This strategy allows us to speed up forward and backward propagation. Tiling can also be used to reduce memory cost for temporary storage by not running all the tiles in parallel (just the tiles which do run in parallel need their scratch space), at the potential expense of parallelism or efficiency.

For the gradient accumulation, we cannot reuse this strategy, since it involves a larger convolution between an input x of size n and a kernel $z=\frac{\partial L}{\partial y}$ of size n-w+1. However, we have a similar formula:

$$\left(\frac{\partial L}{\partial c}\right)_j = \sum_{i=0}^{n-1} x_{j+i} \cdot z_i = \sum_{k=0}^{\lfloor n/d \rfloor - 1} \sum_{i=0}^{d-1} x_{j+i+kd} \cdot z_{i+kd} + \sum_{i=d \lfloor n/d \rfloor}^{n-1} x_{j+i} \cdot z_i$$

And so

$$\left(\frac{\partial L}{\partial c}\right) = \sum_{k=0}^{\lfloor n/d\rfloor-1} x_{[dk,(d+1)k+w-1]} \star z_{[dk,(d+1)k]} + x_{[d\lfloor n/d\rfloor,n]} \star z_{[d\lfloor n/d\rfloor,n-w+1]}$$

We have a few other optimizations that are planned as well. Since much of the data we have is already available in registers or in shared memory, we are implementing our own in-place, in-register transpose via recursive decomposition. The pointwise multiplications in the Fourier domain, especially with tiling, are rather small, so our own matrix multiplication routines integrated with the rest of the convolution kernel code might win over cuBLAS, and prevent the need for multiple CUDA kernel launches and their associated overhead. Finally, as mentioned earlier, bit reversal portions can be eliminated with the FFT using DIF and the IFFT using DIT.

7 CONCLUSION

To summarize, we achieve significant gains in CNNs using FFTs, with a cuFFT convolution implementation achieving $1.4 \times -14.5 \times$ speedups over cuDNN for common sizes. In reaction to cuFFT and cuBLAS limitations in the context of our specific application domain, we developed our own FFT implementation, fbfft, which is more suited to deep learning problem sizes (large batches, small feature planes). fbfft itself is $\geq 1.4 \times$ faster than cuFFT transforms for these problems of interest. For convolution, it is faster than the cuFFT as well, with a mean of $1.51 \times$ for sizes that we wish to exploit.

Given our new efficient primitive for size 8-64 convolution, we are continuing work on bit twiddling, transposition and pointwise multiplication optimizations, and continuing work on tiling to make the computational advantage at that size apply to larger convolution problems. These will all allow for reduced training time and use of ever larger and deeper CNNs.

ACKNOWLEDGMENTS

We would like to thank Julien Demouth from NVIDIA who suggested further improvements are still possible by virtue of the current implementation being LSU throughput-bound rather than memory-bound.

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8 SUPPLEMENT

8.1 CUFFT CONVOLUTION PERFORMANCE BREAKDOWN

We show a breakdown of cuFFT convolution performance for the steps indicated in Table 1. The timings do not add up to 100% of the reported performance in the previous table because we do not report additional copies needed for zero-padding here. We also enforce force extra synchronizations to isolate the contribution of each operation. Abstracting from these details, the FFT and IFFT take up a significant amount of compute resources, which we address in Section 5.

Table 5: cuFFT convolution performance breakdown (K40m, ms)

LAYER	FFT A	TRANS. A	FFT B	TRANS. B	CGEMM	TRANS. C	IFFT C
L1							
fprop	0.86	0.24	1.13	0.32	15.13	12.67	36.46
bprop	0.86	0.24	34.55	10.26	12.62	0.39	1.19
accGrad	1.14	0.32	34.60	10.26	12.37	0.26	0.91
$-\overline{L}\overline{2}$							
fprop	2.99	0.98	5.91	2.03	8.92	1.67	6.24
bprop	2.99	0.98	5.92	2.03	8.85	1.67	6.23
accGrad	5.94	2.04	5.93	2.02	8.38	0.83	3.15
<u>L3</u>							
fprop	3.07	0.89	3.08	0.89	4.40	0.87	3.49
bprop	3.08	0.89	3.07	0.90	4.05	0.86	3.48
accGrad	3.07	0.89	3.06	0.89	4.03	0.87	3.48
<u> </u>							
fprop	0.84	0.24	0.83	0.24	1.21	0.24	0.95
bprop	0.83	0.24	0.83	0.24	1.13	0.23	0.94
accGrad	0.84	0.24	0.82	0.24	1.10	0.24	0.95
<u>L5</u>							
fprop	7.07	1.58	2.39	0.51	6.23	0.50	2.54
bprop	7.07	1.59	2.40	0.51	5.59	0.51	2.54
accGrad	2.40	0.51	2.38	0.52	6.18	1.54	7.51

In the particular case of L1, the FFTs take more than 50% of the runtime. This is due to the wasteful interpolation of the kernel tensor from a 11×11 up to 128×128 , which is the minimal size to compute the FFT of the input array without interpolation loss. In such cases, the tiling strategy we are developing (see section 6) will result in large additional performance gains.

8.2 FFT: DECIMATION IN TIME VS FREQUENCY

A Fourier transform projects \mathbb{R} and \mathbb{C} -valued functions onto a harmonic orthogonal basis. The discrete Fourier transform of a vector $\{x_k\}, k \in [0, n-1]$ is the vector:

$$\{X_k\} = \left(\sum_{j=0}^{n-1} x_j w_n^{kj}\right), \ k \in [0, n-1]$$

where $w_n^j = e^{-2\pi i j/n}$ is the j^{th} n-root of unity. The traditional radix-2 Cooley-Tukey algorithm recursively decomposes the computation between an odd and even part:

$$\{X_k\} = \left(\sum_{j=0}^{(n-1)/2} x_j w_n^{k(2j)} + \sum_{j=0}^{(n-1)/2} x_{2j+1} w_n^{k(2j+1)}\right), \ k \in [1, n]$$

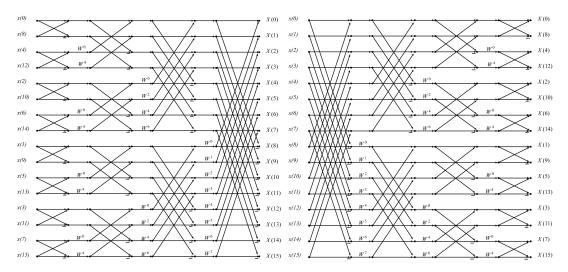


Figure 9: DIT output ordered (left); DIF input ordered (right) (Burrus (2008))

This decomposition is called *decimation in time* (DIT). An alternate decomposition performs *decimation in frequency* (DIF):

$$\{X_k\} = \left(\sum_{j=0}^{(n-1)/2} x_j w_n^{kj} + \sum_{j=(n-1)/2}^n x_j w_n^{kj}\right), \ k \in [1, n]$$

When n is a power of 2, both decimations recursively decompose into a perfectly balanced tree and take advantage of the symmetry properties of the roots of unity. The dataflow graph for the radix-2 FFT has a butterfly shape and is a good way of visualizing the computations. There is a symmetry between DIT and DIF in both the order of operations applied and in whether the input or the output order is shuffled (Figure 9).

8.3 GPU PROGRAMMING

There are a variety of references available that describe CUDA and NVIDIA's various GPU architectures (Garland et al. (2008)) which we won't discuss in detail, but the implementation of fbfft very much depends upon specifics of the Kepler GPU architecture.

NVIDIA GPUs execute code at the granularity of a *warp* which is defined as a set of 32 threads in all existing architectures; each thread is assigned a *lane* within the warp. These threads execute in a *SIMT* (single instruction, multiple thread) fashion, meaning that a warp is an atomic unit of execution. It holds a single *program counter* (PC) and can thus only execute a single instruction at a time across all of its threads. Collections of warps are brought together in *blocks* or *CTAs*, which together share a region of fast *shared memory* resident on chip. Blocks themselves can only exchange data via much slower *global memory*, resident on the GPU or in the host CPU's address space.

Individual threads within a warp are free to take divergent paths, but since a single PC is present, each branch in the execution will be serialized. Threads that aren't participating in the branch in question are disabled. In other words, if all 32 threads were to take divergent code paths, we would obtain only $1/32 \times$ of the computational efficiency.

Divergent code paths are hard to avoid, but the NVIDIA instruction set has means to reduce their cost (Giles (2014)). One is with predicated instructions, which are used for small branches, in which all warp threads execute both parts of the branch, with non-participating threads having no side effects.

Block threads have access to a register file, with up to 255 registers per thread for Kepler. Registers are allocated statically by the CUDA compiler. An important performance factor when writing CUDA kernels is that data should be kept in registers as much as possible to avoid communications.

Registers in CUDA are "addressable": it is possible to declare a static array within registers and operate on its elements. The limitation is that all addressing should be performed using statically determined constants so the compiler can translate these accesses to a register number known at compile time. Indirect addressing is also supported but results in copies to a local region within global memory, which essentially constitutes register spilling. Even with the presence of caches, using local memory usually comes with a performance hit.¹¹ As a consequence, we design our kernels using aggressive inlining, template parameters and unrolling directives to make all register accesses statically addressable.

The Kepler architecture introduced specialized shuffle instructions to exchange data between registers within a warp synchronously, which avoids round-trips to shared or global memory. Interestingly, these shuffle instructions allow the dynamic indexing of an array held in registers, as long as the array is distributed in a cyclic fashion across registers in each thread within a warp.

Many warps run in parallel and can be switched by the GPU hardware at each cycle. When enough parallelism is available (measured in *occupancy* of the GPU as a first approximation), long latency operations are hidden thanks to fast context switching. Registers and shared memory come in finite quantities on each GPU compute multiprocessor. These limited resources are partitioned by the compiler and the hardware amongst computations at the level of a CUDA kernel. Increased usage of registers or of shared memory can reduce GPU *occupancy*, which limits the ability to hide long latency operations. Reduced occupancy does not necessarily result in performance loss (Volkov (2010)). There are often non-obvious performance tradeoffs in increasing or decreasing threads per block, shared memory per block or registers per thread that are hard to discover. This problem is one of the many reasons why designing a one-size-fits-all implementation that aims to be efficient for any problem is difficult.

¹¹There are bleeding edge cases where a little local memory consumption helps performance; for instance, when restricting the number of registers per thread to increase occupancy.