Packaging: Past, Present and Future

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Abstract—**In the past, Microsystems Packaging played two roles: 1) It provided I/O connections to and from devices, referred to as IC or wafer level packaging, and 2) It interconnected both active and passive components on system level boards, referred to as systems packaging. Both were accomplished by interconnections or multilayer wiring at the package or board level. More recently, the IC devices have begun to integrate not only more and more transistors but also active and passive components on an individual chip, leading the community to believe that someday there may be a single-chip system, referred to as SOC or System–on–Chip. This can be called horizontal or 2D integration of IC blocks toward systems. The community began to realize, however, that such an approach presents fundamental, engineering and investment limits and computing and integration limits for wireless and wired communication systems over the long run. This led to 3-D packaging approaches, often referred to as SIP or System-in-Package. The SIP, while providing major opportunities in both miniaturization and integration for advanced and portable electronic products, is limited by the CMOS process just like the SOC. Some existing and emerging applications, however, include sensors, memory modules and embedded processors with DRAMs. More recent 3-D solutions, which incorporate stacked package approaches, offer solutions towards faster time-to-market and business impediments that have plagued MCM deployment for the past decade.**

There is a new concept which is called SOP or System-on-Package. With SOP, the *package,* not the board, is the *system.* As such, SOP is beginning to address the shortcomings of both SOC and SIP, as well as traditional packaging which is bulky, costly, and lower in performance and reliability than ICs, in two ways: 1) It uses CMOS-based Si for what it is good for, namely, for transistor integration, and the package, for what it is good for, namely, RF, optical and digital integration by means of IC-package–system co-design. The SOP package, therefore, overcomes both the computing limitations and integration limitations of SOC, SIP, MCM and traditional system packaging. It does this by having global wiring as well as RF, digital and optical component integration in the package, not in the chip. SOP, therefore, includes both active and passive components including embedded digital, RF and optical components and functions in a microminiaturized package or board.

Index Terms—**Integrated circuit packaging, Convergent Electronics Systems, SOP, SOC, SIP, Interconnections, Optoelectronics, Multichip modules, Consumer electronics, Integrated optoelectronics, Moore's Law**

I. INTRODUCTION: THE TREND TOWARD CONVERGENT SYSTEMS

The electronic systems in the past are primarily discrete systems with computers performing data computations, telecommunications providing voice-based communications, and consumer products providing audio, video and other functions in portable products. The current focus, however, is in portable and wireless systems such as cell phones. There is a new and emerging trend in systems which is referred to as "Convergent Systems" that is characterized by the convergence of computer, communications, consumer and biomedical product functions into one package or product. Convergent systems span consumer, infrastructure, automotive, aerospace and biomedical industries. Examples of next-generation convergent systems include personal digital assistants with cell phones, GPS, sensors, web mail access and smart medical implants, as illustrated in **Fig. 1**.

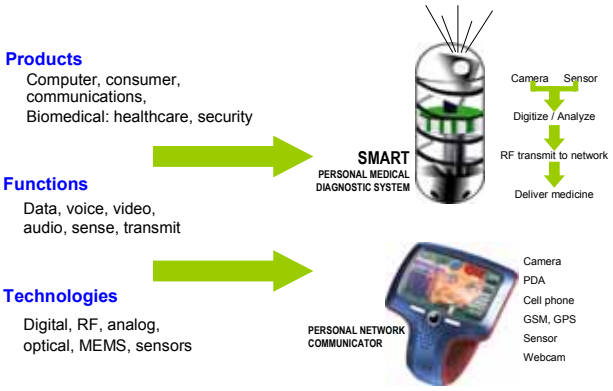

Fig. 1. Trend to convergent and miniaturized electronic and bio-electronic systems.

The technologies required to accomplish this convergence of data, video, voice, sensing and other functions are digital, optical, RF, analog, MEMS and sensors. While some of this convergence is beginning to take place in the industry, it is primarily by discrete and bulky components which don't take advantage of the synergy between the IC and the package as the new SOP and SIP concepts for highly integrated multi-functional systems do, as described in this paper.

II. PACKAGING IN THE PAST WITH COMPUTING FOCUS

Packaging in the past is shown in table 1. In 1970s and 80s, it is primarily by bulky component packaging such as DIP and QFPs with peripheral I/Os and the system boards are made up of mechanically–drilled holes that are subsequently plated to form interconnections from layer to layer. The holes also served to interconnect components by pin-through-hole technology. These technologies paved the way for smaller packages such as BGA with more I/Os, this time in area array fashion, to and from the system board, leading to surface mount technology (SMT). These technologies served the high performance computing and communication needs despite

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their bulky nature. When extremely high computing or communication performance was needed, a new advanced packaging technology called MCM (Fig 2.) was invented back in the 1980s at IBM and NEC, Fujitsu and Hitachi for the sole purpose of regrouping good bare ICs directly onto a ceramic or ceramic package with polymer-copper wiring since larger chips could not be produced with any acceptable yields on the original silicon wafer. These original MCMs were horizontal or two-dimensional.

Fig 2. MCM Technology in 1980s

Table 1. Packaging Evolution Trend

	1970s	1980s		1990s		2000s	2010s	
	DIP	PGA	QFP	BGA	CSP	WLP	SIP	SOP
Single	→	→	→	→	→			
Chip Connector	Wirebond →	Redistribution to Area Array →		Flipchip Area Array →				
Board	Ceramic →	Ceramic or Thin Film on Ceramic →		Thin Film on PWB →				
Package	PWB-D →	PWB-D →		PWB-Micro Via →				
Board Connector	PTH →	Peripheral SMT →		Area/BGA SMT →				
Discrete :	1005 →	0805 →	0603 →	0402 →		0201	01005?	Integratio

The above traditional packaging presents major problems. The IC packaging that is used to provide I/O connections from the chip to the rest of the system is typically bulky and costly, limiting both the performance and the reliability of the IC it packages. Systems packaging, involving the interconnection of components on a system level board, is similarly bulky and costly with poor electrical and mechanical performance.

III. CURRENT PACKAGING WITH PORTABLE WIRELESS FOCUS

Current packaging is driven by portable and wireless products such as Cellular phones. These products do not generally drive the performance except for RF but they demand portability and lower cost. This type of packaging called form-factor packaging began to push new directions in both IC and systems packaging. In IC packaging, it led to such a variety of wafer level technologies as CSP, compliant interconnects and so on, as illustrated in Fig.3. It also led to thin film organic package technologies pioneered originally by IBM in Japan called SLC or build-up and flip chip to organic assembly, also pioneered by IBM. These technologies became the basis of all high-performance and portable wireless systems of today.

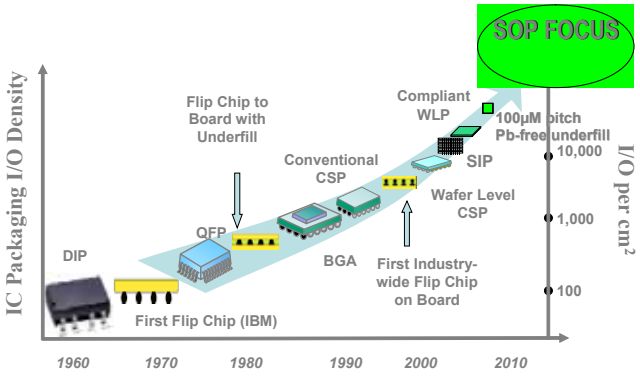
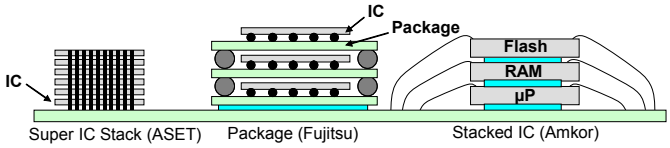


Fig 3. Package Evolution Trend

A new technology called SIP emerged more recently to add to the above two technologies. SIP is defined in this paper as the vertical stacking of similar or dissimilar ICs. They can be stacked bare or stacked as packaged structures. There are clear major benefits to SIP in contrast to SOC: simpler design and design verification, IC processing with minimal mask steps, minimal time-to-market, and minimal IP issues.

Because of these benefits, about 30 IC and packaging companies alike have been gearing up in a big way to produce SIP-based multichip modules (**Fig. 4**). SIPs seem to come in many flavors as fabricated in organics, ceramics or Si wafers.



- 3-D Plus
- Amkor Technology, Inc.
- APack Technologies, Inc.
- Array Packaging Technologies, Inc.
- ChipPAC, Inc.
- Dense-Pac Microsystems, Inc. and Q-Flex, Inc.
- Epson Electronics America / Seiko Epson
- Fujitsu Microelectronics, Inc.
- IBM
- Intel Corporation
- Irvine Sensors
- Mitsubishi Electronic & Electronics USA, Inc.
- Sharp Corporation
- Silicon Bandwidth
- Tru-Si Technologies
- Toshiba Corporation
- Unitive Electronics
- Vertical Circuits

Source: Chip Scale Review March 2001

Fig. 4. Some of more than 30 companies currently pursuing SIP.

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IV. FUTURE PACKAGING WITH DIGITAL CONVERGENCE FOCUS

One can visualize four approaches as in Fig. 5 for the digital convergence:

1. SOC (System-on-Chip)
2. MCM (Multichip Module)
3. SIP (System-in-Package)
4. SOP (System-on-Package)

The SOC schematic shown in **Fig. 5**, for example, seeks to integrate numerous system functions on one silicon platform horizontally, namely the chip. If this chip can be designed and fabricated cost effectively with computing, communication and consumer functions such as processor, memory, graphics, antennas, filters, switches, fibers or waveguides and other components required to form a complete end-product system, then all that is necessary to package such a system is to power and cool. If this can be realized, SOC offers the promise for the most compact, light-weight system that can be mass-produced. This has been and continues to be the roadmap of IC companies. So the key question is whether SOC can lead to cost effective, complete end-product systems such as tomorrow's leading-edge cell phones with digital and sensing capabilities or as bio-medical implants. Researchers around the world, while making great progress, are realizing that SOC, in the long run presents fundamental limits for computing and integration limits for wireless communications and additional non-incremental costs to both. Among SOC challenges are the long design times due to integration complexities, high wafer fabrication costs, test costs, and mixed-signal processing complexities requiring dozens of mask steps and IP issues. The high costs are due to the need to integrate disparate active devices such as bipolar, CMOS, SiGe and OEIC — all in one chip with multiple voltage levels and dozens of mask steps to provide digital, RF, optical and MEMS-based components.

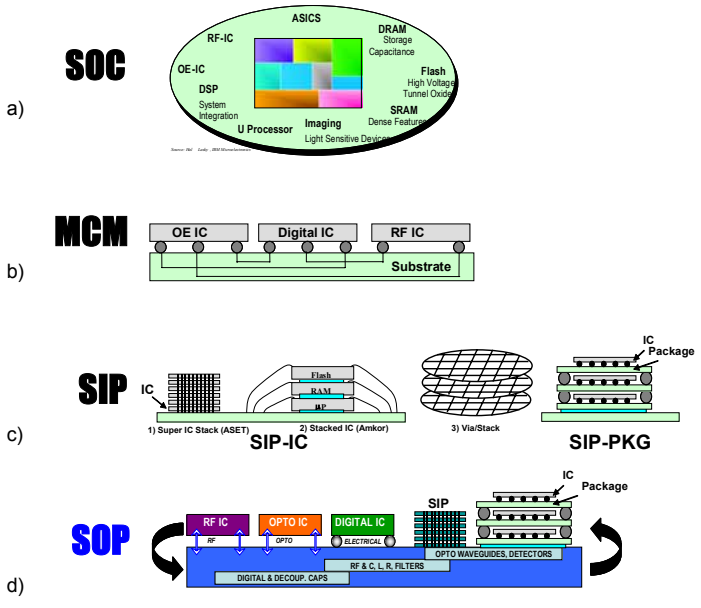

Fig. 5 a) System-on-Chip (SOC) based on a complete system on one chip; b) Multi-Chip Module (MCM) based on interconnected components; c) System-in-Package (SIP) based on a stacked chip/package for reduced form factors; and d) System-on-Package (SOP), offers the best of IC and packaging technologies by optimizing functions between ICs and the package while miniaturizing systems.

A new paradigm that overcomes the shortcomings of both SOC and traditional packaging, therefore, is necessary. The articles in this issue make a compelling case for the synergy between the IC-package-system by means of the SOP paradigm.

SOP (System-on-Package) goes one step beyond all three of the above approaches in overcoming both the fundamental and integration shortcomings of SOC, SIP and MCM, which are limited by CMOS processing and the shortcomings of current packaging. While silicon technology is great for transistor density improvements from year to year, according to Moore's Law, it is not an optimal platform for system integration of RF, optical, and certain digital components, as stated above. The SOP is akin to Moore's Law for IC, integrating transistors; it integrates thin film components at microscale in the short term and nanoscale in the long run for mixed-signal electronic and bioelectronics systems, as shown in **Fig. 6**.

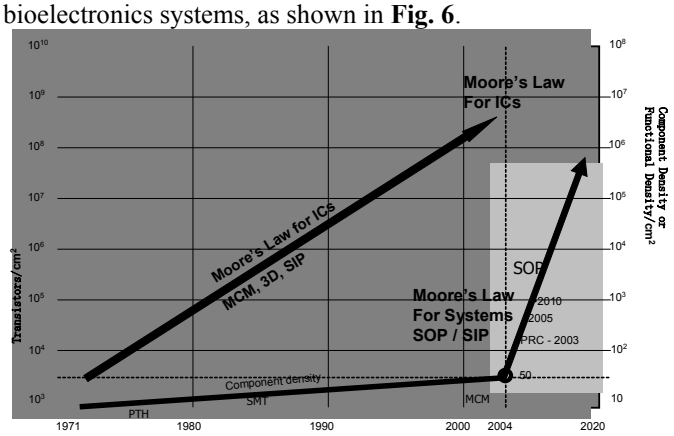

Fig. 6. SOP: Moore's Law for System Integration

The SOP concept overcomes a number of the engineering limits of SOC. As IC integration moves to nanoscale and wiring resistance increases, the global wiring delay in SOC becomes too high for computing applications. This leads to what is referred to as "latency" which can be avoided by either moving global wiring from the nanoscale on ICs to the microscale on SOP, or making the digital chips much smaller. SOP handles both of these. Wireless integration limits of SOC are also handled well by SOP. RF components such as capacitors, filters, antennas, switches, and high frequency and high Q inductors, are best fabricated in the package rather than on silicon. To meet the need for the amount of decoupling capacitance necessary to suppress the expected power plane noise associated with very high performance ICs which require more than 100 watts per chip, a major portion of the chip area would have to be dedicated to decoupling capacitance alone. Semiconductor companies are not in the capacitor business; they are in the transistor business. The highest Q factors reported on silicon are about 10-25, in contrast to 100-400 achieved in the SOP package. Optoelectronics, which today finds use primarily in the back

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planes and is used for high-speed board interconnects, is moving onto the package as chip-to-chip for high I/O and high-speed interconnections, replacing copper, and thus, addressing both the resistance and cross-talk issues of electronic ICs. Optoelectronics is not seen as moving onto the SOC chip to replace copper wiring anytime soon.

The SOP concept seeks to integrate multiple system functions into one compact, light-weight, thin profile, low-cost, high performance packaged system (Fig. 7). The system design may call for high performance digital logic, memory and graphics, and analog signals for RF and video as well as broadband optical functions. Unlike SOC, however, no performance compromises have to be made in order to integrate these disparate technologies since each technology is separately integrated into the SOP package. System design times are expected to be much shorter, and the testing is expected to be simpler. In addition, the SOP concept allows for shorter time-to-market and greater flexibility with which to take advantage of emerging technologies. With the SOP concept, the chip size can be as small as required to be manufacturable with high yields and its wiring length can be as small as needed to overcome the high resistance-imposed global signal delays.

Fig. 7 illustrates the difference between SIP and SOP.

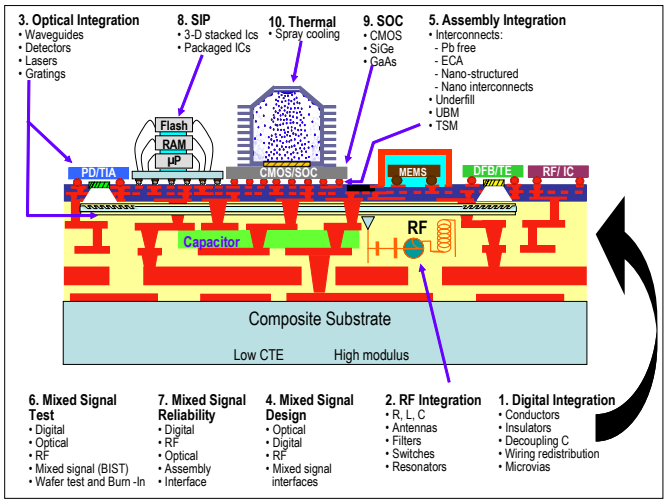

Fig. 7. SOP concept of system integration of components.

V. GLOBAL STATUS OF SOP

The SOP concept of embedding RF, optical, and certain components by means of thin films in the package began in 1994 at the Georgia Institute of Technology with funding from the National Science Foundation, the Georgia Research Alliance and partnerships with 50 global semiconductor, packaging and systems companies. Today, SOP R&D is pervasive and goes beyond SIP as shown in Fig. 8.

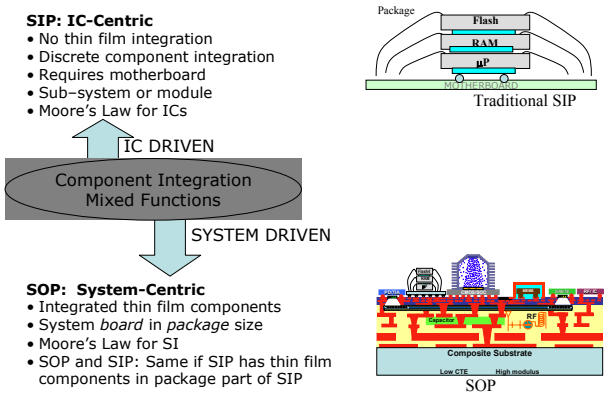

Fig. 8. Difference between SIP and SOP concepts

ACKNOWLEDGMENT

The author acknowledges the contributions of his faculty and staff colleagues including Mr. Reed Crouch for graphics at the PRC. He also wishes to thank the National Science Foundation (NSF) for supporting this work through the NSF ERC in Electronic Packaging (EEC-9402723) at the Georgia Institute of Technology.

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Born in India, Dr. Tummala received his B.E. degree (‘64) in metallurgical engineering from the Indian Institute of Science, Bangalore, India and his Ph.D. degree (‘69) in materials science and engineering from the University of Illinois.

After earning his Ph.D., he began a 25-year career at IBM where he was awarded the IBM Fellow designation. At IBM, he led a number of pioneering developments that included the industry's first alumina multichip substrate development, industry’s first LTCC, first gas discharge display, now called flat panel display, and advanced materials for ink jet printing and magnetic storage products. He is known as the father of glass-ceramic or LTCC and author and co-editor of the “Bible”—the first modern book on packaging called the “Microelectronic Packaging Handbook” (Van Nostrand, 1988) and the author and editor of first textbook called “Fundamentals of Microsystems Packaging”. He received a total of 71 U.S. patents and authored 345 papers in these pioneering developments. He then embarked on a new career at Georgia Tech in 1993 and wrote the proposal for, and was awarded, an NSF Engineering Research Center to explore and develop the SOP concept that led to the well known center called Packaging Research Center (PRC). Considered the pioneer of SOP technology that is sweeping the microsystems industry today, he is an internationally recognized leader in his field and is sought out as a keynote speaker at conferences around the world and as consultant and advisor. His research interests include: microsystems systems packaging, electronic materials, display technologies, and magnetic storage.

Dr. Tummala is a member of the National Academy of Engineering; a Fellow of IEEE, the American Ceramic Society and IMAPS. He has received countless awards including: IEEE‘s major Education Innovation Medal, Dan Hughes award from IMAPS, David Sarnoff award from IEEE, IEEE Millennium Medal of Honor, Educator of the Year for Excellence in Teaching, Research, and Innovation in the Field of Electronics by the India-American Cultural Association, Inc., and Distinguished Professor award from University of Illinois, Georgia Institute of Technology and Indian Institute of Science, Bangalore.

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