

CHALMERS

EXAMINATION / TENTAMEN

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Course code/kurskod	Course name/kursnamn			
DIT431	High Performance Parallel Programming			
Anonymous code Anonym kod		Examination date Tentamensdatum	Number of pages Antal blad	Grade Betyg
DIT431-0007-ADT		27/10/2023	13	

I confirm that I've no mobile or other similar electronic equipment available during the examination.
Jag intygar att jag inte har mobiltelefon eller annan liknande elektronisk utrustning tillgänglig under examinationen.

Solved task Behandlade uppgifter	Points per task Poäng på uppgiften	Observe: Areas with bold contour are to completed by the teacher. Anmärkning: Rutor inom bred kontur ifylles av lärare.
No/nr		
1	X 8	
2	X 8	
3	X 2	
4	X 9	
5	X 9	
6	X 6	
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
Bonus poäng		
Total examination points Summa poäng på tentamen	42	

~~(a) (1) N:1:~~~~1000 ULTs.~~

~~$$\frac{1000}{10} = 100 \text{ ULTs on each core.}$$~~

~~$$\text{Total execution time} = 100 * (10 + 1) = 1100 \text{ units}$$~~

(1) N:1:

(a) Only 1 core can be used.

1000 ULTs.

$$\text{Total execution time} = 1000 * (10 + 1) = 11000 \text{ units.}$$

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(2) 1:1

$$\frac{1000}{10} = 100 \text{ KLTs on each core.}$$

$$\text{Total execution time} = 100 (10 + 5) = 1500 \text{ units.}$$

2.5

(3) N:M, 10:1

$$\text{No. of KLTs} = \frac{1000}{10} = 100.$$

$$\begin{aligned} \text{Total execution time of 1 KLT} &= 10 * \text{time for 1 ULT} \\ &= 10 * (10 + 1) \\ &= 110 \text{ units} \end{aligned}$$

$$\text{Total execution time} = \frac{100}{10} (110 + 5) = 1150 \text{ units.}$$

1b) Each task now takes 20 units, thus the execution time to context switch time ratio increases to 20:1 for ULTs and 20:5 for KLTs.

This makes using ~~MPM or MMT more suitable~~ more fine grained threading models more suitable.

~~N:1 results in execution time~~

N:1 is not suitable as no parallelism is utilised.

1:1 has execution time of $100(20+5) = 2500$ units.

10:1 has $10 \times (5 + 10(1+20)) = 2150$ units.

100:1 has $1 \times (100(1+20)) = 2100$ units

Thus 100:1 is most effective.

1c) If there are more than 1 KLT like in 1:1 or N:M, the KLTs have a shared address space.

Thus having multiple KLTs should have no issues on the program, as each KLT is able to pass the message to the different node.

1d) CUDA threads are significantly more fine grained. ~~Each~~ CUDA threads have private registers but shared memory between threads in the same block. There is also global memory that all threads can access.

There are many CUDA cores that can execute the many fine grained CUDA threads. Context switching overheads are also low as each thread has its own registers. Similar to SIMD, CUDA uses Single Instruction Multiple Threads by ~~executing~~ ^{executing} the same instruction on all threads in a warp.

2a) a) Static scheduling.

64 loop iterations. Each processor has $\frac{64}{8} = 8$ iterations.

$$\text{Time units to complete} = 8 \times 2.0 = 16 \text{ time units.}$$

2a (b) self-scheduling.

Each processor has 8 iterations

$$\text{Time units to complete} = 8 \times 2.0 = 16 \text{ time units.}$$

2a (c) chunk-scheduling.

$$\frac{64}{6} = 10.6 \text{ chunks.}$$

$$\text{Each processor executes } \frac{16}{8} = 2 \text{ chunks.}$$

There are 10 chunks of size 6, 1 chunk of size 4.

6 6 4.

6 6 6 6 6 6 6 6

P₁ P₂ P₃ P₄ P₅ P₆ P₇ P₈

$$\text{Execution time} = (2 \times 6) \times 2.0 = 24 \text{ time units.}$$

2a)(d) guided-scheduling.

$$\begin{array}{ccccccc} 4 & 4 & 4 & 4 & 4 & 2 & & \\ \frac{64}{8} = 8 & \frac{56}{8} = 7 & \frac{49}{8} = 6 & \frac{43}{8} = 5 & \frac{38}{8} = 4 & 4 & 4 & 4 \\ P_1 & P_2 & P_3 & P_4 & P_5 & P_6 & P_7 & P_8 \end{array}$$

$$\text{Execution time} = (8 + 4) \times 2.0 = 24 \text{ time units.}$$

2b) We can ~~collapse~~ collesce (collapse) the nested loop to be of depth 1.

#define N 64.

```
for (int j=0; j<N*N; j++) {
    int k = j % N;
```

~~original~~

```
int i = j / N;
```

```
a[i*N+k] = (i+1)*N+k;
```

```
}
```

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2c) Overhead > speedup.

$0.5 > \text{ceil}(\frac{x}{p}) \times 2.0$ where x is no. of iterations.

$$\frac{1}{4} > \text{ceil}(\frac{4096}{p})$$

$$p > 1024.$$

After $p=1024$, adding new processors result in a slowdown.

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3a) $AI = \frac{\text{FLOPs}}{\text{Bytes}} = \frac{2}{4 \times 4} = \frac{1}{8} \text{ FLOPs/Byte}$, since
C has to be loaded and stored, and each
float is 4 bytes.

Single core: performance = $\min(4, \frac{1}{8} \times 16)$
= 2 GFLOPs.

execution time = $\frac{100 \times 100 \times 100 \times 2}{10^6 \times 2} = 1 \text{ s.}$

8 cores: performance = $\min(8 \times 4, \frac{1}{8} \times 16)$
= 2 GFLOPs.

execution time = 1 s

3b) By multiplying the performance of each core by 4,
the AI is not changed thus the bottleneck is still
memory. Even in a 32-core machine, the bottleneck
is still the same.

3c) multi-core chip execution time = 1 s.

upper limit = $\frac{1}{f}$ where f is serial fraction
= $\frac{1}{0.5 \times 10^{-3}} = 2000.$

Using my results, since the single core has the
same execution time since it is bounded by
memory, executing on more cores will not
result in more speed-up. Optimising the kernel
is very suitable here. Optimising the serial portion
is less suitable since the ratio of 0.5×10^{-3}
to 1 s is already quite low.

4a) No. There is a read after write dependency. For example, when $i=0$ we write to $A[0]$, but when $i=N-1$, we read from $A[0]$.

4b).

parallel

~~#omp para~~

#pragma omp parallel for reduction

for (int i=0; i<N; i++) {

if ($i < \frac{N}{2}$) {

$A[i] += A[N-1-i];$

}

#pragma omp barrier;

if ($i \geq \frac{N}{2}$) {

$A[i] += A[N-1-i];$

}

}.

4c) $quad += temp$ has a dependency and there is a risk that stores are lost.

First Method:

We can make $quad += temp$ an atomic instruction using `#pragma omp atomic`. This way every variable can be shared, except for $temp$ which should be private.

Second method:

We can use make $quad += temp$ a critical region so that only 1 thread runs the instruction at a given time. We use `#pragma omp critical`. using shared variables, except for $temp$ which should be private. 4

Third method:

We can use `reduce` in our for loop with $quad$ and $temp$ as shared variables.

`#pragma omp parallel for reduce(+:quad) private(temp)`

4d) I expect using `reduce` to be the fastest since every thread can still be fully run asynchronously, followed by ~~critical~~ ^{atomic} then critical, since critical requires longest waiting. For critical, compiler can create a lock for the variable $quad$. For atomic, a lock can also be used. For `reduce`, the compiler can create different $quad$ variables for each thread.

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5a)

First way: We can use Scatter so that the one processor can allocate the chunks of the matrix to the corresponding processors.

```
int id = MPI_get_MPI_id;
```

```
MPI_Scatter (sendbuf, bytesToSend, sendType, recvbuf,  
            recvCount, recvType, 0, MPI_COMM_WORLD);
```

Now the processors portion of the matrix is in
recvbuf

Second way: We can use the root to send each
processors portion of the matrix.

```
if (get_MPI_rank() == 0) {  
    for (int i=0; i < P; i++) {  
        MPI_Scatter  
        MPI_Send (buf[i], count, datatype, i, 0, MPI_COMM_WORLD);  
    }  
} else {  
    MPI_Recv (recvbuf, count, datatype, dest get_MPI_rank(), 0, MPI_COMM_WORLD,  
             status);  
}
```

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5b)

int* block = ... // obtained from 5a)

int zeros = 0;

for (int i = 0; i < $\frac{N}{P}$; ~~int~~ i++) {

for (int j = 0; j < N; j++) {

if (block[i][j] == 0) {
zeros++;

}

}

int* receive;

:

MPI_Reduce (&zeros, receive, P, MPI_INTEGER,
MPI_ADDITION, 0, MPI_COMM_WORLD
) ;MPI_Bcast (receive, P, MPI_INTEGER, 0, MPI_COMM_WORLD
) ;

5c) Ssend and Srecv are synchronous ^{and non blocking} which means Ssend only returns when the other side has started receiving and Srecv only returns when it has ~~started receiving~~ received into the buffer. This means for every Ssend, it is able to synchronise with a Srecv and vice versa, since no deadlocks were observed. Thus, even if they are replaced to non-blocking and Wait calls, no deadlock would occur.

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6a)

A: & d-row

B: & d-col

C: & d-data

D: & d-x

E: & d-y

F: d-row, &row

G: d-col, &col

H: d-data, &data

I: d-x, &x.

J: 1, N.

K: d-row, d-col, d-data, d-x, d-y, N

L: &y, d-y

6b)

~~Row and column~~~~Data and~~
data and col vectors are accessed sequentially in each thread.~~-- global --~~ ~~vec~~ ~~spawn (.....)~~~~-- shared --~~ ~~shared~~

6b) x offers temporal locality as each value in x is accessed multiple times. Thus we can bring x into shared memory.

```
--global-- void spmv( .... ) {
    --shared-- x_shared[N];
    int tid = ...
    if (tid < N) {
        float dot = 0.0;
        for (int i = row[tid] ..... ) {
            int col_ind = col[i];
            int x_val;
            if (x_shared[col_ind] == -1) { // (Some way
                x_shared[col_ind] = x[col_ind]; // of checking
                                                    // value has not
                                                    // been added)
            }
            dot += data[i] * x_shared[col_ind];
        }
        y[tid] = dot;
    }
}
```

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6c)

6d) Make use of loop tiling so that we access x in blocks, ~~to~~ and each thread block is able to share the block of x that they require.