GEORGIA INSTITUTE OF TECHNOLOGY

School of Electrical and Computer Engineering

ECE-6276-A DSP Hardware System Design (Fall 2018)

Midterm Coding: Serial Distributed Arithmetic

Assigned Date :

Due Date : 3 hours later

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1 Introduction

In this question, we will be designing a **signed** *Distributed Arithmetic* (DA) with serial inputs. This serial DA is similar to the one you designed in Lab 6 except for the following:

1. Instead of 4 input data at a cycle, this DA is an 4-tap FIR filter, whose input are serially fed into the design, i.e. one input data at a cycle. The input is a 4-bit signed number.
2. The coefficients for this FIR filter is as follows.

$$h[n] = \{7 - j5, 3 - j8, -8 + j3, -5 + j7\}$$

3. All coefficients are signed 4-bit fixed point complex number. We split the combination of all coefficients into two ROMs, one for real part and one for imaginary part. Each ROM will be looked up by **the same** 4-bit vector.

The data flow (Architecture) of DA looks like Figure 1. You can use the shifter like Figure 2. Other things that is common with the one in Lab 6 are mentioned below:

1. There is `next_in` at the input side but no `next_out` at the output side.
2. **The computation to be done is:**

```
data_out = data[0] * h[0] + data[1] * h[1]
         + data[2] * h[2] + data[3] * h[3],
```

3. There is a controller which selects which group of bits as address to look up the ROMs.
4. Note that Figure 1 may be incomplete. It is up to your design whether and where to add additional pipeline registers.

The input, output ports are showed in Figure 3. We will use **rising edge of clock** to trigger flops, **Synchronous active high reset**.

To implement this design, there are a few things you need to know:

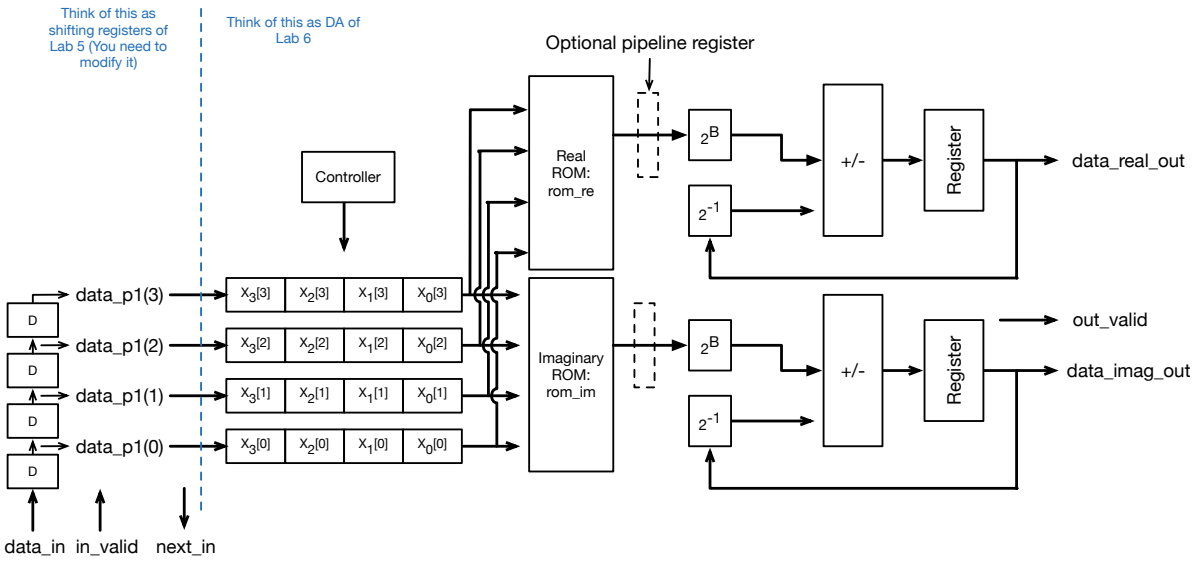

Figure 1 Data flow of a signed DA system

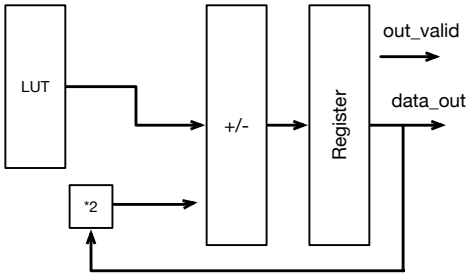

Figure 2 Another static shifter design

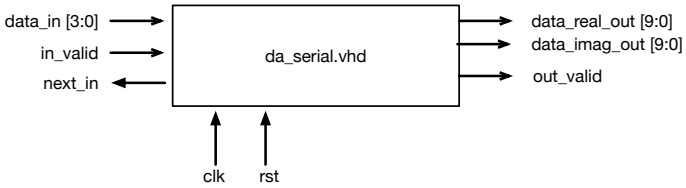

Figure 3 Input, output ports of the design

- The 2 ROMs are already coded for you.
- This is part of the midterm exam. You should finish it individually. You are NOT allowed to discuss with others. **Strict penalty will be applied if copied codes are found!**
- However, you are allowed to use your codes from all previous labs and the lab answer codes coded by the TA.
- Please use `xc7a35tcpg236-1` for synthesis and implementation.

The grading will take into consideration the functional correctness, utilization (area), timing and the power of the design. Three re-submissions are allowed for this lab.

2 Instructions

1. Complete your design in only *ONE* file: `da_serial.vhd`. **NOTE: You are NOT allowed to use multiplication in this lab, which means you cannot use assignments like** `a <= b * c;`.

2. Run the simulation for `da_serial.vhd` using the provided testbench `tb_da_serial.vhd` to match your output file `output.txt` with the reference `output_ref.txt`.

3. Run the synthesis and implementation of your design `da_serial.vhd` in Vivado using the provided constraint file `constraints.xdc`.

3 Deliverables

- **No PDF needs to be turned in.**
- (70% of grade) The *SINGLE* completed design file `da_serial.vhd` . The 70% grading will be based on:
  - (40%) Functional correctness of your design.
  - (20%) **Counter, static shifter (not dynamic), accumulator should be used. Only 2 ROMs are instantiated.**
  - (10%) Sampling period and area of your design.
  - No latch generated. Synchronous reset, sensitivity signal list correct.
- (15% of grade) The simulated output file `output.txt` in the "run" folder. If functionality is incorrect, the grade of this bullet will not be considered.
- The simulated output file `output_cycle.txt` in the "run" folder.
- (15% of grade) The implemented area (utilization), power and timing reports, namely,

  `da_serial_utilization_placed.rpt`

  `da_serial_power_routed.rpt`

  `da_serial_timing_summary_routed.rpt`

Move all of these files into a folder called `midterm_firstname_lastname_gtID` . Zip the folder and upload the archive `midterm_firstname_lastname_gtID.zip` on T-Square (eg. `midterm_george_burdell_123456789.zip`). The first name and last name should be all in lower case. **Please strictly follow this naming convention. Otherwise my script will not work and you might get points deduction.**

Note: Late submissions are not accepted. In case of extraordinary circumstances, written permission must be obtained from Dr. Madisetti.