A 32-bit 100MHz RISC-V Microcontroller with 10-bit SAR ADC in 130nm CMOS GP

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Integrated Circuits and Systems Group

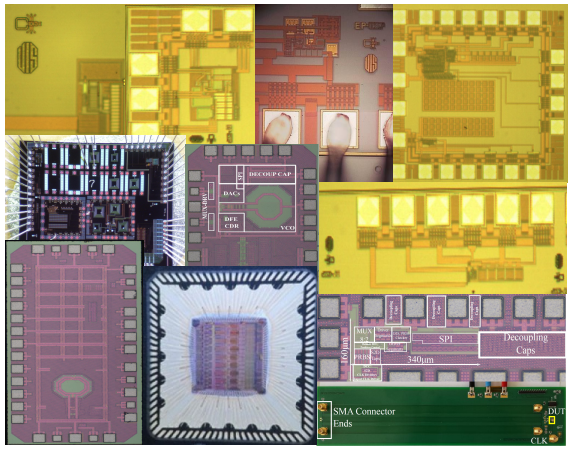
Team

We are a circuit design team NOT a computer architecture team. We can crack specs to RTL and to transistor level.

Over 10 tapeout chips. Analog and digital flow. 45nm, 65nm, 130nm, 180nm, 0.35um and 0.8um CMOS.

Graduate students with industry experience from Freescale, NXP and Samsung.

Alumni at Intel, Qualcomm, Freescale, NXP, Rambus, IDT and Semtech.



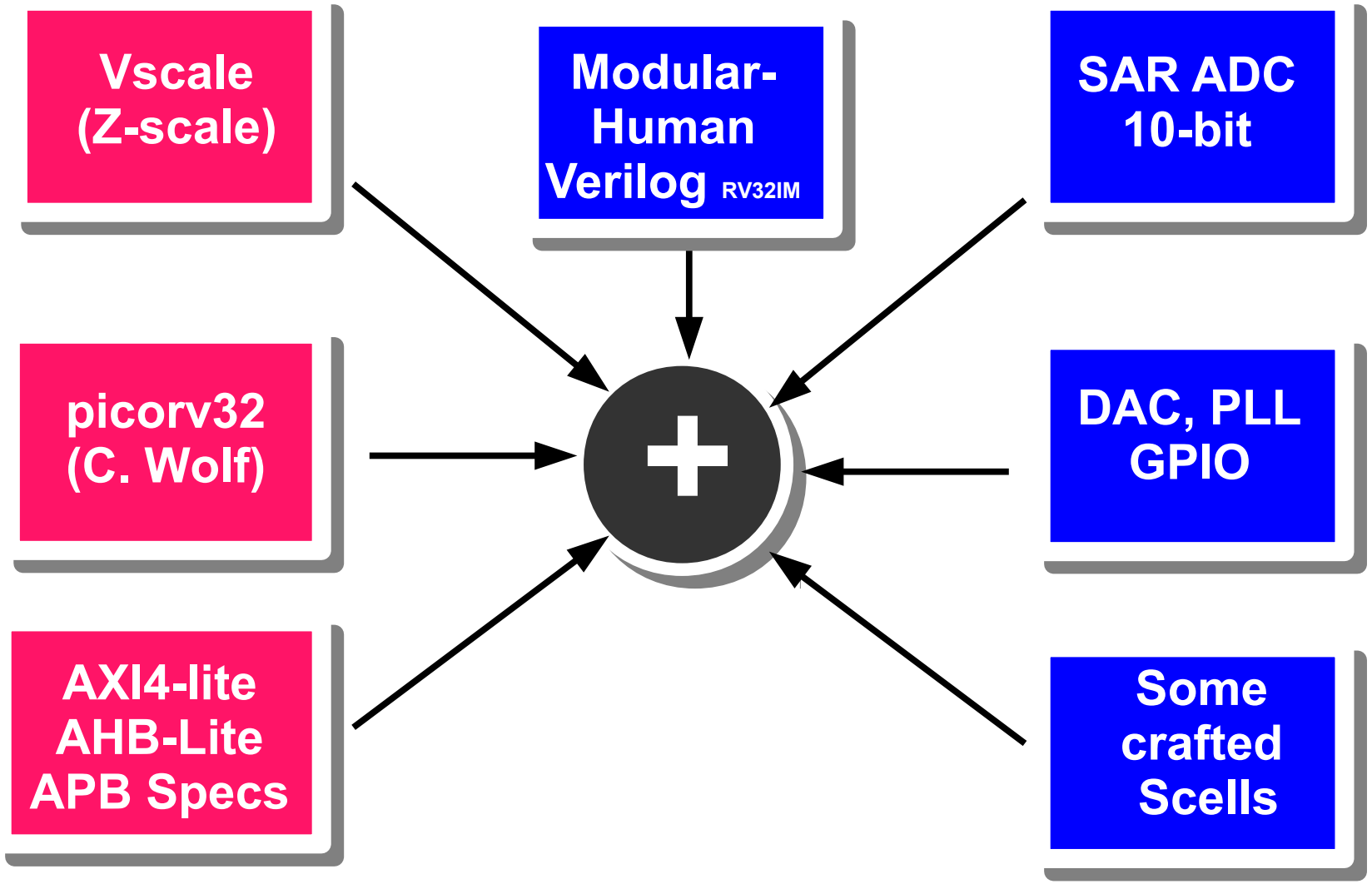
Project Goals

Initial :
An ARM-M0 to be used as on-chip test platform for high-speed interfaces. Test of high-speed flops and circuitry within a processor.

Mid:
A RISC-V core to be used for on-chip test platform.

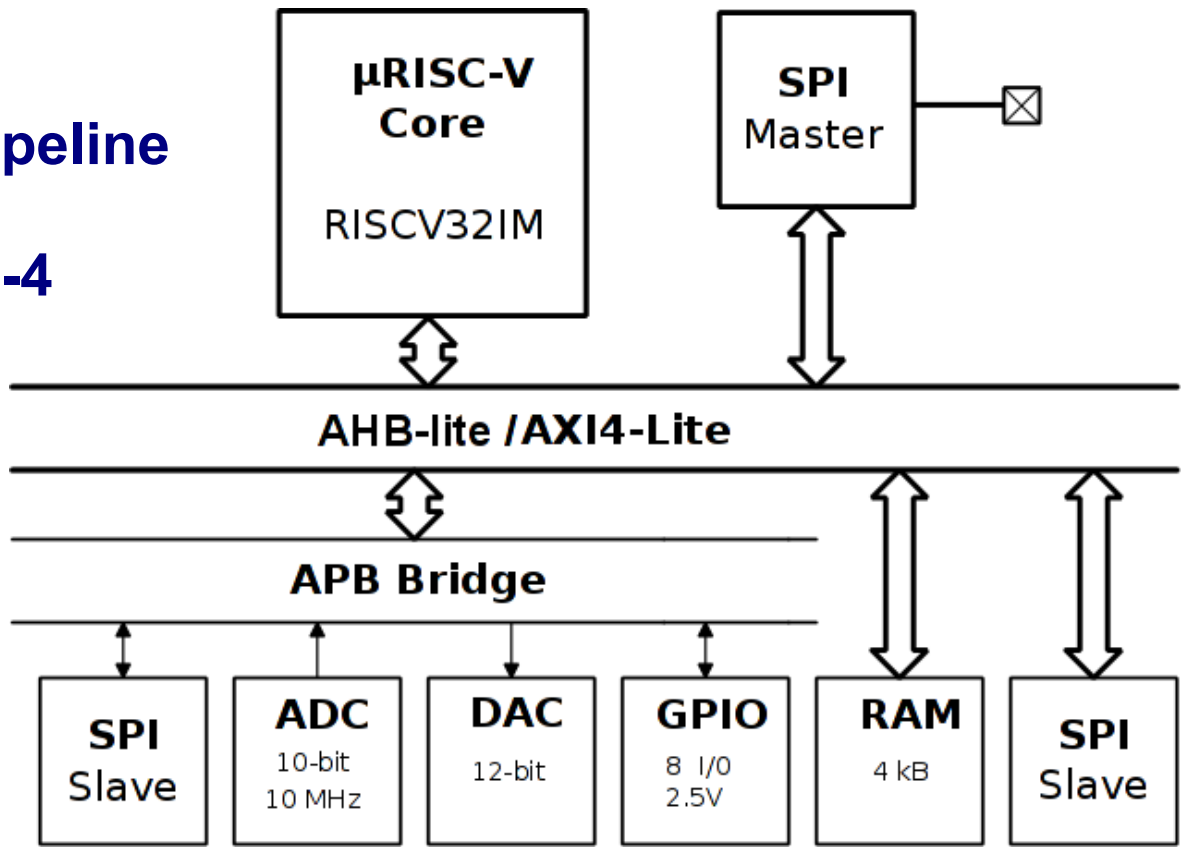
Current:
A low-footprint RISC-V microcontroller alike EFM32 (Silicon Labs) and SAMD11 (Atmel) with USB low-speed PHY on-chip.

Inputs


Vscale
(Z-scale)
Modular-
Human
Verilog RV32IM
SAR ADC
10-bit
picorv32
(C. Wolf)
DAC, PLL
GPIO
AXI4-lite
AHB-Lite
APB Specs
Some
crafted
Scells

Architecture

- Executes RV32IM
- 32-bit 3-stage SIIO pipeline
- AHB-Lite 3.0 and AXI-4 32-bit wide
- IRQ handling adapted from picorv32. Timer

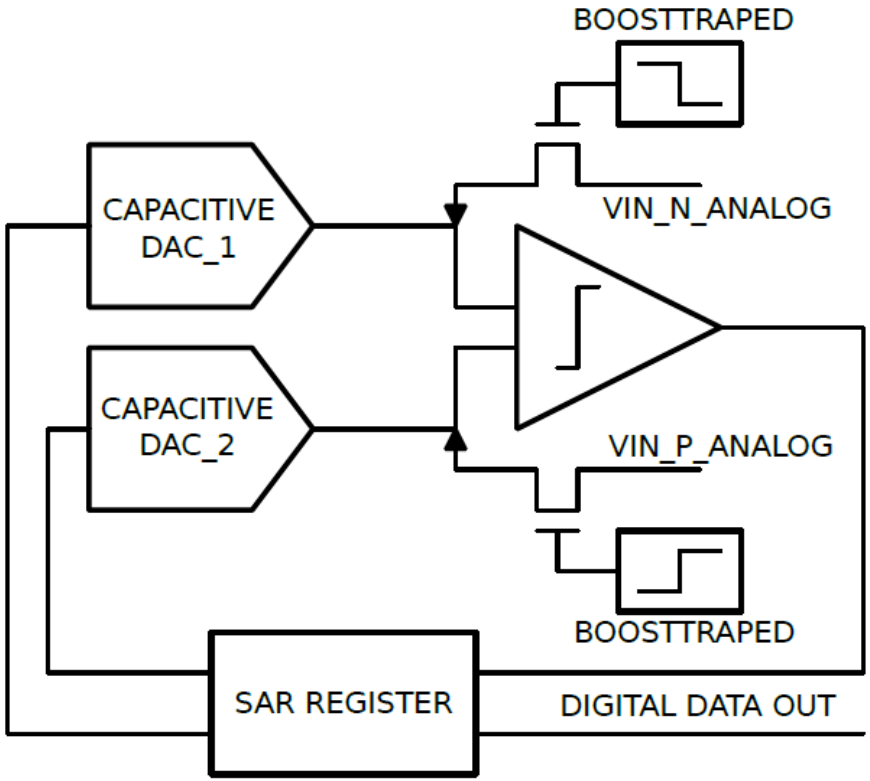


Implementation

- Human-readable modular verilog for RV32I
  - 1210 synthesizable LoC for AXI-4 based micro
  - 8110 logic and 3426 logic cells using RVT lib
  - 2613 buffering cells
- AXI-4 lite 4.0 compliant? (hoping commercial VIP)
- APB-bridge interface, SPI-AXI-4 interface
- 32 dual-port register file
- GPIO and DAC-12-bit AXI-4 interface
- Verification IP for AXI-4 to APB following UVM
- Ring-VCO based PLL and SAR ADC 10-bit

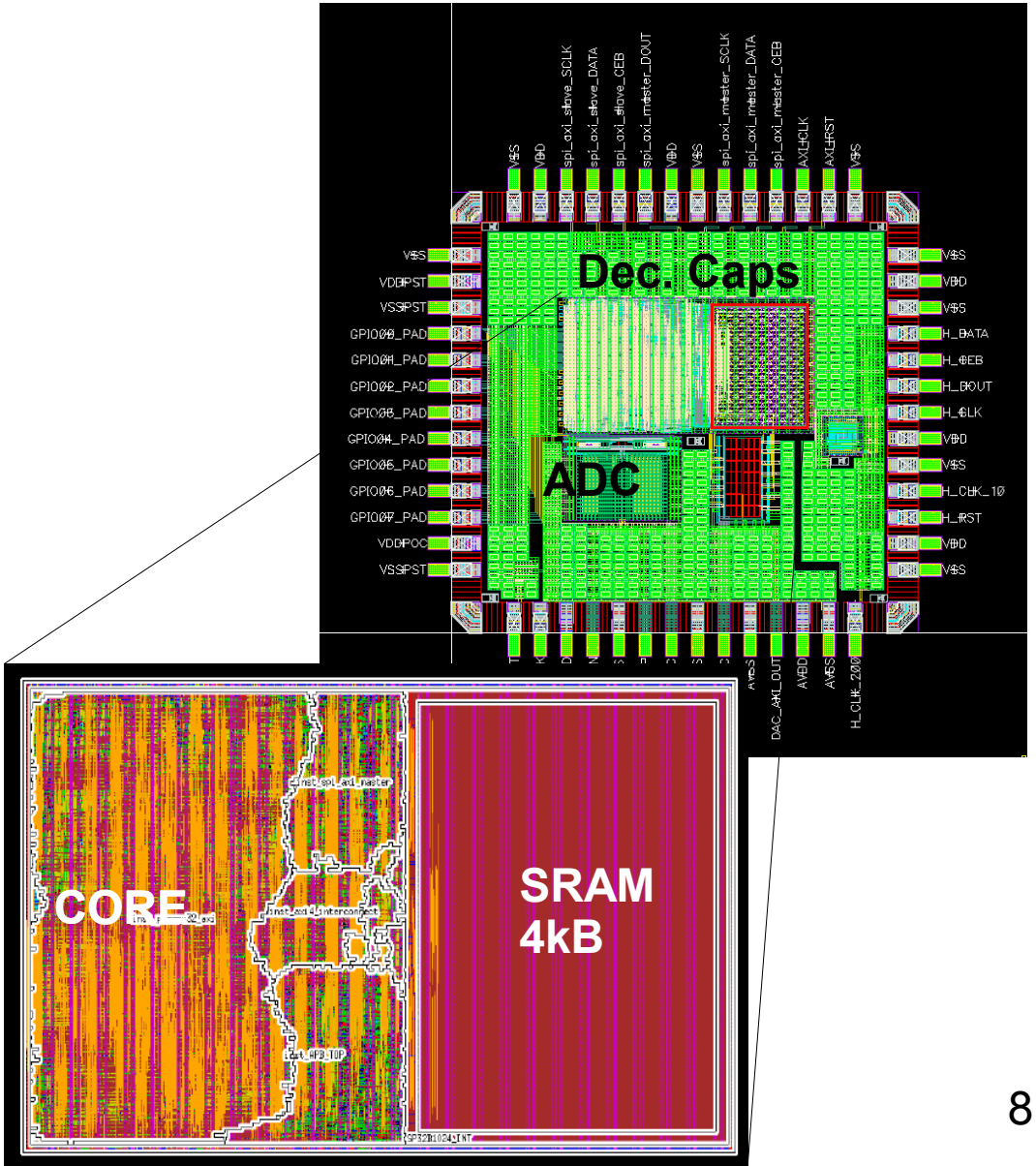
SAR ADC

- 10-bit 10MHz
- APB interface
- IRQ enabled
- Planned to be fully synthesizable → pseudo synthesized



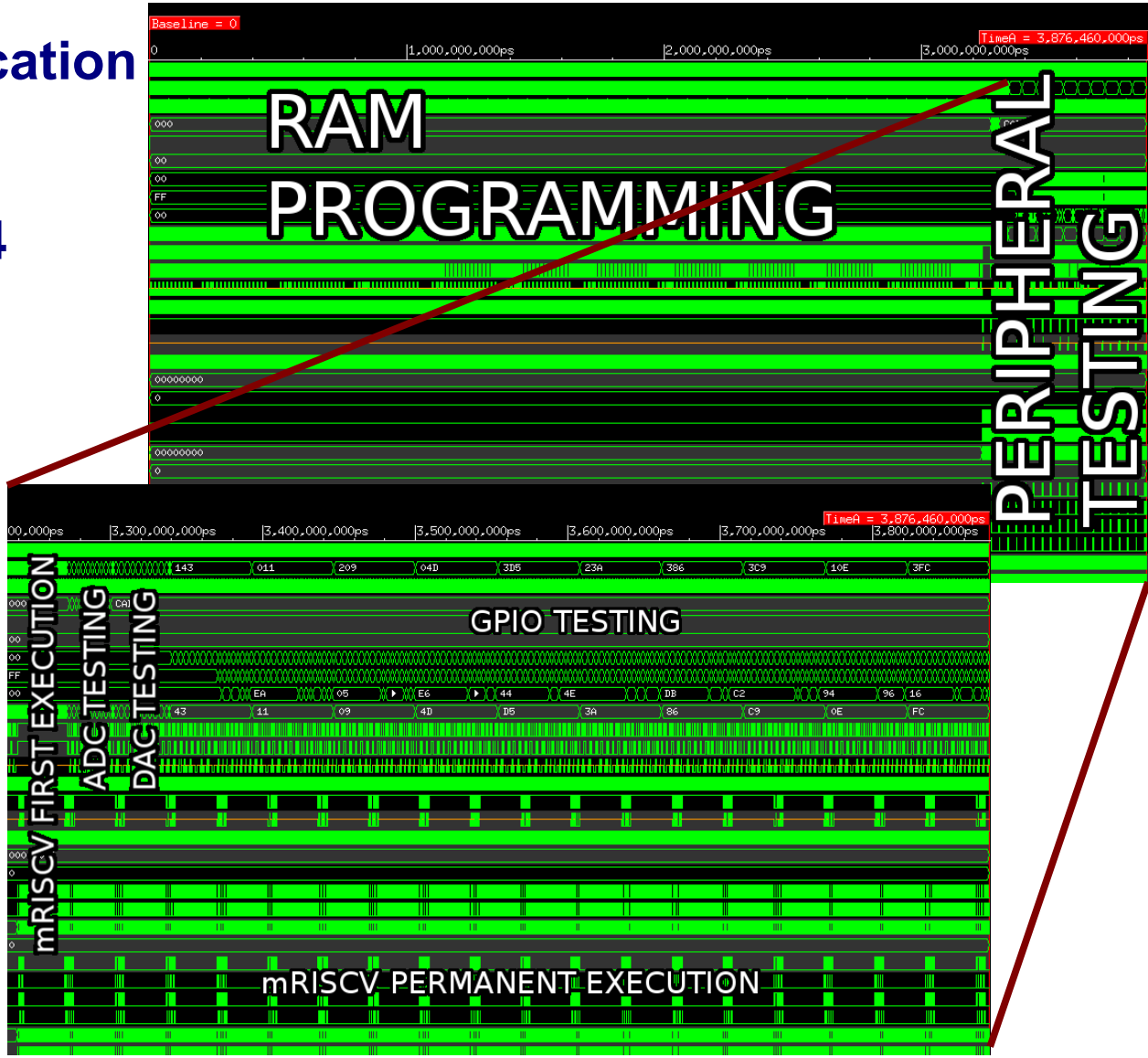
Chip

- TSMC 130nm GP
- I/O standard lib 2.5V
- Regular VT cell lib
- Tested from 10MHz to 100MHz (wc SSLHH)
- Taped-out in Oct. 2015
- Core+interfaces area: 800µm x 480µm



UVM Verification IP

- Large effort on verification
- Implemented VIP testbenches for AXI-4 and APB peripheral functionality
- Post-synthesis, post-PnR and sign-off test UVM modes
- Still work going on. We would like to partner to get proven VIP



Performance

	Z-SCALE	µRISC-V
ISA	RV32IM	RV32IM
Architecture	Single-Issue In-Order 3-stage	Single-Issue In-Order 3-stage
Process	TSMC 40nm GP	TSMC 130nm GP
Core area	0.0098 mm²	0.12 mm² !
Performance	1.35 DMIPS/MHz	0.32 DMIPS/MHz
Frequency	~500MHz	100MHz
Core Voltage	1 V	1.2 V
Dynamic Power	1.8 µW/MHz	19 µW/MHz !*

! Fully constrained clock and loads for SSLHH corner. Zero skew CTS.
*** Measured at 100MHz typical corner averaged from typical memory access execution.**

Summary

A RV32IM microcontroller-based with 10-bit ADC, DAC, timer and GPIO

Human-readable synthesizable verilog for core and AXI-4 lite, AHB lite, APB bridge and AXI-4-SPI interfaces

First effort for open source UVM VIP for RV32IM, AXI-4 lite, APB bridge

Future work on USB PHY LS interface, DMA channels, Watchdog timer, eNVM 1-poly ROM.