Raven3: 28nm RISC-V Vector Processor with On-Chip DC/DC Convertors

Brian Zimmer[1], Yunsup Lee[1], Alberto Puggelli[1], Jaehwa Kwak[1], Ruzica Jevtic[1], Ben Keller[1], Stevo Bailey[1], Milovan Blagojevic[1,2], Pi-Feng Chiu[1], Hanh-Phuc Le[1], Po-Hung Chen[1], Nicholas Sutardja[1], Rimas Avizienis[1], Andrew Waterman[1], Brian Richards[1], Philippe Flatresse[2], Elad Alon[1], Krste Asanović[1], and Borivoje Nikolić[1]

[1]University of California, Berkeley, USA

[2]STMicroelectronics, Crolles, France

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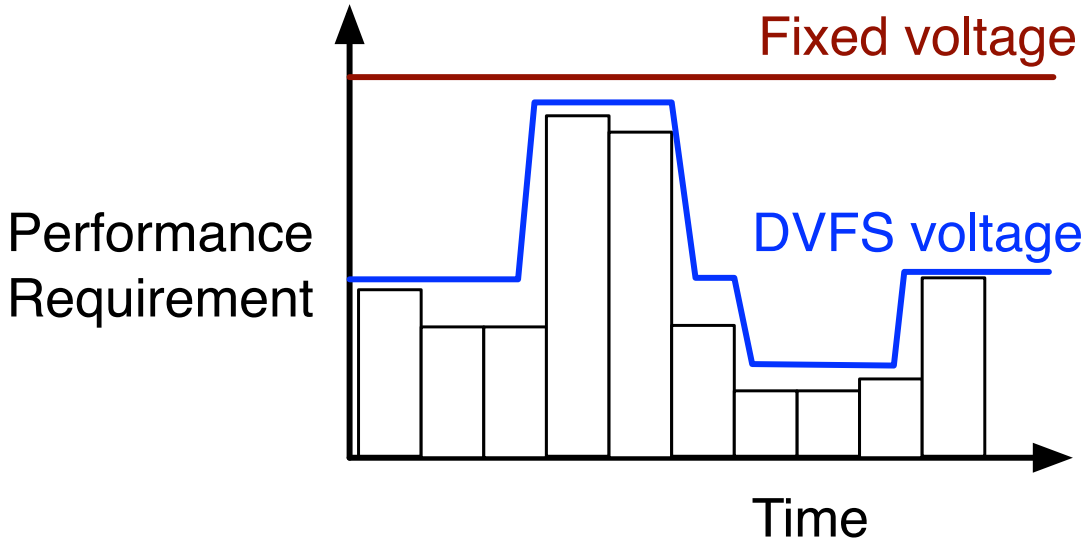
Motivation

- Dynamic voltage and frequency scaling (DVFS) maximizes energy efficiency



- Off-chip conversion
  - ✖ Slow mode transitions
  - ✖ Limited voltage domains
  - ✖ Costly off-chip components
- On-chip conversion
  - ✔ Fast transitions
  - ✔ Many domains
  - ✔ No off-chip components

Project Goals

Energy-efficient	• Fine-grained DVFS • High conversion efficiency
low-cost	• Entirely on-chip converter • Low area overhead
processor	• Runs Linux • Realistic digital load

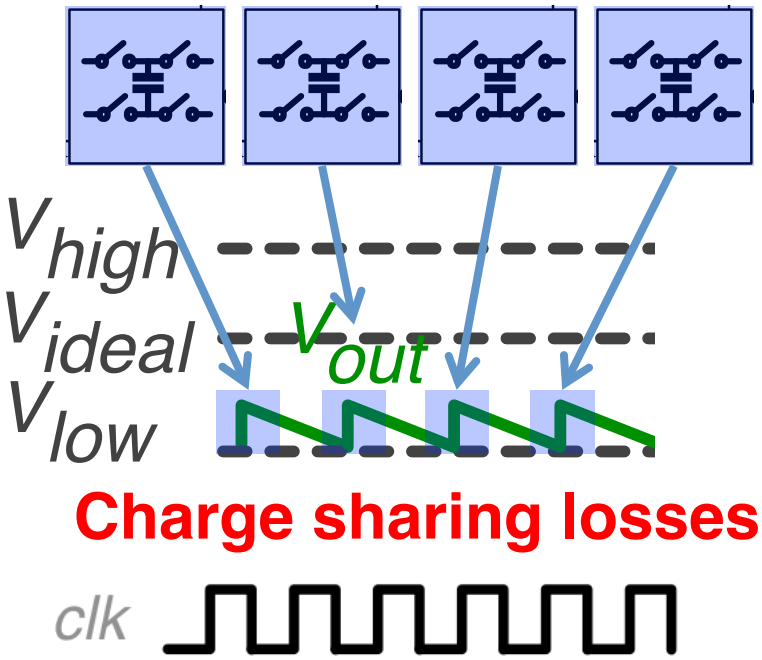
Integrated Voltage Regulators

Method	Efficiency (0.5V output)	Off-chip components	Area overhead
Linear regulator (eg. Toprak-Deniz ISSCC2014)	**<50%**		
Buck converter (eg. Kurd ISSCC2014)	**?%-90%**		
Interleaved switched-capacitor (eg. Kim ISSCC2015[1], Clerc ISSCC2015[2])	**40%-65%[1]** **65%-82%[2]**		
Simultaneous switched-capacitor with adaptive clock (Proposed)	**85%**		

Proposed Solution

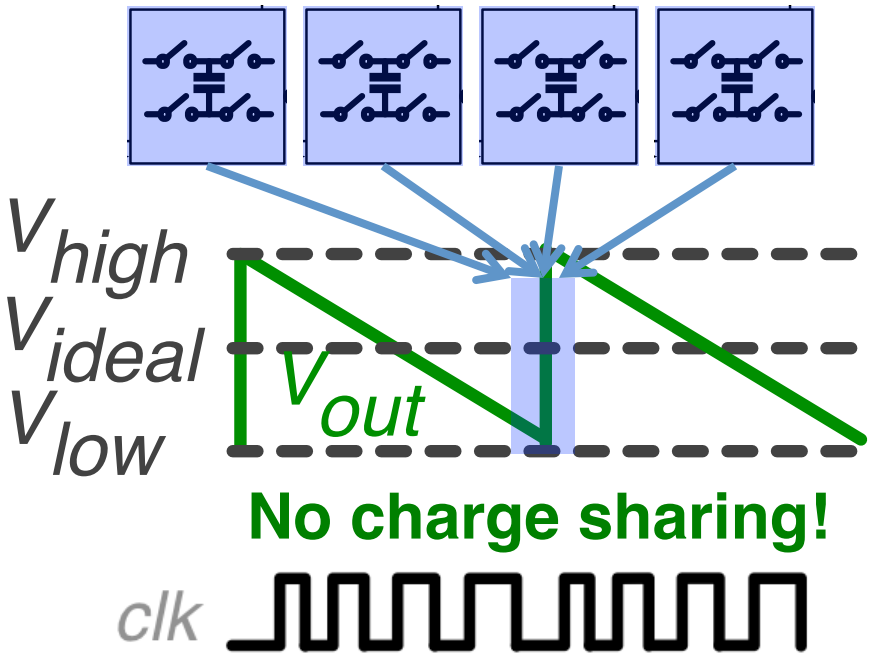
- Switch all converters simultaneously to avoid charge sharing

Traditional Interleaving



Charge sharing losses

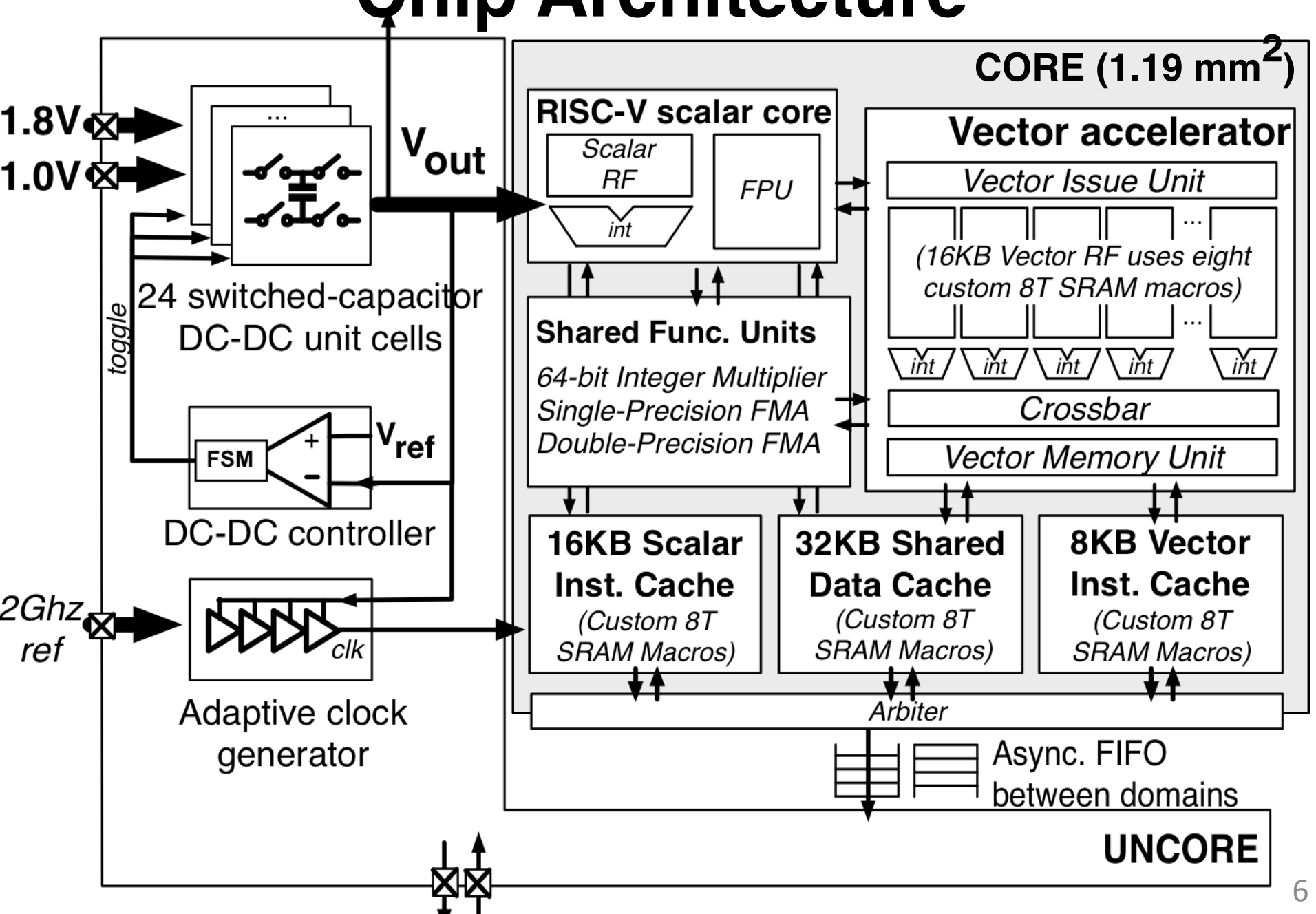
Simultaneous Switching



No charge sharing!

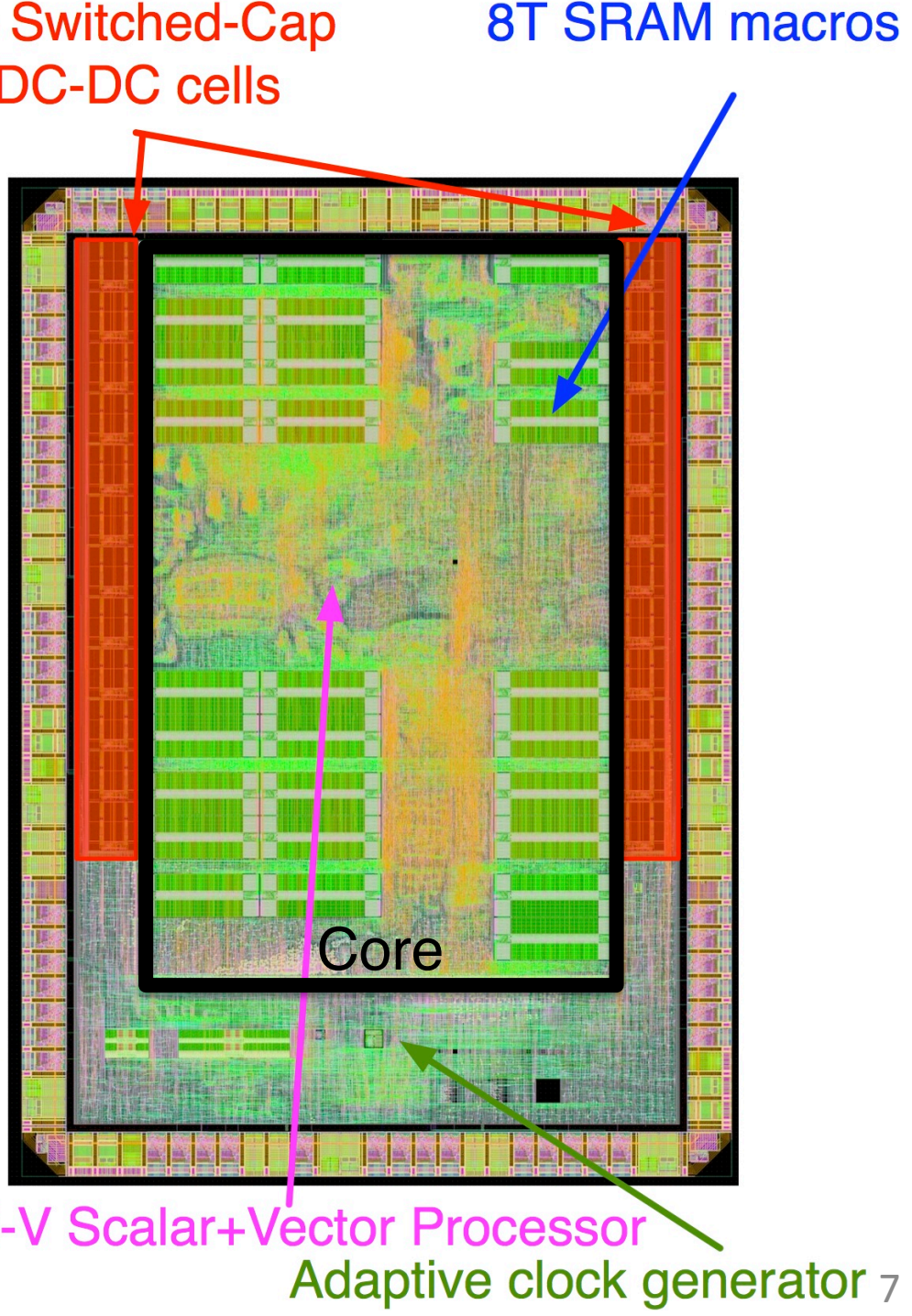
- Clock frequency adapts to track the voltage ripple

Chip Architecture



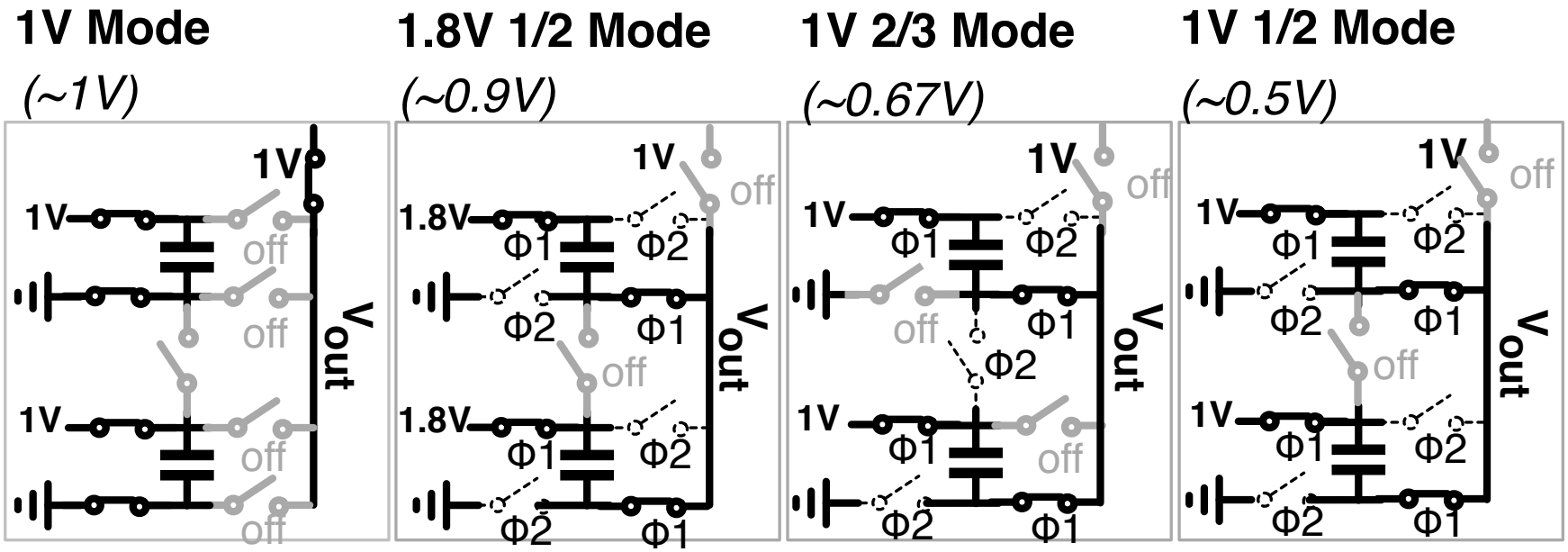
Floorplan

- ST 28nm FDSOI
- Die area: 2.37mm^2
- Core area: 1.19mm^2
- Converter area: 0.19mm^2 (16%)
- MOS+MOM (to M3) density: 11fF/μm^2

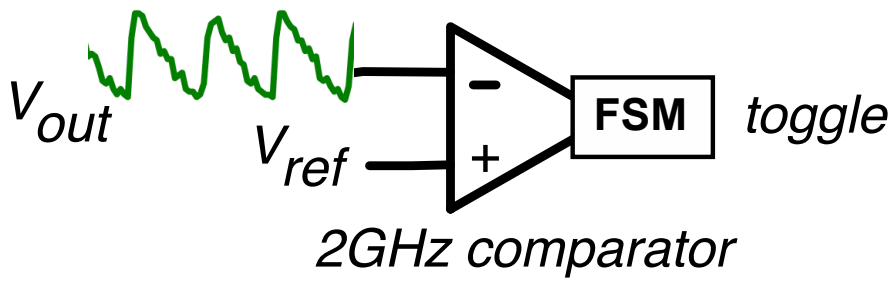


Reconfigurable SC Converters

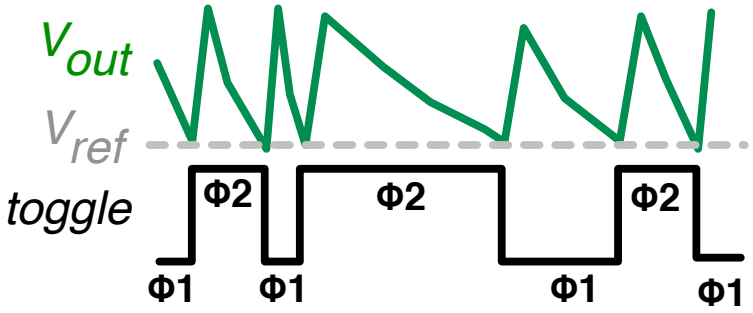
- Four output voltages, single unit cell



- Simple lower bound control

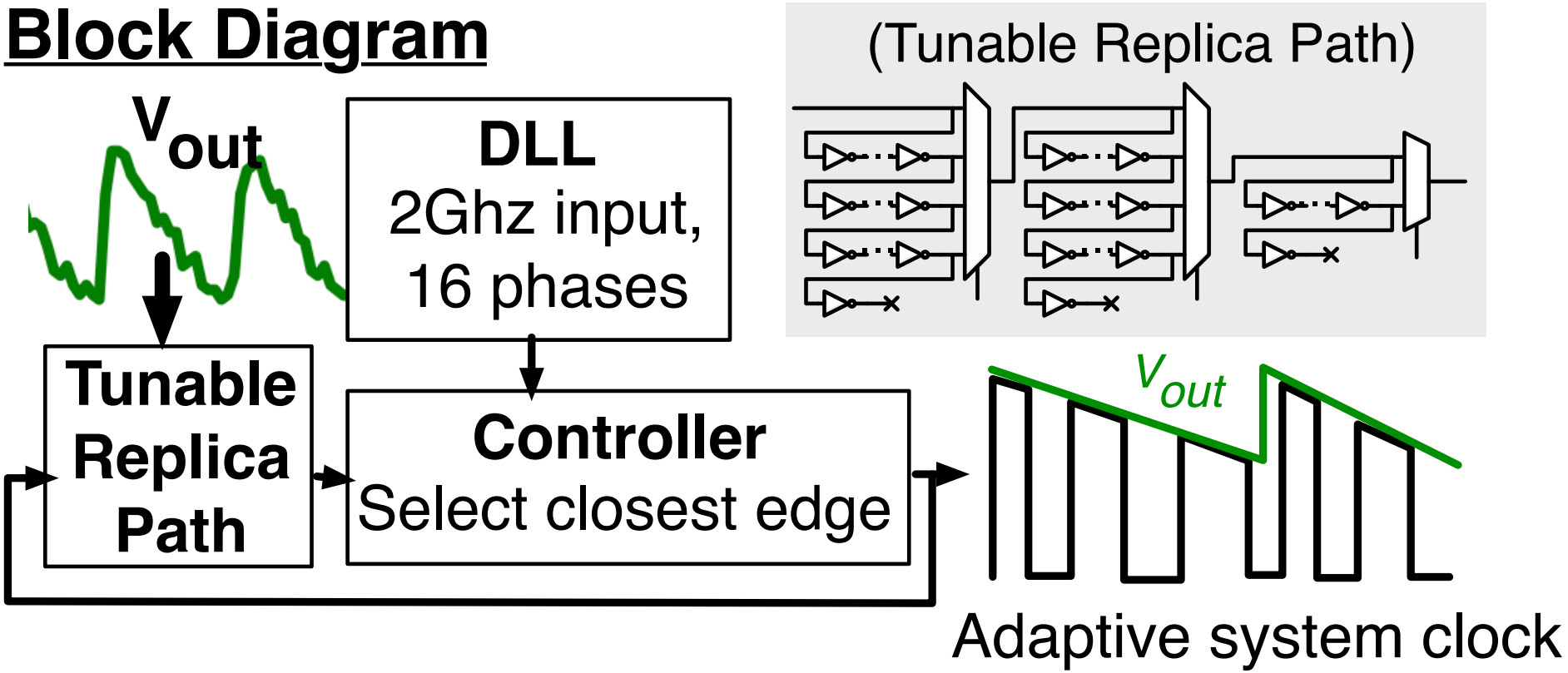


- Simultaneous switching



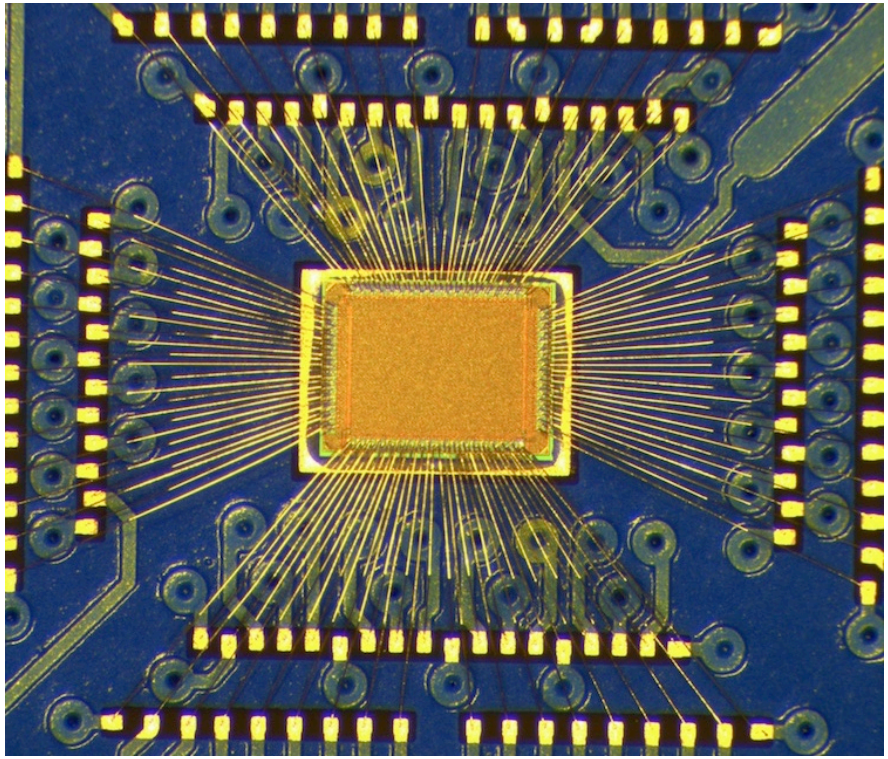
Self-Adjusting Clock Generator

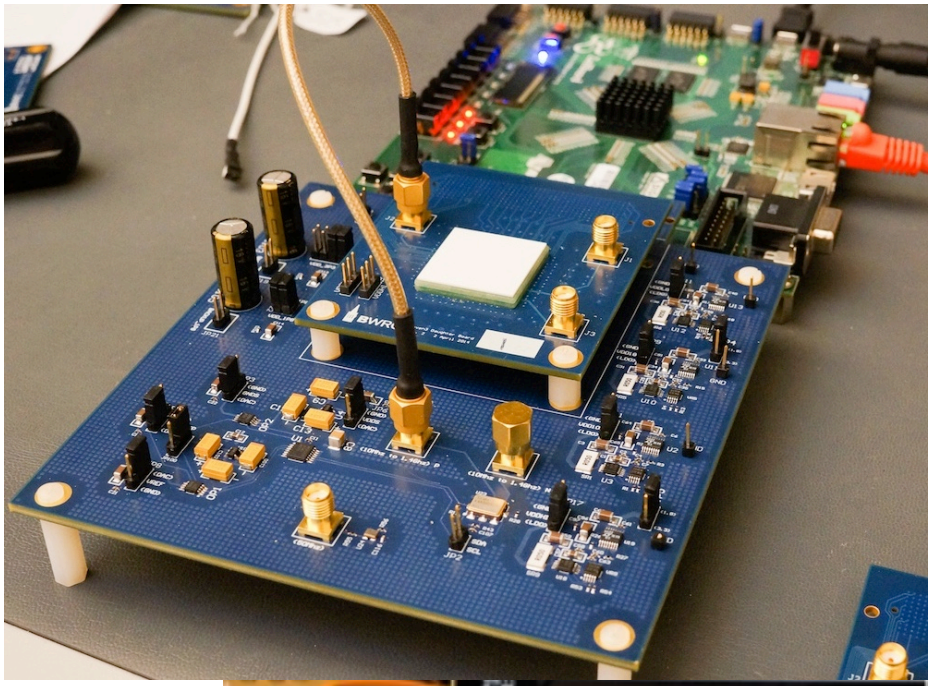
Block Diagram

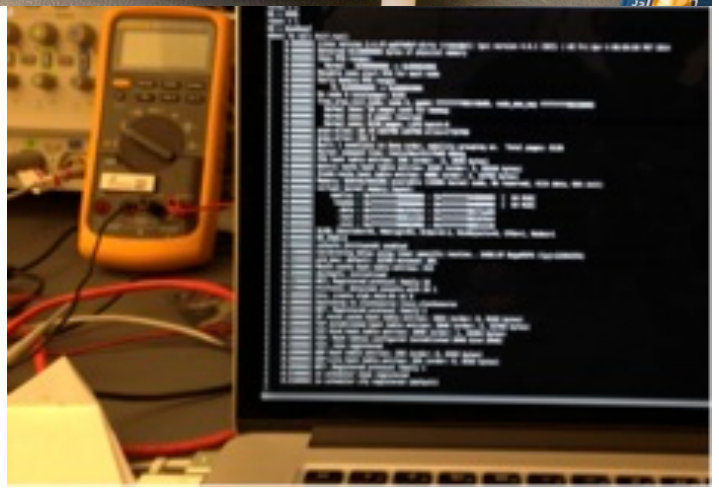


- Replica tracks critical path with voltage ripple
- Controller quantizes clock edge

Test setup

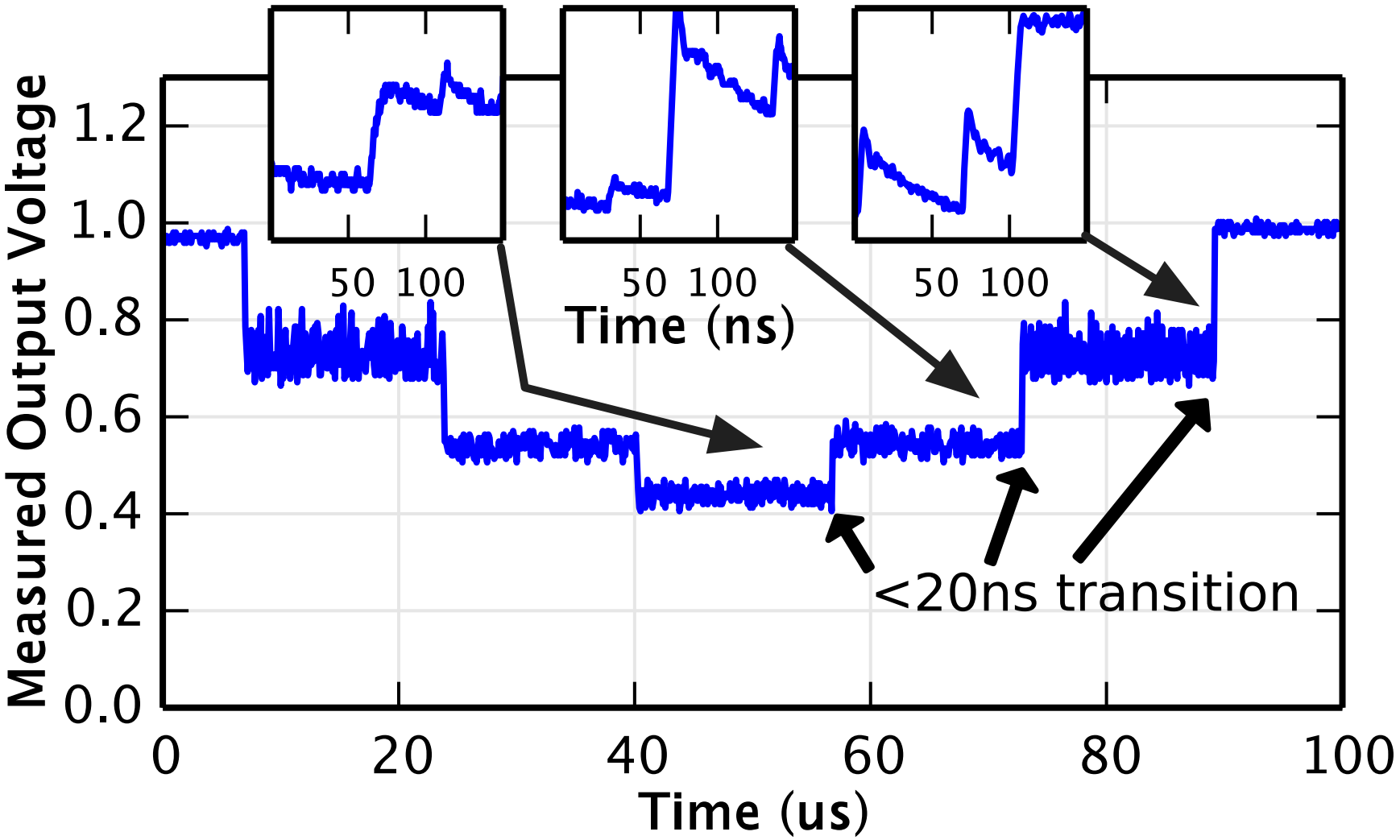






- Host: Zedboard (ARM+FPGA, network accessible)
- Motherboard: Programmable supplies
- Daughterboard: Chip-on-board

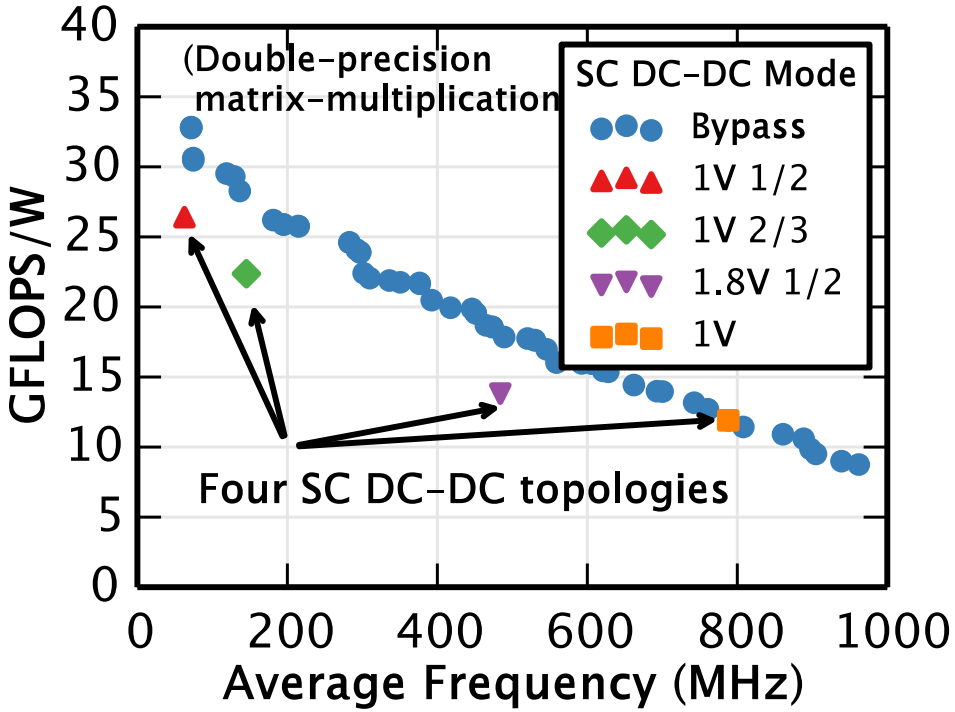
Vout Measurements

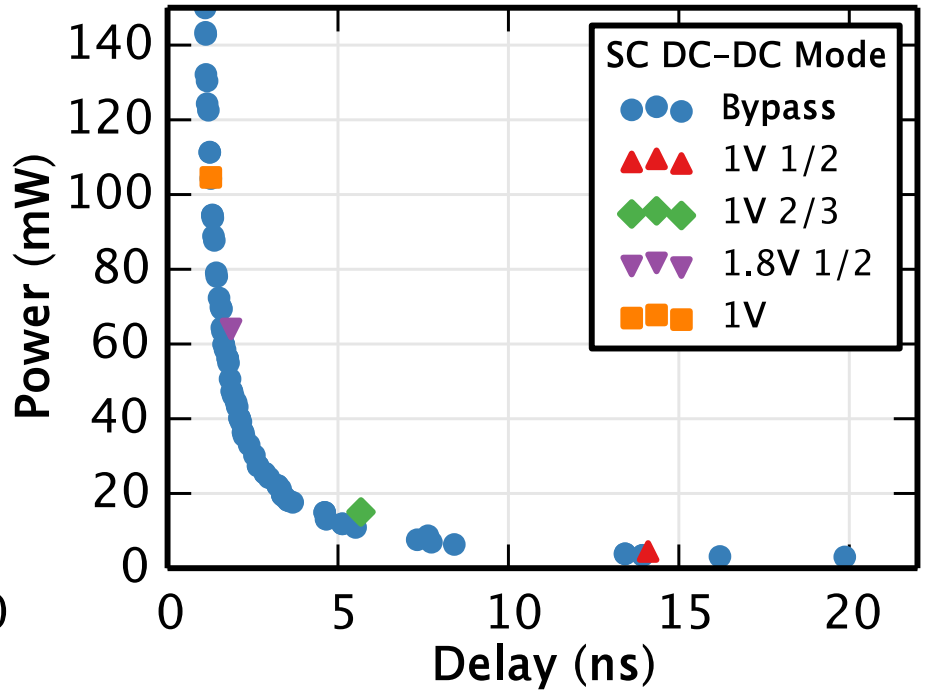


Fast converter mode transitions enable extremely fine-grain DVFS algorithms

GFLOPS/W

- Double-precision matrix-multiplication used as energy-efficiency metric
- GFLOPS/W inverse of energy/operation





28nm FDSOI offers high energy efficiency and 4 converter modes cover wide operating range

Conclusion

Energy-efficient 28nm processor featuring:

1. **Fine-grained and wide-range DVFS**
   - 20ns transitions
   - 1V to 0.45V
2. **Entirely on-chip voltage conversion**
   - Simultaneous switched-capacitor
3. **High efficiency**
   - 80% across wide voltage range
4. **Extreme energy efficiency**
   - 26 GFLOPS/W with on-chip conversion

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