AURIX™ 32-bit Microcontroller family

Performance meets Safety

- 11.09.2018 Karlsruhe
- 12.09.2018 München
- 13.09.2018 Hanover

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Field Application Engineer, Automotive Microcontroller

Agenda

1. TriCore in the CAV market
2. Aurix 1G Overview
3. Aurix 1G Derivatives
4. Aurix 2G Introduction
5. Aurix Safety Features
6. Aurix SW

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AURIX™ – one family multiple use cases

Target application segments

Chassis Control

Safety

Autonomous Driving

Connected Car

Powertrain

eMobility

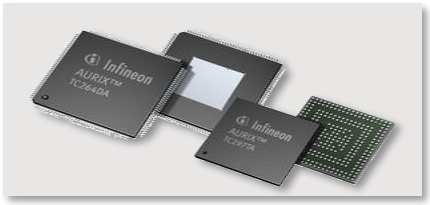
Industrial & MultiMarket

CAV

Beyond classic ATV segments

AURIX™ versatile architecture for various CAV applications

AURIX™ – Safety joins Performance



NG Forklift ECU Platform
Key Selling Points:
Performance, Safety & CAN FD

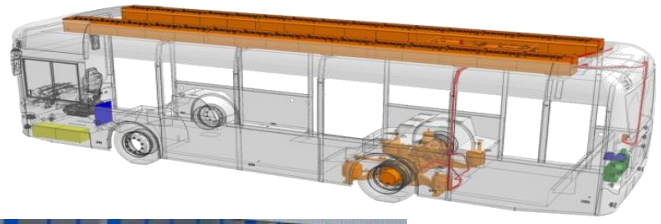
CAN Ethernet Gateway
Key Selling Points:
Performance, CAN FD, scalability

Various other applications
Key Selling Points:
Performance, Scalability, Safety , ext. SRAM

AURIX™ for CAV Success Stories

Infineon's focus applications in CAV

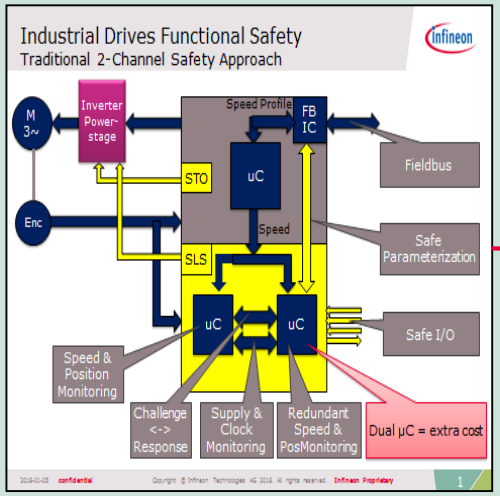
- Hybrid and fully **electric drive train**
- **DC Chargers** for fast battery charging
- **Replacing hydraulic drives** using electric motors
- **Air conditioning and Climate Control** at >10kW
- **Auxiliary drives** for tools Harvester/Mixer/Brushes/Chain Saw
- **Local, grid-like Power Supply** 220V/50Hz 1~ or 380V/50Hz 3~



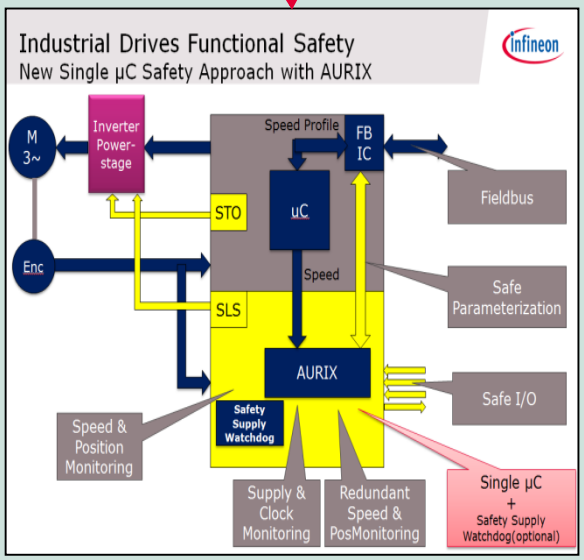
Climate Control

Success story of motor control
Project: safe servo drive with AURIX™

Application diagram



Significant cost savings with AURIX™



Success factors

- Reduction of BOM cost:
  - 1x MCU with lockstep supporting IEC61508 safety level up to SIL-3 replacing Dual channel with 2x MCU
- High calculation performance:
  - 2 cores fully loaded by motor control
  - 1 core drive based PLC & motion control
- Different variants of drive portfolio
  - scalable IFX µC portfolio with AURIX™
- Long-term availability of µC

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Infineon's AURIX™ µC powered by Tricore™
Highest 32-bit Automotive Performance

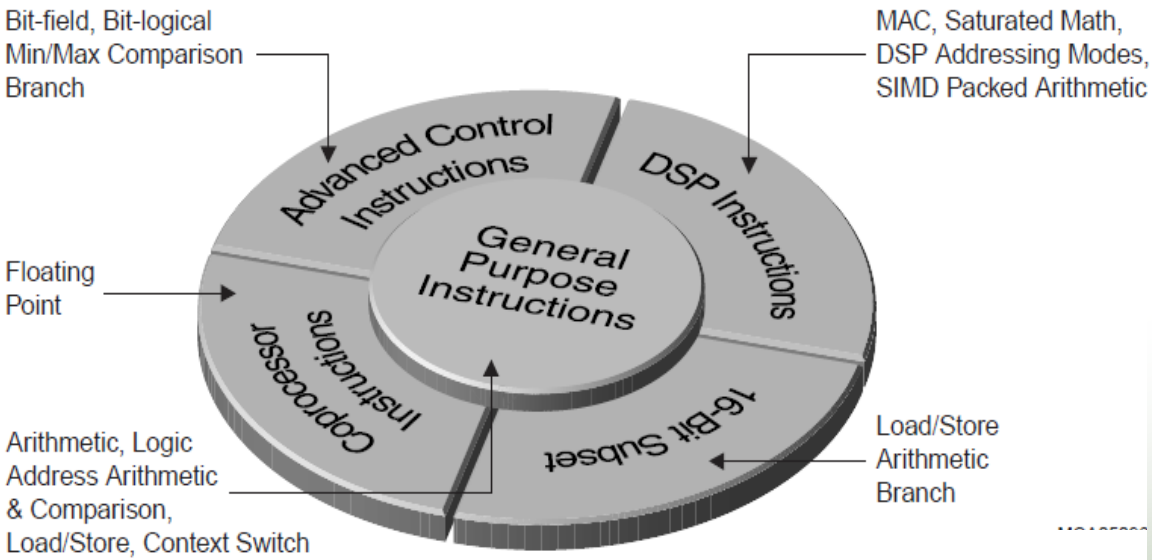
Three in one

Microcontroller

RISC processor

DSP

TriCore™ UNIFIED PROCESSOR



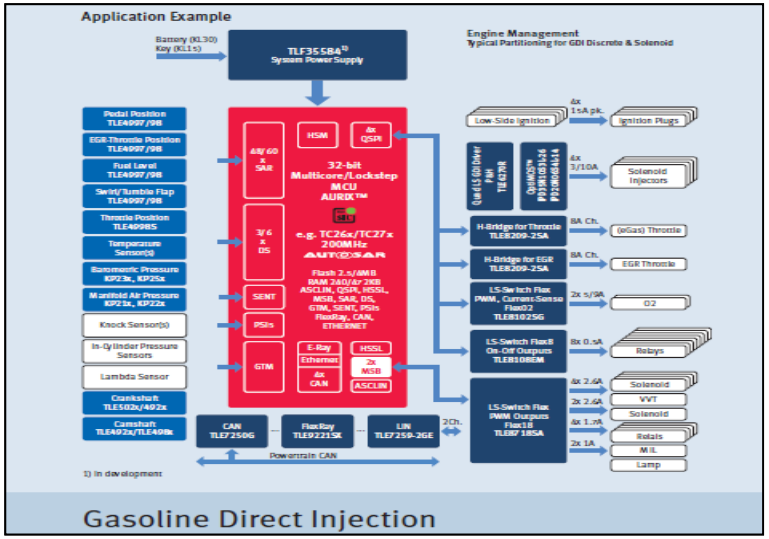
Microcontroller Features/Highlights
- Fast context switch
- Fast interrupt response
- Low code size through use of 16-bit and 32-bit instructions
- Powerful bit manipulation unit
- Powerful comparison instructions
- Integrated peripheral support

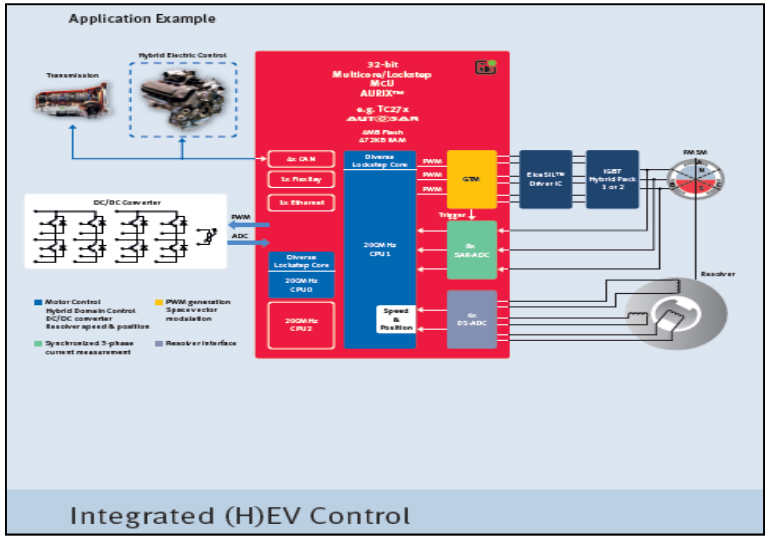
DSP Features/Highlights
- Sustainable single-cycle dual MAC
- Packed/SIMD instructions
- DSP addressing modes
- Zero overhead loops
- Saturation
- Rounding
- Q-Math (fraction format)

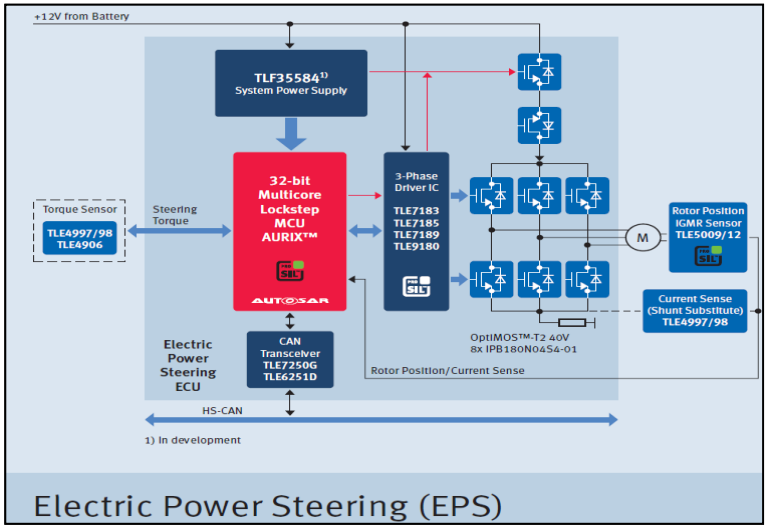
RISC Processor Features/Highlights
- 32-bit load/store Harvard architecture
- Super-scalar execution
- 4 or 6 stage pipelines (TC16E/P)
- Uniform register set
- Single data-memory model
- fine grain Memory protection (MPU)
- C/C++ and RTOS support

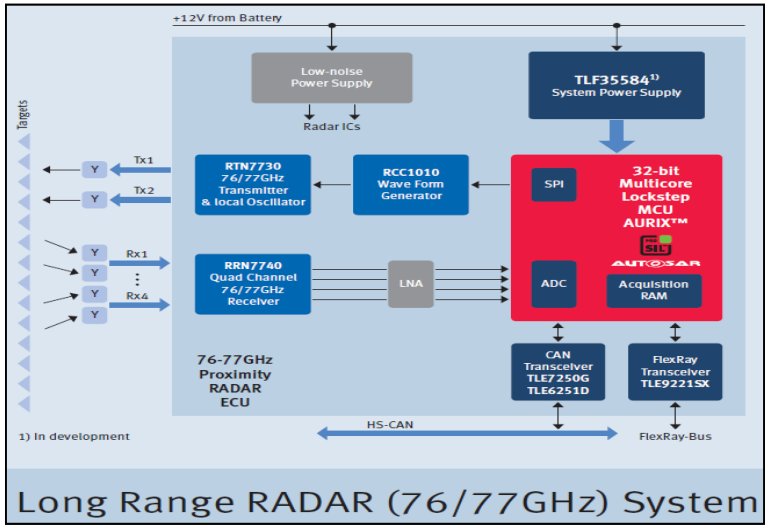
One Family - scalable across application

Most scalable 32-bit MCU portfolio on the market









SAFETY: Complete Solution for Safety up to ASIL-D

SECURITY: Integrated hardware support for Security

24V EHPS for trucks

Load dump protection

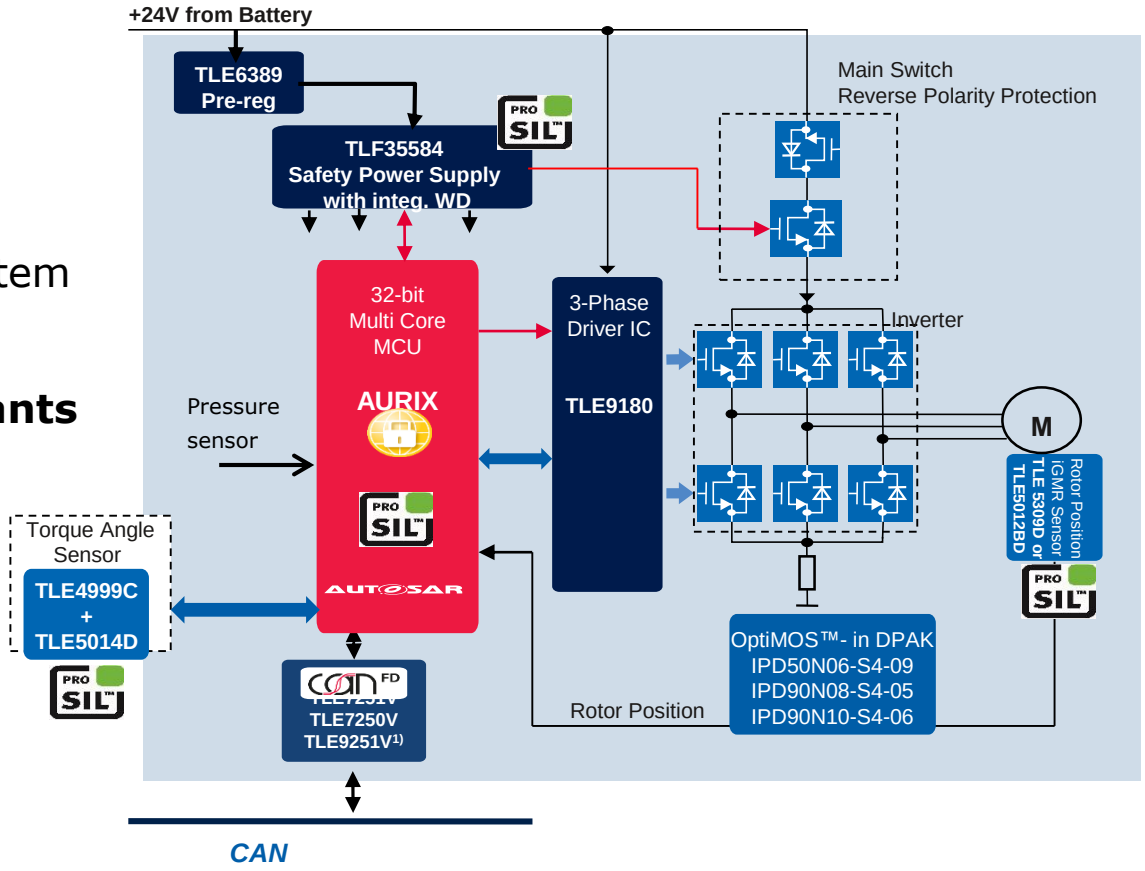
- Active clamping
- Pre-regulator (TLE6389)

› Same safety concept as 12V system

Scalable MCU family for all variants

- basic EHPS
- Variable steering assist
- Up to EHPS with lane assist (security over CAN)

› Proven platform for EPS and EHPS



IFX Microcontroller Chassis/Safety Roadmap

future proof roadmap guarantees joint success story

16 MByte
8 Mbyte
4 Mbyte
<= 2 Mbyte

Nomenclature:

Device Name
#/LS# cores/freq
Flash/SRAM size
Acclerators

Umbrella device

TC39xX
6x/4x 300MHz
16MB/6528kB

TC29xT
3x/1x 300MHz
8MB/728kB
HSM

TC29xT N
3x/1x 300MHz
8MB/728kB
HSM

CAN FD DIS 2015

Premium ESC
Chassis domain control

TC27xT
3x/2x 200MHz
4MB/472kB
HSM

TC27xT N
3x/2x 200MHz
4MB/472kB
HSM

High-end ESC
Suspension
Safety domain control

TC26xD
2x/1x 200MHz
2,5MB/240kB

TC26xD N
2x/1x 200MHz
2,5MB/240kB

Standard ESC
Power Steering
Airbag
ABS

TC23xL
1x/1x 200MHz
2MB/192kB
HSM

TC23xL N
1x/1x 200MHz
2MB/192kB
HSM

TC21/2xL
1x/1x 133MHz
1MB/96kB

TC22xL N
1x/1x 133MHz
1MB/96kB

AURIX™ TC2xx Family

TC39xP
6x/4x 300MHz
16MB/2528kB
HSM+

Premium ESC
(AEB+Full speed)
Autonomous
Braking/Steering

TC38xQ
4x/2x 300MHz
10MB/1376kB
HSM+

Chassis domain
control
Power Steering incl.
OTA

TC37xT
3x/2x 300MHz
6MB/992kB
HSM+

Main ESC
Integrated brake
systems
HE Power
Steering

TC36xD
2x/2x 200MHz
4MB/576kB
HSM+

Suspension
Safety domain
control

TC33xL
1x/1x 200MHz
2MB/248kB
HSM+

Low-cost ESC
Power steering
Airbag

TC32xL
1x/1x 160MHz
1MB/152kB
HSM+

AURIX™ TC3xx Family

TC4xxx
32MB/8MB

Chassis Control
Autonomous driving

TC4xxx
16MB/4MB

Adv. ESC controller
Adv. EPS incl. OTA
Domain control

TC4xxx
8MB/2MB

ESC controller
EPS controller
Domain control

TC4xxx
4MB/1MB

Restraint
EPS
ESCL

AURIX™ TC4xx Family

Concept Phase

Available 2016 2017 2018 2019 2020 beyond 2021

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AURIX™ TC2xx portfolio

From low cost to high performance applications

Flash / Package	TQFP 80	TQFP 100	T/LQFP 144	LQFP 176	LFBGA 292	BGA 416	LFBGA 516
9x Series 8 MB					TC297T 300MHz	TC298T 300MHz	TC299T 300MHz
7x Series 4 MB				TC275T 200 MHz	TC277T 200MHz		
6x Series 2.5 MB			TC264D 200 MHz	TC265D 200 MHz	TC267D 200 MHz		
3x Series 2 MB		TC233L 200 MHz	TC234L 200 MHz		TC237L 200 MHz		
2x Series 1 MB	TC222L 133 MHz	TC223L 133 MHz	TC224L 133 MHz				
1x Series 512 kB	TC212L 133 MHz	TC213L 133 MHz	TC214L 133 MHz				

Hardware security enabled

All devices CAN FD enabled based on DIS2015

L - Single Lockstep Core
D - Dual Core
T - Triple Core

System solution
- AURIX Microcontroller
- Pre-driver & MOSFETs
- Power supply

MCU Scalability
- Performance & Flash
- Software compatibility
- Pin-compatibility
- Diverse timer architecture

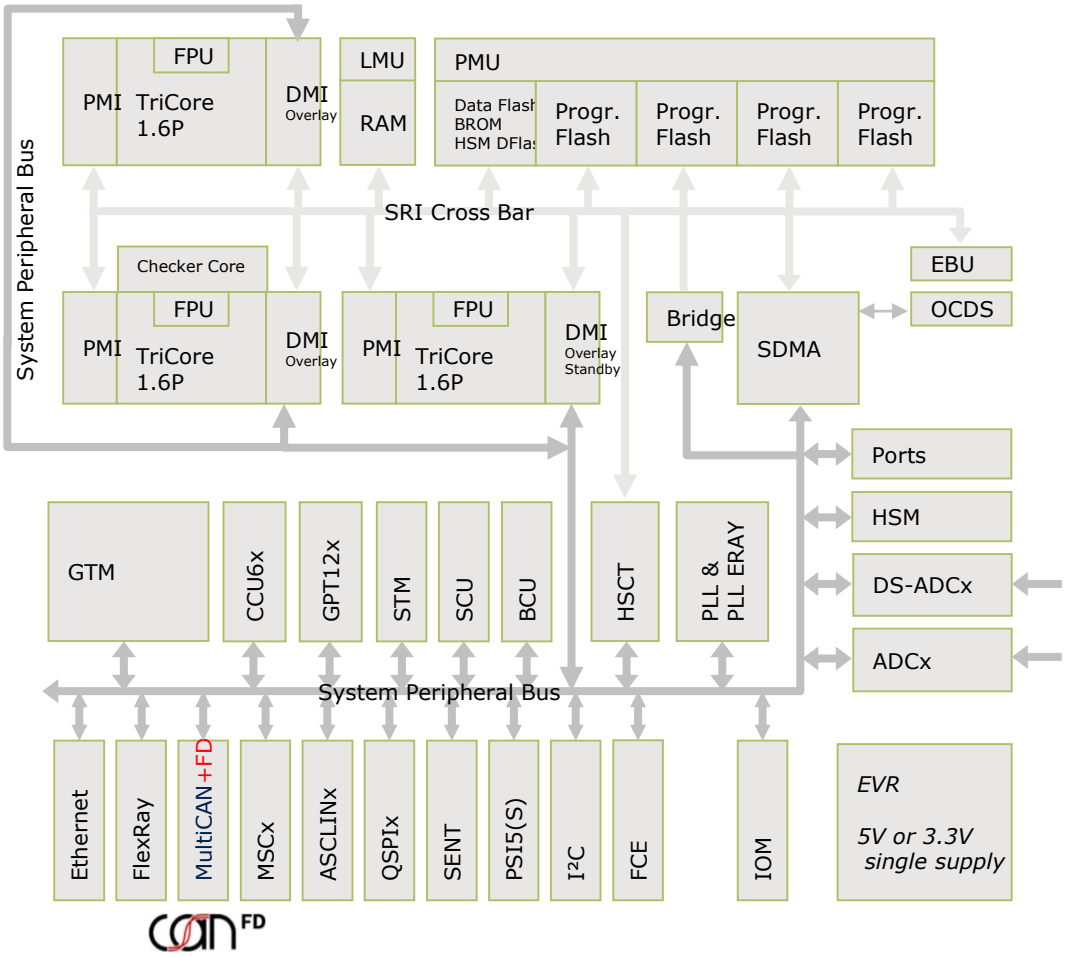
Power Consumption
- On-chip DC/DC high-efficiency power supply

Safety/Security Concept
- ISO26262 compliance
- HW redundancy options
- Hardware security support

9x Series – Umbrella Device

SAK-TC29xTP-128F300

Feature Set		9x Series
TriCore 1.6P	# Cores / Checker	3 / 1
	Frequency [2]	2x300 / 1x200[2] MHz
Flash	Program Flash	8 MB
	EEProm @ w/e cycles	128 KB @ 500k
SRAM	Total (DMI , PMI, LMU)	728 KB
DMA	Channels	128
ADC	Modules 12bit / DS	11 / 10
	Channels 12bit / DS	84 / 10 diff
Timer	GTM Input / Output	48 / 152 channels
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	2 / 4
	CAN FD[3] (nodes/obj)	6 / 384
	QSPI / ASCLIN / I2C	6 / 4 / 2
	SENT / PSI5 / PSI5S	15 / 5 / 1
	HSCT / MSC / EBU	1 / 3 diff LVDS / 1
	Other	Ethernet MAC
Safety	SIL Level	ASIL-D
Security	HSM	Yes
Power	EVR	Yes
	Standby Control Unit	Support



Package Variants

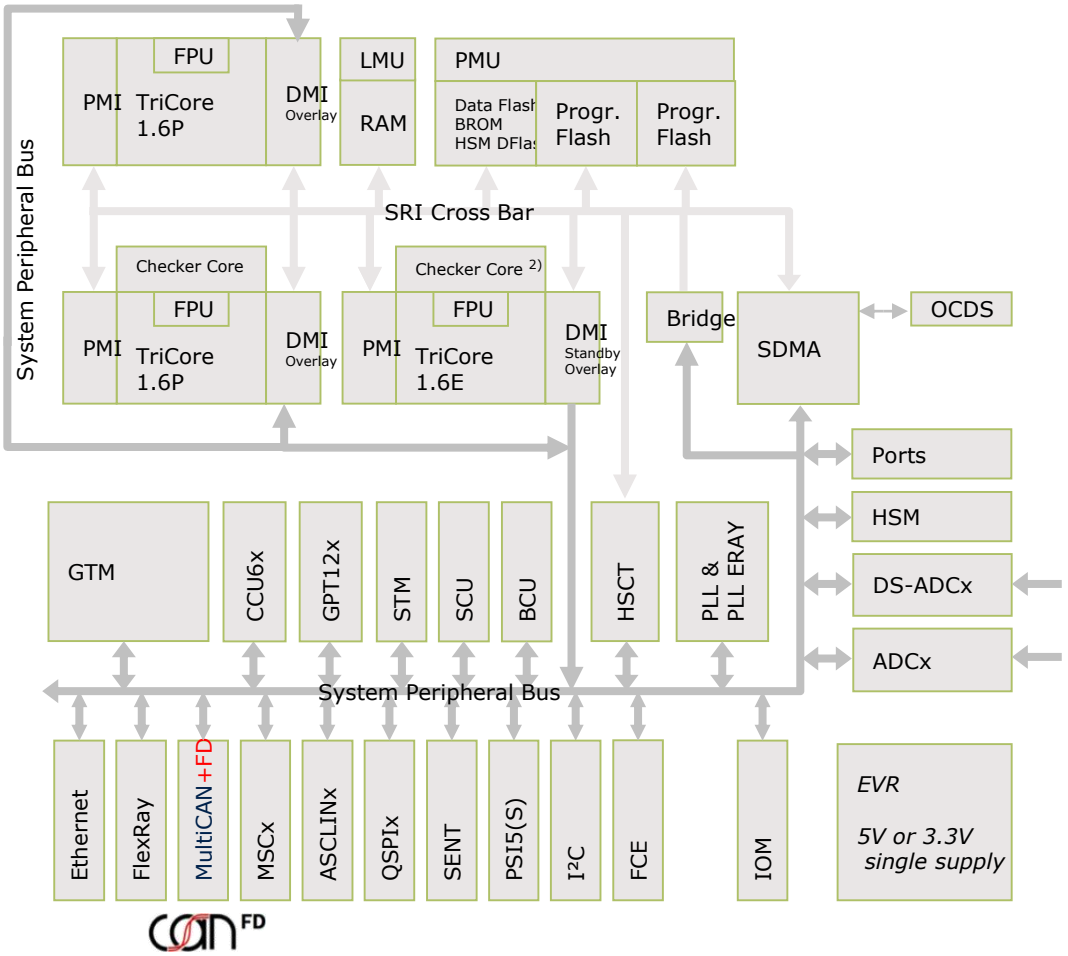
LFBGA-516	BGA-416	LFBGA-292	Bare Die
0.8mm	1.0mm	0.8mm	
-40°C to +125°C, [1]	-40°C to +125°C [1]	-40°C to +125°C [1]	T_{jmax} 170°C,
84 ADC inputs	60 ADC inputs	60 ADC inputs	84 ADC inputs

1) *Grade 0 option available on request with specific limitations for Ta=150°*
2) *High performance version with 3x300MHz on request with specific limitations*
3) *Option: CAN FD*

7x Series – Umbrella Device

SAK-TC27xTP-64F200

Feature Set		7x Series
TriCore 1.6P	# Cores / Checker	2 / 1
	Frequency	200 MHz
TriCore 1.6E	# Cores / Checker	1 / 1
	Frequency	200 MHz
Flash	Program Flash	4 MB
	EEProm @ w/e cycles	64 KB @ 500k
SRAM	Total (DMI , PMI)	472 KB
DMA	Channels	64
ADC	Modules 12bit / DS	8 / 6
	Channels 12bit / DS	60 / 6 diff
Timer	GTM Input / Output	32 / 88 channels
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	1 / 2
	CAN-FD[3] (nodes/obj)	4 / 256
	QSPI / ASCLIN / I2C	4 / 4 / 1
	SENT / PSI5 / PSI5S	10 / 3 / 1
	HSCT / MSC / EBU	1 / 2 diff LVDS / -
	Other	Ethernet MAC
Safety	SIL Level	ASIL-D
Security	HSM	Optional
Power	EVR	Yes
	Standby Control Unit	Support



Package Variants

LFBGA-292
0.8mm
-40°C to +125°C [1]
60 ADC inputs

LQFP-176
0.5mm
-40°C to +125°C [1]
48 ADC inputs

Bare Die
T_{jmax} 170°C
60 ADC inputs

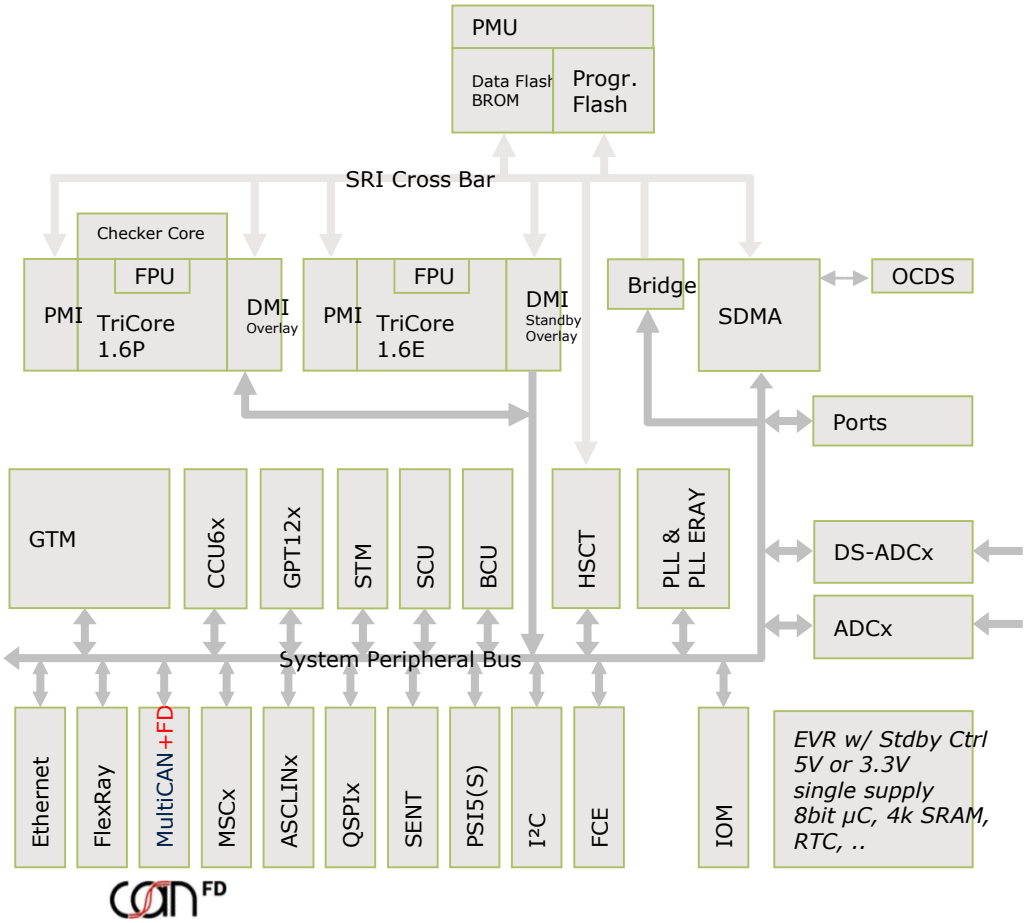
1) *Grade 0 option available on request with specific limitations for Ta=150°*
2) *Option: CAN FD*

6x Series – Umbrella Device

SAK-TC26xD-40F200

Feature Set		6x Series
TriCore 1.6P	# Cores / Checker	1 / 1
	Frequency	200 MHz
TriCore 1.6E	# Cores / Checker	1 / -
	Frequency	200 MHz
Flash	Program Flash	2.5 MB
	EEProm @ w/e cycles	16 KB @ 500k
SRAM	Total (DMI , PMI)	240 KB
DMA	Channels	48
ADC	Modules 12bit / DS	4 / 3
	Channels 12bit / DS	50 / 3 diff
Timer	GTM Input / Output	24 / 64 channels
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	1 / 2
	CAN FD[2] (nodes/obj)	5 / 256
	QSPI / ASCLIN / I2C	4 / 4 / 1
	SENT / PSI5 / PSI5S	6 / 2 / 1
	HSCT / MSC / EBU	1 / 2 diff LVDS / -
	Other	Ethernet MAC
Safety	SIL Level	ASIL-D
Security	HSM	No
Power	EVR	Yes
	Standby Control Unit	Yes

1) *Grade 0 option available on request with specific limitations for Ta=150°*
2) *Option: CAN FD*



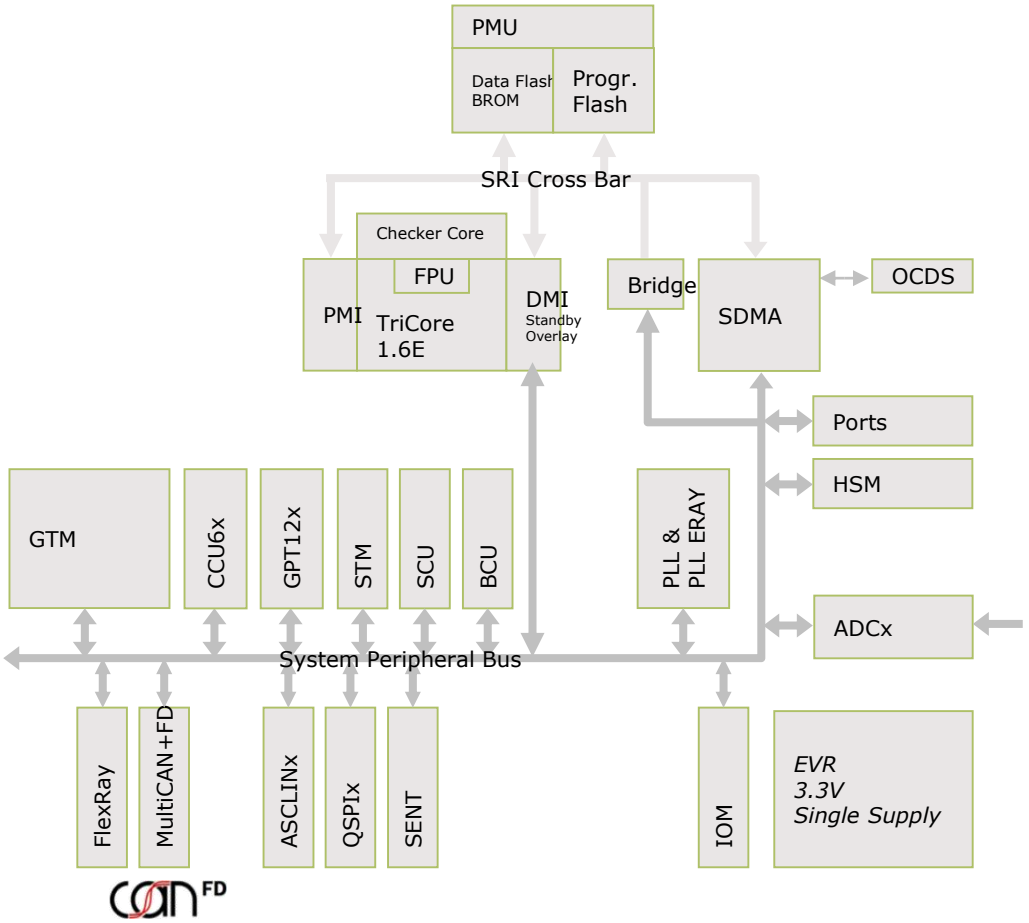
Package Variants

LFBGA-292	LQFP-176	LQFP-144	Bare Die
0.8mm	0.5mm	0.5mm	
-40°C to +125°C 1)	-40°C to +125°C [1]	-40°C to +125°C [1]	T_{jmax} 170°C
50 ADC inputs	50 ADC inputs	40 ADC inputs	50 ADC inputs

3x Series – Umbrella Device

SAK-TC23xLP-32F200

Feature Set		3x Series
TriCore 1.6P	# Cores / Checker	- / -
	Frequency	-
TriCore 1.6E	# Cores / Checker	1 / 1
	Frequency	200 MHz
Flash	Program Flash	2 MB
	Data Flash	128k , 125 k cycles
SRAM	Total (DMI, PMI)	192 KB
DMA	Channels	16
ADC	Modules 12bit / DS	2 / -
	Channels 12bit / DS	24 / -
Timer	GTM Input / Output	8 / 32
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	1 / 2
	CAN FD[3)] (nodes/obj)	6 / 256
	QSPI / ASCLIN / I2C	4 / 2 / -
	SENT / PSI5	4 / -
	HSCT/ MSC / EBU	- / - / -
	Other	-
Safety	SIL Level	ASIL-D
Security	HSM	Optional
Power	EVR	Yes
	Standby Control Unit	WUT + SRAM



Package Variants

TQFP-144	TQFP-100	LFBGA-292
0.4mm	**0.4mm**	**0.8mm**
-40°C to +125°C [1)]	-40°C to +125°C [1)]	-40°C to +125°C [1)]
24 ADC inputs	24 ADC inputs	24 ADC inputs

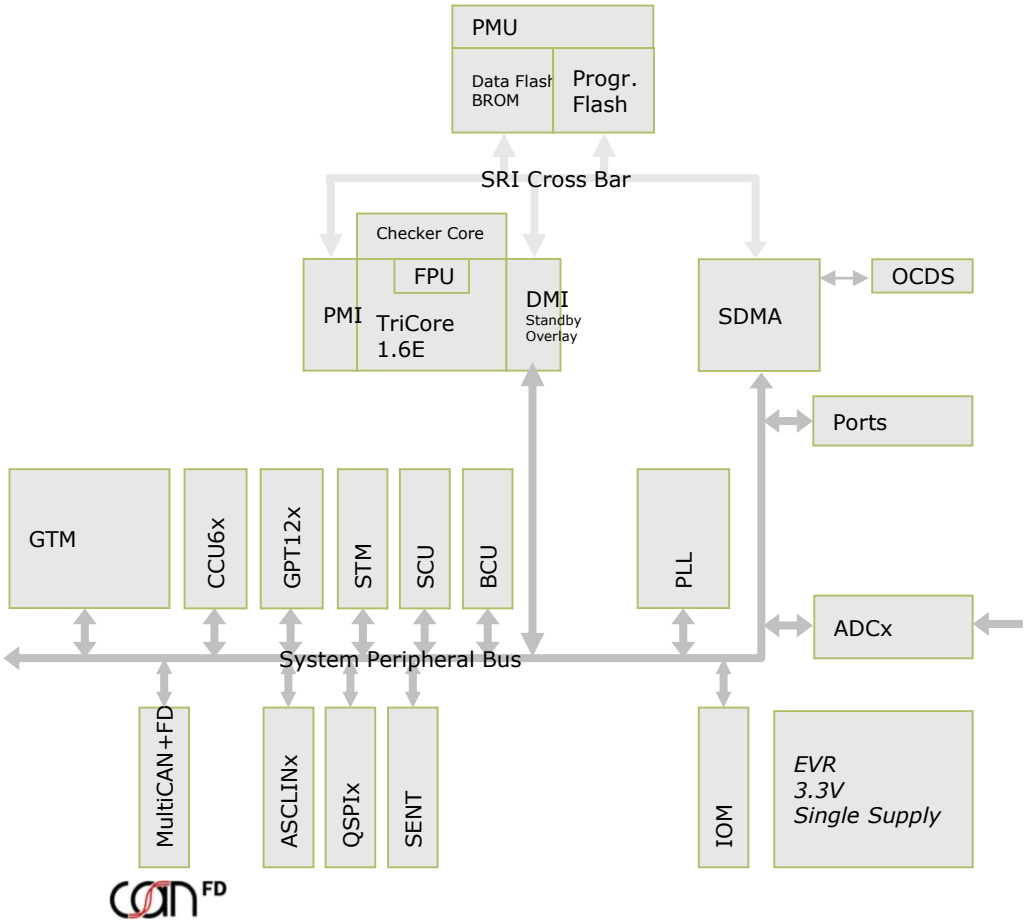
1) *Grade 0 option available on request with specific limitations for Ta=150°*
2) *Option: CAN FD*

2x Series – Umbrella Device

SAK-TC22xL(S)-16F133

Feature Set		2x Series
TriCore 1.6P	# Cores / Checker	- / -
	Frequency	-
TriCore 1.6E	# Cores / Checker	1 / 1 (1 / 0)
	Frequency	133 MHz
Flash	Program Flash	1 MB
	Data Flash	96k, 125k cycles
SRAM	Total (DMI, PMI)	96 KB
DMA	Channels	16
ADC	Modules 12bit / DS	2 / -
	Channels 12bit / DS	24 / -
Timer	GTM Input / Output	8 / 32
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	-
	CAN FD[2)] (nodes/obj)	3 / 128
	QSPI / ASCLIN / I2C	4 / 2 / -
	SENT / PSI5	4 / -
	HSCT/ MSC / EBU	- / - / -
	Other	-
Safety	SIL Level	ASIL-D
Security	HSM	No
Power	EVR	Yes
	Standby Control Unit	WUT + SRAM

1) *Grade 0 option available on request with specific limitations for Ta=150°*



Package Variants

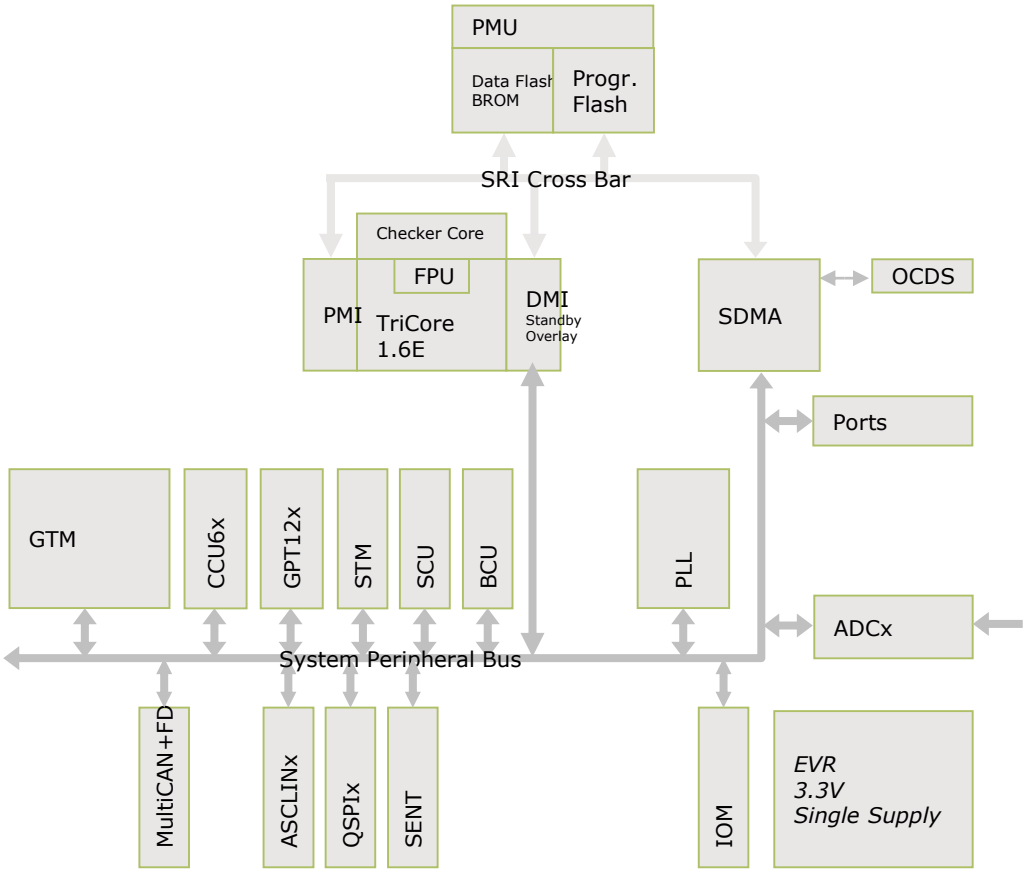
TQFP-144	TQFP-100	TQFP-80
0.4mm	**0.4mm**	**0.4mm**
-40°C to +125°C [1)]	-40°C to +125°C [1)]	-40°C to +125°C
24 ADC inputs	24 ADC inputs	14 ADC inputs

1x Series – Umbrella Device

SAK-TC21xL(S)-8F133

Feature Set		1x Series
TriCore 1.6P	# Cores / Checker	- / -
	Frequency	-
TriCore 1.6E	# Cores / Checker	1 / 1 (1 / 0)
	Frequency	133 MHz
Flash	Program Flash	512 KB
	Data Flash	64k, 125k cycles
SRAM	Total (DMI , PMI)	56 KB
DMA	Channels	16
ADC	Modules 12bit / DS	2 / -
	Channels 12bit / DS	24 / -
Timer	GTM Input / Output	8 / 32
	CCU / GPT modules	2 / 1
Interfaces	FlexRay (#/ch.)	-
	CAN (nodes/obj)	3 / 128
	QSPI / ASCLIN / I2C	4 / 2 / -
	SENT / PSI5	4 / -
	HSCT/ MSC / EBU	- / - / -
	Other	-
Safety	SIL Level	ASIL-D
Security	HSM	No
Power	EVR	Yes
	Standby Control Unit	WUT + SRAM

1) *Grade 0 option available on request with specific limitations for Ta=150°*



Package Variants

TQFP-144	TQFP-100	TQFP-80
0.4mm	**0.4mm**	**0.4mm**
-40°C to +125°C [1]	-40°C to +125°C [1]	-40°C to +125°C
24 ADC inputs	24 ADC inputs	14 ADC inputs

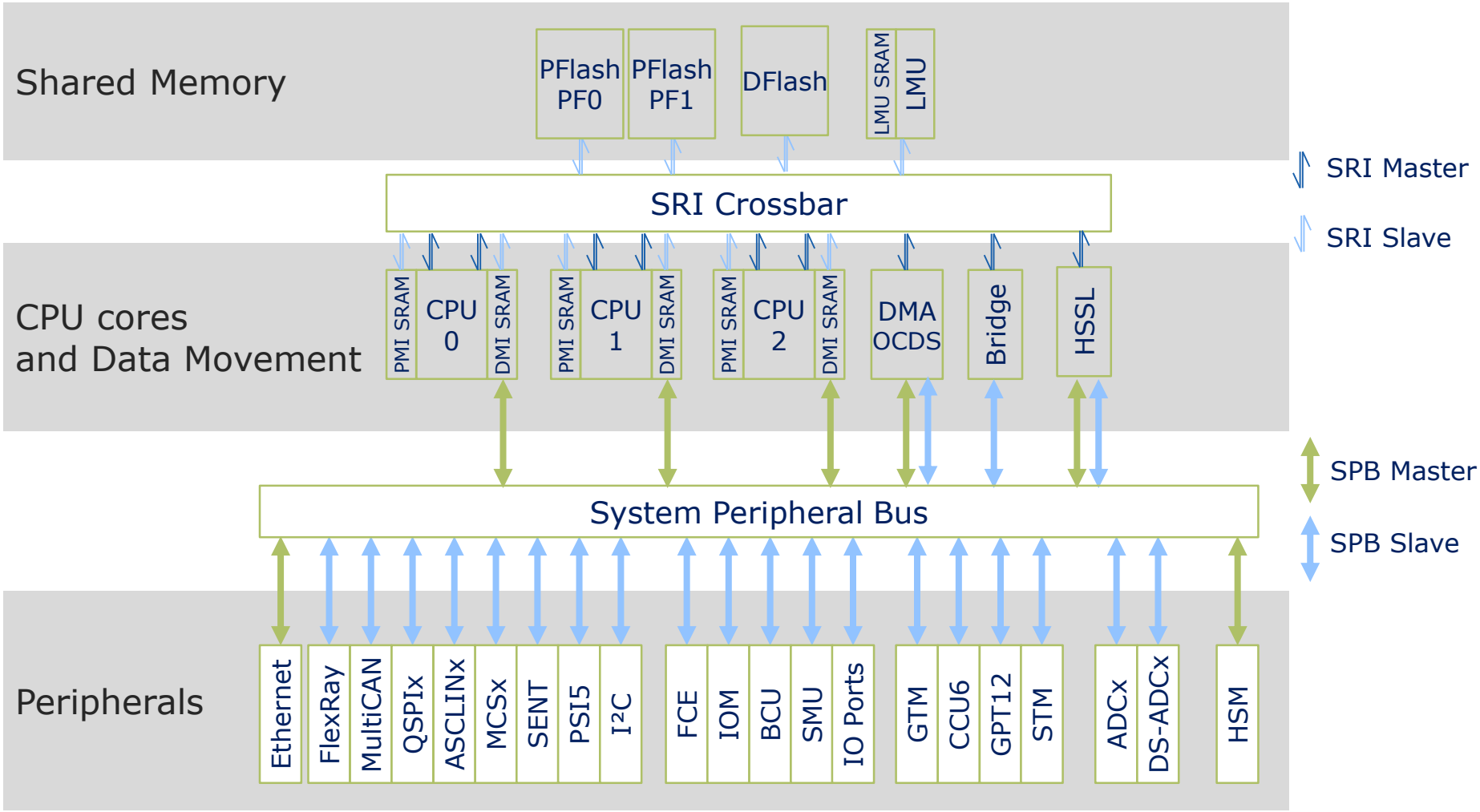
AURIX™ standard devices overview

Feature Set		9x Series	7x Series	6x Series	3x Series	2x Series	1x Series
TriCore 1.6P	# Cores / Checker	3 / 1	2 / 1	1 / 1	- / -	- / -	- / -
	Frequency	2x300 / 1x200 MHz	200 MHz	200 MHz	-	-	-
TriCore 1.6E	# Cores / Checker	- / -	1 / 1	1 / -	1 / 1	1 / 1 (1 / 0)	1 / 1 (1 / 0)
	Frequency	-	200 MHz	200 MHz	200 MHz	133 MHz	133 MHz
Flash	Program Flash	8 MB	4 MB	2.5 MB	2 MB	1 MB	512 KB
	EEProm @ w/e cycles	128 KB @ 500k	64 KB @ 500k	16 KB @ 500k	128k @ 125 k cycles	96k @ 125k cycles	64k @ 125k cycles
SRAM	Total (DMI , PMI, LMU)	728 KB	472 KB	240 KB	192 KB	96 KB	56 KB
DMA	Channels	128	64	48	16	16	16
ADC	Modules 12bit / DS	11 / 10	8 / 6	4 / 3	2 / -	2 / -	2 / -
	Channels 12bit / DS	84 / 10 diff	60 / 6 diff	50 / 3 diff	24 / -	24 / -	24 / -
Timer	GTM Input / Output	48 / 152 channels	32 / 88 channels	24 / 64 channels	8 / 32	8 / 32	8 / 32
	CCU / GPT modules	2 / 1	2 / 1	2 / 1	2 / 1	2 / 1	2 / 1
Interfaces	FlexRay (#/ch.)	2 / 4	1 / 2	1 / 2	1 / 2	-	-
	CAN FD[3] (nodes/obj)	6 / 384	4 / 256	5 / 256	6 / 256	3 / 128	3 / 128
	QSPI / ASCLIN / I2C	6 / 4 / 2	4 / 4 / 1	4 / 4 / 1	4 / 2 / -	4 / 2 / -	4 / 2 / -
	SENT / PSI5 / PSI5S	15 / 5 / 1	10 / 3 / 1	6 / 2 / 1	4 / -	4 / -	4 / -
	HSCT / MSC / EBU	1 / 3 diff LVDS / 1	1 / 2 diff LVDS / -	1 / 2 diff LVDS / -	- / - / -	- / - / -	- / - / -
	Other	Ethernet	Ethernet	Ethernet	-	-	-
Safety	SIL Level	ASIL-D	ASIL-D	ASIL-D	ASIL-D	ASIL-D	ASIL-D
Security	HSM	Yes	Optional	No	Optional	No	No
Power	EVR	Yes	Yes	Yes	Yes	Yes	Yes
	Standby Control Unit	Support	Support	Yes	WUT + SRAM	WUT + SRAM	WUT + SRAM

AURIX™ special devices overview

Feature Set Special Devices		9x Xtended	9x ADAS	6x ADAS	3x Xtended	3x ADAS
TriCore	# Cores / Checker	3 / 1	3 / 1	- / -	- / -	- / -
1.6P	Frequency	2x300 / 1x200 MHz	2x300 / 1x200 MHz	-	-	-
TriCore	# Cores / Checker	- / -	- / -	1 / -	1 / 1	1 / 1
1.6E	Frequency	-	-	200 MHz	200 MHz	200 MHz
Flash	Program Flash	8 MB	8 MB	2.5 MB	2 MB	2 MB
	EEPROM @ w/e cycles	128 KB @ 500k	128 KB @ 500k	16 KB @ 500k	128k , 125 k cycles	128k , 125 k cycles
SRAM	Total (DMI , PMI, LMU)	728 KB + **2MB**	728 KB + 2MB	240 KB + 512 KB	192 KB **+ 512KB**	192 KB + 512KB
DMA	Channels	128	128	48 + ADAS DMA	16	16
ADC	Modules 12bit / DS	11 / 10	11 / 10	4 / 3	4/ -	4 / -
	Channels 12bit / DS	84 / 10 diff	84 / 10 diff	40 / 3 diff	24 / -	24 / -
Timer	GTM Input / Output	48 / 152 channels	48 / 152 channels	24 / 64 channels	8 / 32	8 / 32
	CCU / GPT modules	2 / 1	2 / 1	2 / 1	2 / 1	2 / 1
Interfaces	FlexRay (#/ch.)	2 / 4	2 / 4	1 / 2	1 / 2	1 / 2
	CAN FD[3)] (nodes/obj)	6 / 384	6 / 384	5 / 256	6 / 256	6 / 256
	QSPI / ASCLIN / I2C	6 / 4 / 2	6 / 4 / 2	4 / 4 / 1	4 / 2 / -	4 / 2 / -
	SENT / PSI5 / PSI5S	15 / 5 / 1	15 / 5 / 1	6 / 2 / 1	4 / -	4 / -
	HSCT / MSC / EBU	1 / 3 diff LVDS / 1	1 / 3 diff LVDS / 1	1 / 2 diff LVDS / -	- / - / -	- / - / -
	Other	Ethernet	Ethernet, **CIF, FFT accelerator**	Ethernet, **CIF, FFT accelerator**	Ethernet	Ethernet, **FFT accelerator**
Safety	SIL Level	ASIL-D	ASIL-D	ASIL-D	ASIL-D	ASIL-D
Security	HSM	Yes	Optional	No	Option	Option
Power	EVR	Yes	Yes	Yes	Yes	Yes
	Standby Control Unit	Support	Support	Yes	WUT + SRAM	WUT + SRAM

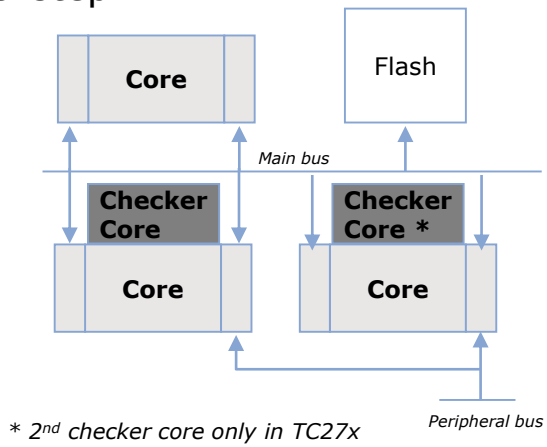
AURIX Bus Architecture



AURIX™ Core Architectures

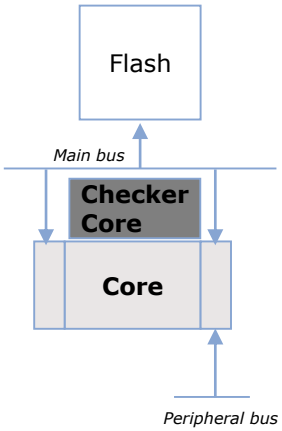
from single core to triple core lockstep w/ clock delay

Triple Core Lockstep - „**T**“ Marking

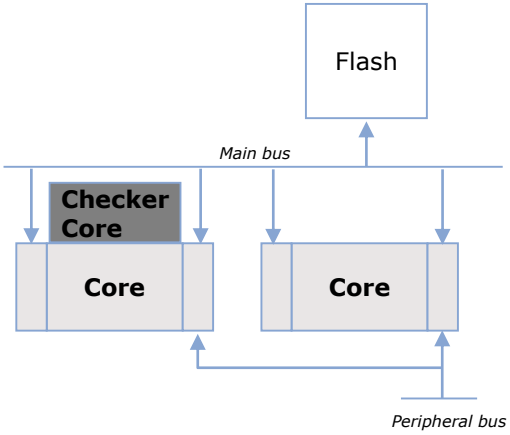


** 2nd checker core only in TC27x*

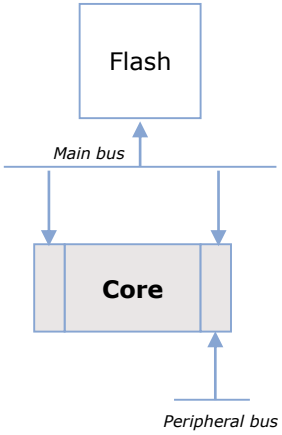
Lockstep - „**L**“ Marking



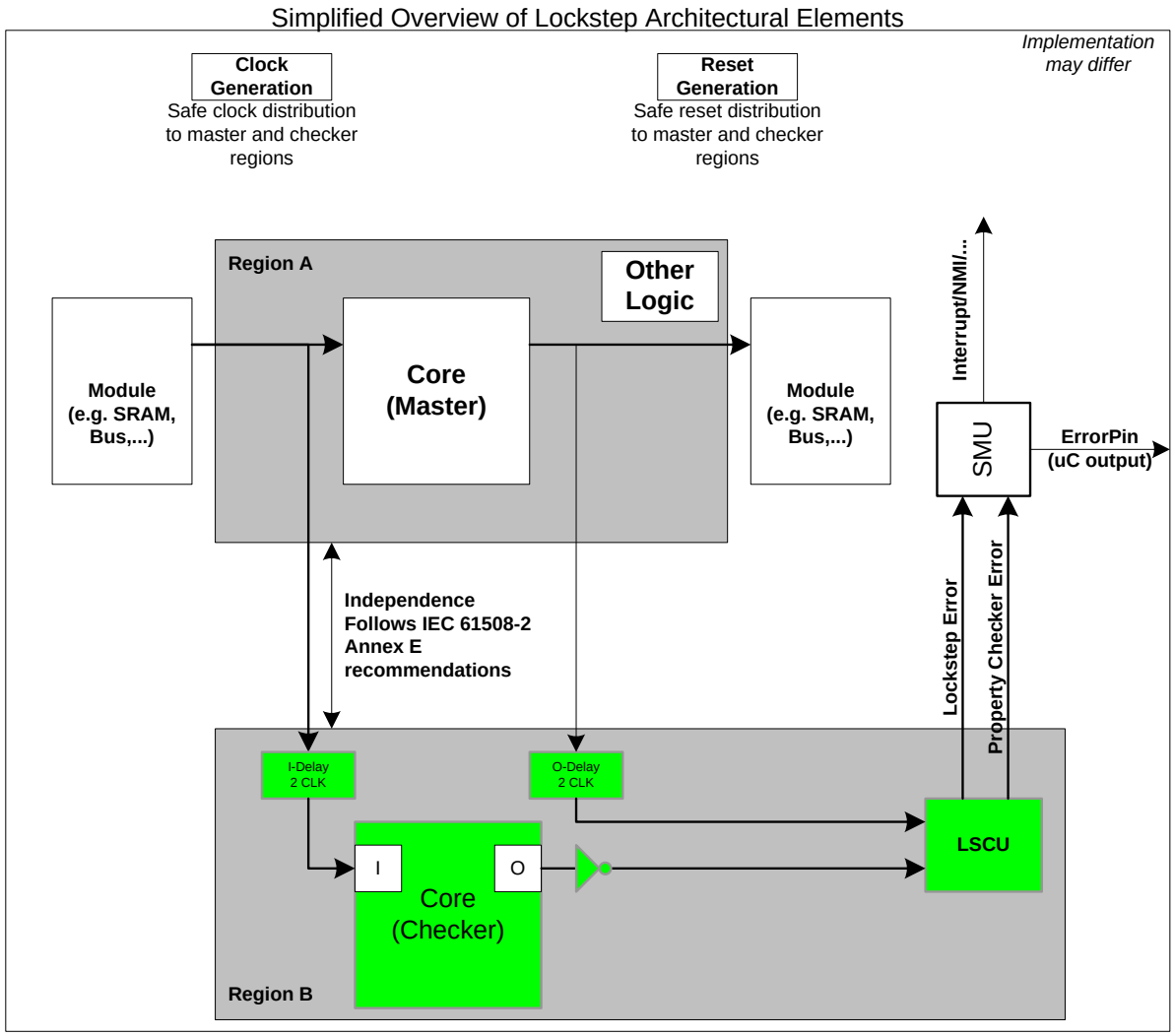
Dual Core Lockstep - „**D**“ Marking



Single Core - „**S**“ Marking



Diverse Lockstep CPU: Overview

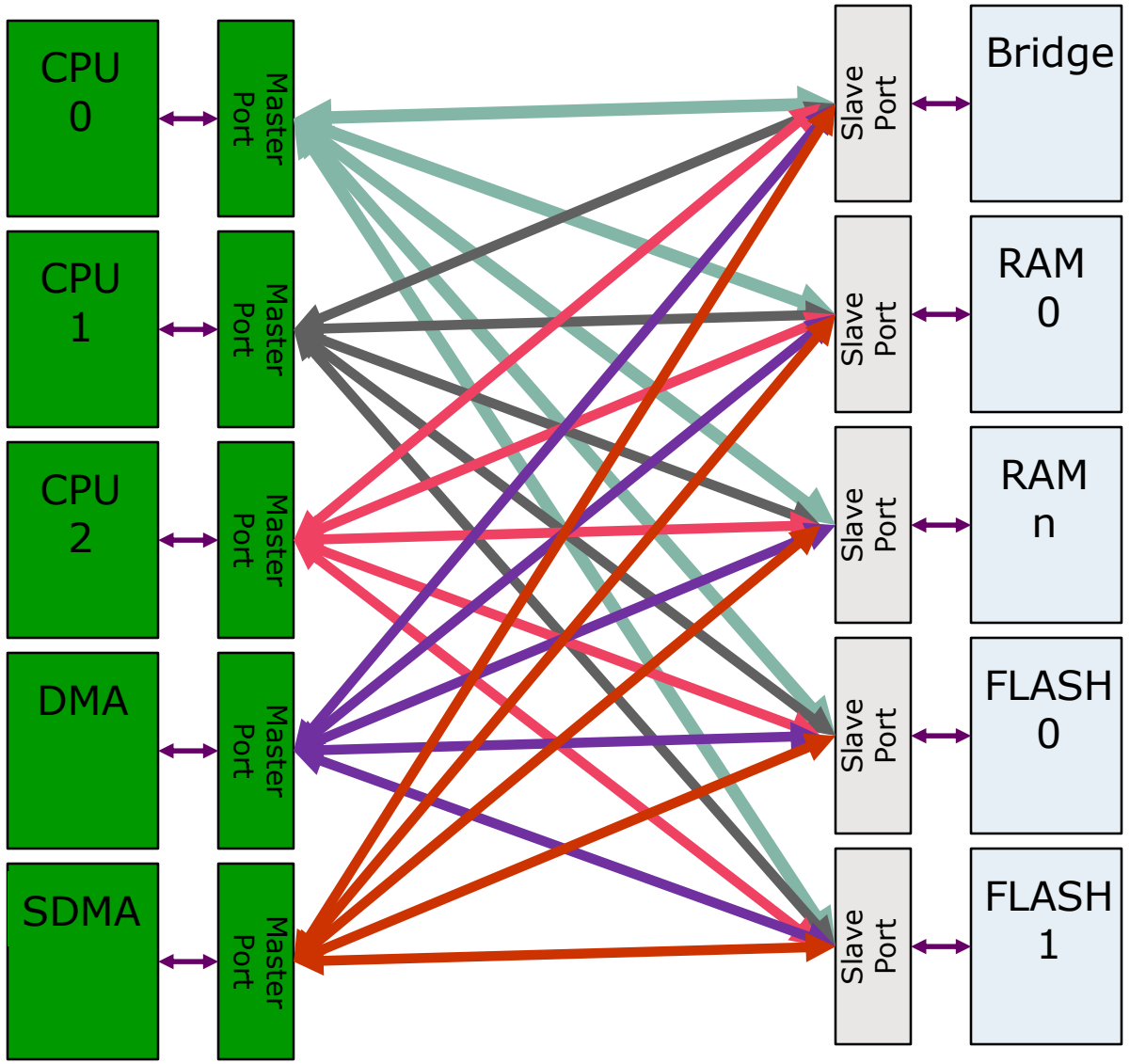


Infineon® Anti-Core the diverse lockstep concept

- Lockstep Architecture
  - Physical Isolation
  - Instruction-level execution Diversity
  - Circuit-level Design & Timing Diversity
  - Layout-level Diversity
  - Avoid symmetries
- Special design of clock & reset networks
- Careful design of lockstep comparator

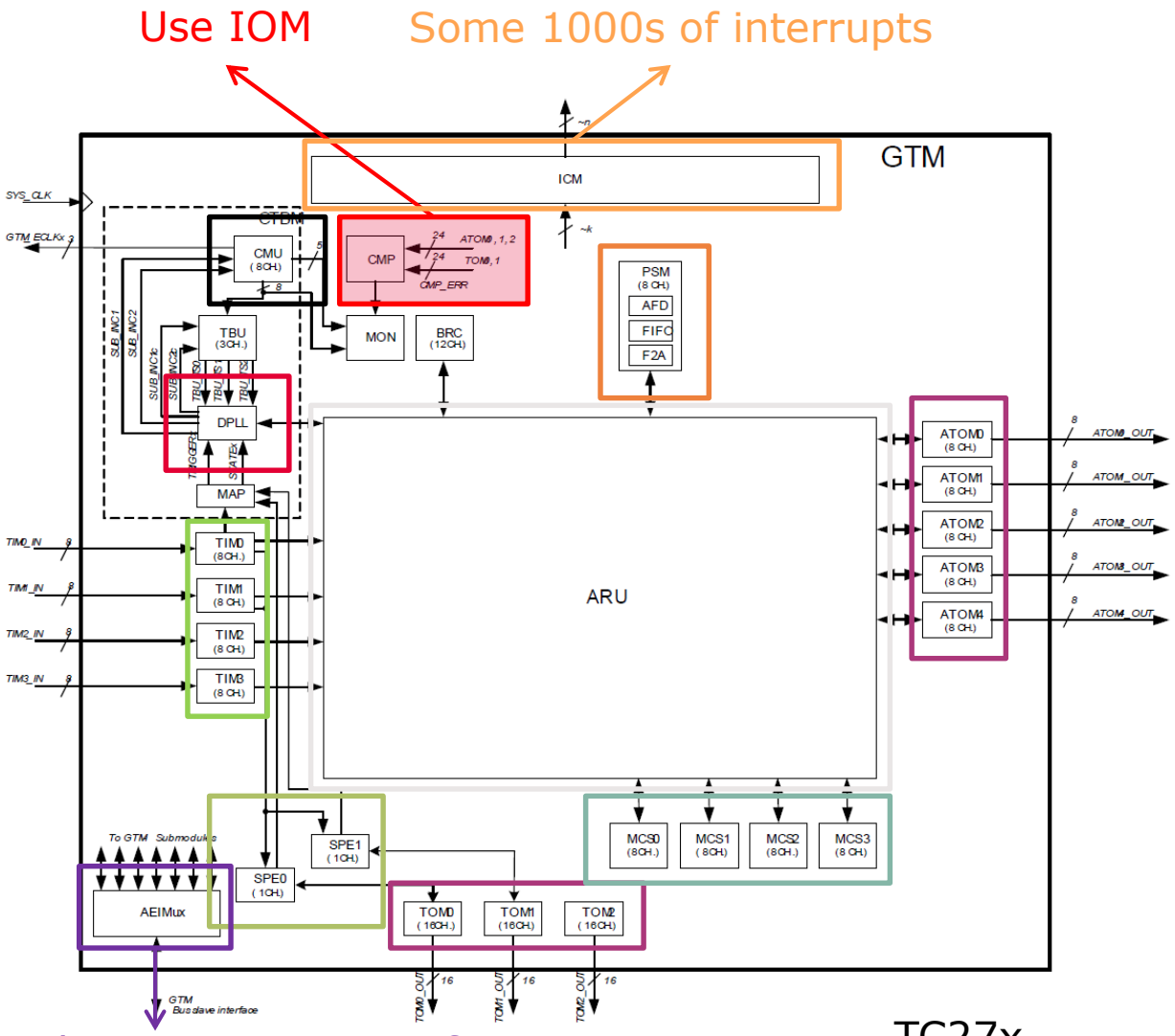
Multicore Bus Architecture
AURIX™ SRI Crossbar Realization

- One Master has direct access to several slave ports
- One slave serves one master at the same time
- Access Latency still can happen, if several masters using the same slave
- There is no access latency when different slaves are addressed
- Code and Data location has great influence on bus performance



GTM – Overview >=TC26x

- Timer-Output Modules
  - TOM
  - ATOM
- Timer-Input Modules
  - TIM
- State machines for BLDC-control over Hall-sensors
- Small data processing Modules MCS
- Own clock sources
- Engine management control unit (DPLL)
- PSM (FIFO)
- Advanced Routing Unit



AURIX™ - TC3xx

GTM Configurations

AURIX™ - TC3xx (GTM V3.1.2.0 – 2014.12.17)		**TC39x** 16MB	GTM V1.5.5.1	**TC38x** 10MB	GTM V1.5.5.1	**TC37x** 6MB	GTM V1.5.5.1	**TC36x** 4MB	GTM V2.02.1	**TC33x** 2MB
compare with AURIX (65nm) (GTM V1.5.5.1 and V2.02.1)			TC29x 8MB		TC27x 4MB		TC26x 2.5MB		TC23x 2MB	
Timer Inputs	**Total channels**	**64**	48	**56**	32	**40**	24	**24**	8	**16**
TIM	8 channels	**8**	6	**7**	4	**5**	3	3	1	2
Timer Outputs	**Total channels**	**192**	152	**152**	88	**88**	64	**64**	32	**32**
TOM	Standard 16-bit PWM ch.	**6**	5	5	3	3	2	2	2	2
ATOM	Complex 24-bit PWM ch.	**12**	9	9	5	**6**	4	4	0	0
DTM (with 4ch each)	Dead Time Module	**12** (TOM0-5) **12** (ATOM0-5)		**8** (TOM0-3) **12** (ATOM0-5)		**6** (TOM0-2) **10** (ATOM0-4)		**4** (TOM0-1) **8** (ATOM0-3)	**2** (TOM0-1)	**4** (TOM0-1)
SRAM	**Total**	**144.39**	56.75	**104.76**	35.13	**71.13**	26.13	**44.13**	0	0
MCS	Sequencer RAM 1536x32bit	**120**	36	**84**	24	**60**	18	**36**	0	0
PSM	FIFO, 1024x29bit	**3**x 3.63	2x 3.63	2x 3.63	3.63	3.63	3.63	3.63	0	0
DPLL	SRAM	13.5	13.5	13.5	7.5	7.5	4.5	4.5	0	0
Configuration										
Clock Generation	**DPLL**	1	1	1	1	1	1	1	0	0
	CMU	1	1	1	1	1	1	1	1	1
	TBU	3	3	3	3	3	3	3	1	1
Processing	**MCS**	**10**	6	**7**	4	**5**	3	3	0	0
amount 200MHz clusters	max MCS0-MCS4	**5**		**5**		**5**		**3**		
Pattern Evaluation	**SPE**	**6**	4	4	2	2	2	2	0	0
Broadcast Unit1	**BRC**	1	1	1	1	1	1	1	0	0
Safety	**MON**	1	1	1	1	1	1	1	1	1
	CMP	1	1	1	1	1	1	1	1	1

Why CAN FD?

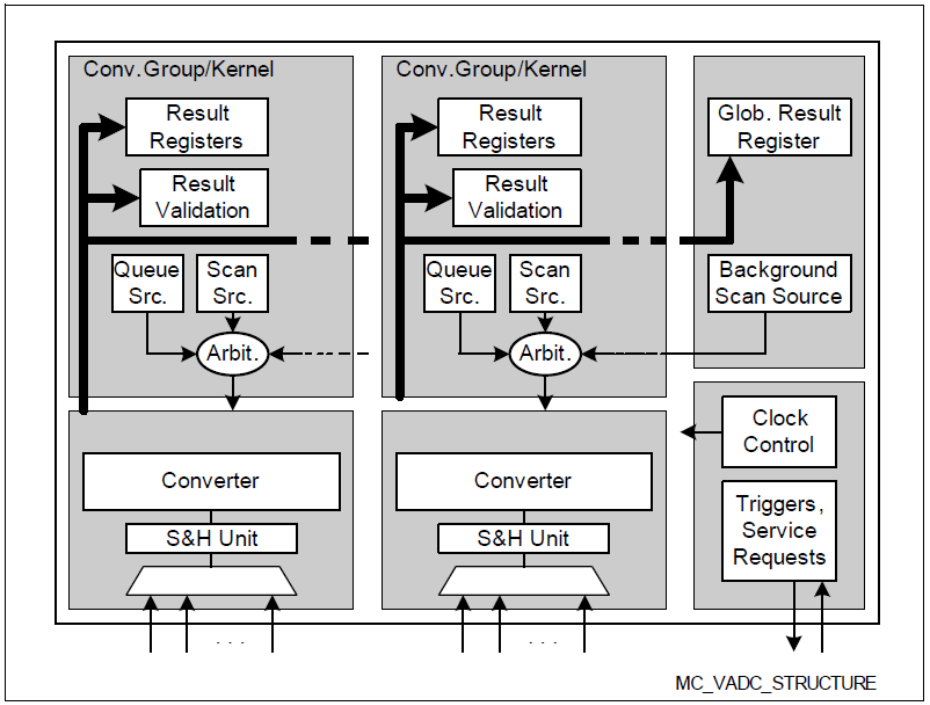
- Known as Classical CAN (CAN 2.0)
- Data payload upto 8 bytes
- One data speed
  - Max 1MBit/sec
- Included in all versions of AutoSAR
- In long term production

- CAN **F**lexible **D**ata
- Increased data payload upto 64 bytes
- Flexible data rate
  - 5MBit/sec point to point (AURIX PLUS)
  - 2MBit/sec network communication
- AutoSAR 4.0.3 is currently integrating CAN FD into specification
- First market implementation (AURIX) sampling today
- Includes Classical CAN

Major CAN FD advantages are ***Increased Payload*** and ***Increased Data rate***

AURIX VADC
General Overview

- ADC channels processed in groups
  - Input multiplexer selects one of n ADC inputs
  - Each group has independent request source arbitration, converter logic, and result handling
- Background request source can access all analog input channels not already assigned to a group request source
  - These conversions are executed with low priority
  - Background request source acts additional (virtual) background converter



HSM (Hardware Security Module)

within EVITA context and mapping on IFX products

EVITA[1] Classification within automotive Hardware Security Module	SHE[2] (HIS compliant)	Light EVITA HSM	Medium EVITA HSM	Full EVITA HSM
HSM secure internal RAM	key RAM only	optional	✓	✓
HSM private NVM (e.g. Key Storage, Secure Data)	key storage only	optional	✓	✓
symmetric HW Crypto Engine (e.g. 128-bit AES)	✓	✓	✓	✓
Asymmetric HW Crypto Engine (e.g. ECC256, RSA1024, RSA 2048)	—	—	—	✓
HW Hash Engine (e.g. SHA1, SHA2, RIPEMD, ...)	✓	—	✓	✓
RNG (Random Number Generator)	TRNG	PRNG (with ext. seed)	TRNG	TRNG
Secure CPU	State Machine (HIS compliant API)		✓	✓
Secure Application Use Cases	Immobilizing, Anti-Theft Secure Boot, Key Storage	Secure Sensors Secure Satellite ECU	Powertrain , Braking, Chassis ECUs (various)	Car2Car / Car2x Communication
IFX Implementations	**AUDO MAX - SHE** (TC1791/93/98)	not applicable for µC	**AURIX Performance HSM** (TC29x / TC27x) **AURIX Efficiency HSM** (TC23x)	**AURIX PLUS (TC3xx)**

(1) EU-funded project (2008-2011) on secure automotive onboard networks - www.evita-project.org

(2) Secure Hardware Extension - SHE, Standard by HIS ("Hersteller Initiative Software" by German OEMs)

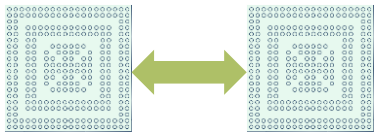
Agenda

1. TriCore in the CAV market
2. Aurix 1G Overview
3. Aurix 1G Derivatives
4. Aurix 2G Introduction
5. Aurix Safety Features
6. Aurix SW

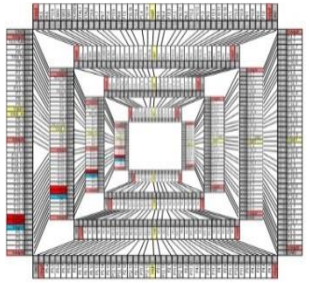
AURIX™ TC2xx to AURIX™ TC3xxx

Easy migration - Scalability & Compatibility

Fast conversion of existing AURIX™ TC2xx designs
- High AURIX TC3xx compatibility to pinout of existing QFP100/144/176 and BGA packages



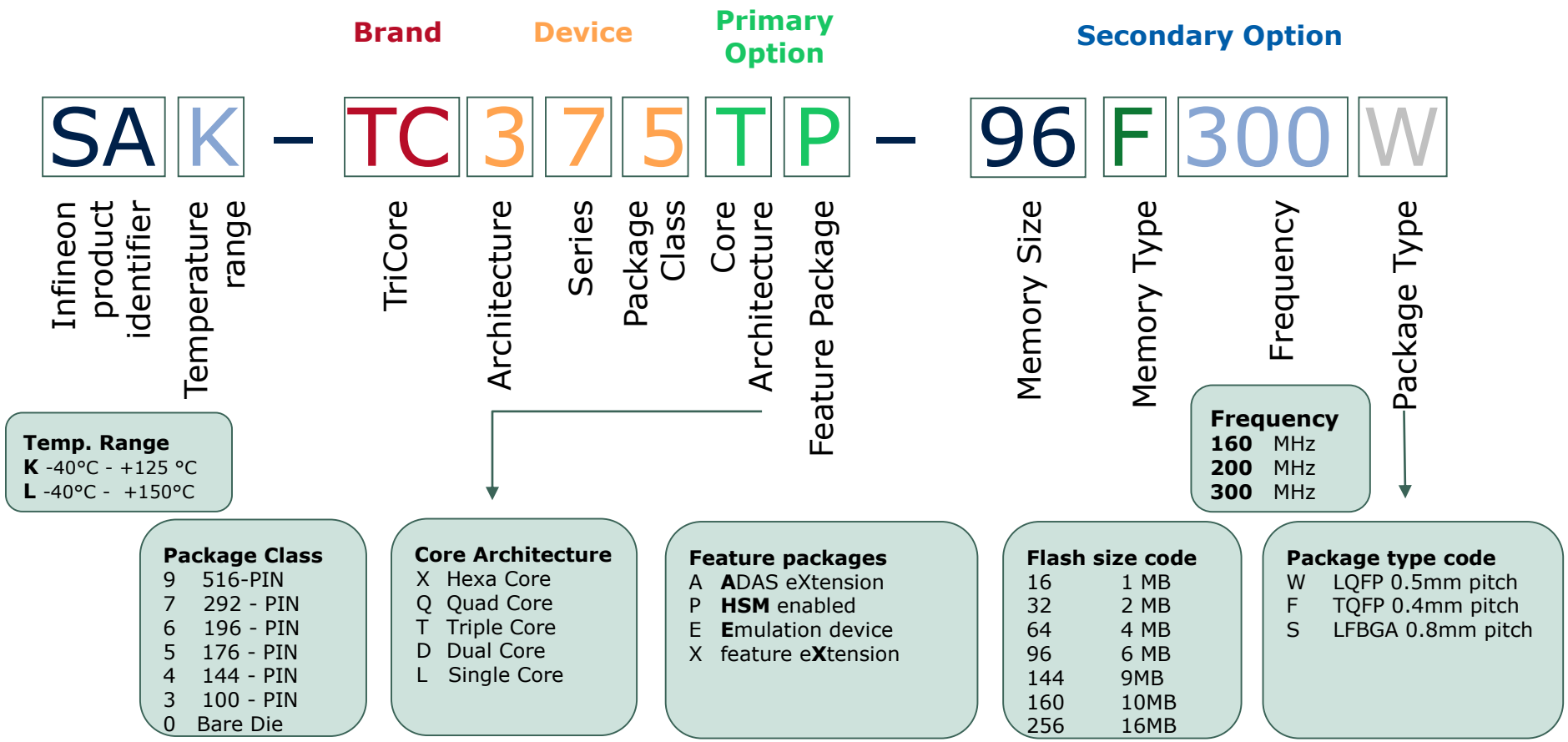
Flexibility - Scalability within the AURIX™ TC3xx family
- Up-/Downgrade paths for devices in identical packages
- Compatible pin-out of QFP/BGA package options enabling combi designs



Reuse – Software compatibility across the AURIX™ TC3xx family
- Binary compatible TC1.6.2 P cores
- Single set of peripherals across the AURIX™ TC3xx family

Common safety concept across the family
- Reuse of safety features from AURIX™ TC2xx
- Holistic safety concept across the AURIX™ TC3xx family

AURIX 2G Product Naming



AURIX™ TC3xx – scalable family

From low-cost to high-performance sensor fusion applications

9x Series up to 16 MB						TC397Xx TC397Qx 300MHz	TC399Xx 300MHz
8x Series up to 12 MB						TC387QX 300MHz	
8x Series up to 10MB						TC387Q 300MHz	TC389Q 300MHz
7xX Series up to 6MB						TC377TX 300 MHz	
7x Series up to 6MB					TC375T 300 MHz	TC377T 300 MHz	
6x Series up to 4MB			TC364D 300 MHz	TC366D 300 MHz	TC365D 300 MHz	TC367D 300 MHz	
5xA Series up to 4MB				TC356TA 300 MHz		TC357TA 300 MHz	
3xA Series up to 2 MB				TC336DA 200 MHz		TC337DA 200 MHz	
3x Series up to 2 MB	TC332L 200 MHz	TC333L 200 MHz	TC334L 200 MHz	TC336L 200 MHz		TC337L 200 MHz	
2x Series up to 1 MB	TC322L 160 MHz	TC323L 160 MHz	TC324L 160 MHz			TC327L 160 MHz	
Flash / Package	TQFP 80	TQFP 100	T/LQFP 144	BGA 180	LQFP 176	LFBGA 292	LFBGA 516

New device planned

- 12MB
- 16x CAN
- 1x eMMC
- +256KBRAM

2x GETH

ETHERNET

MCU Scalability

- Performance & Flash
- Pin-compatibility
- Binary compatible cores

Power Consumption

- On-chip SC DC/DC high-efficiency power supply

Safety/Security Concept

- ISO26262 compliance
- Hardware security support – eVita Full

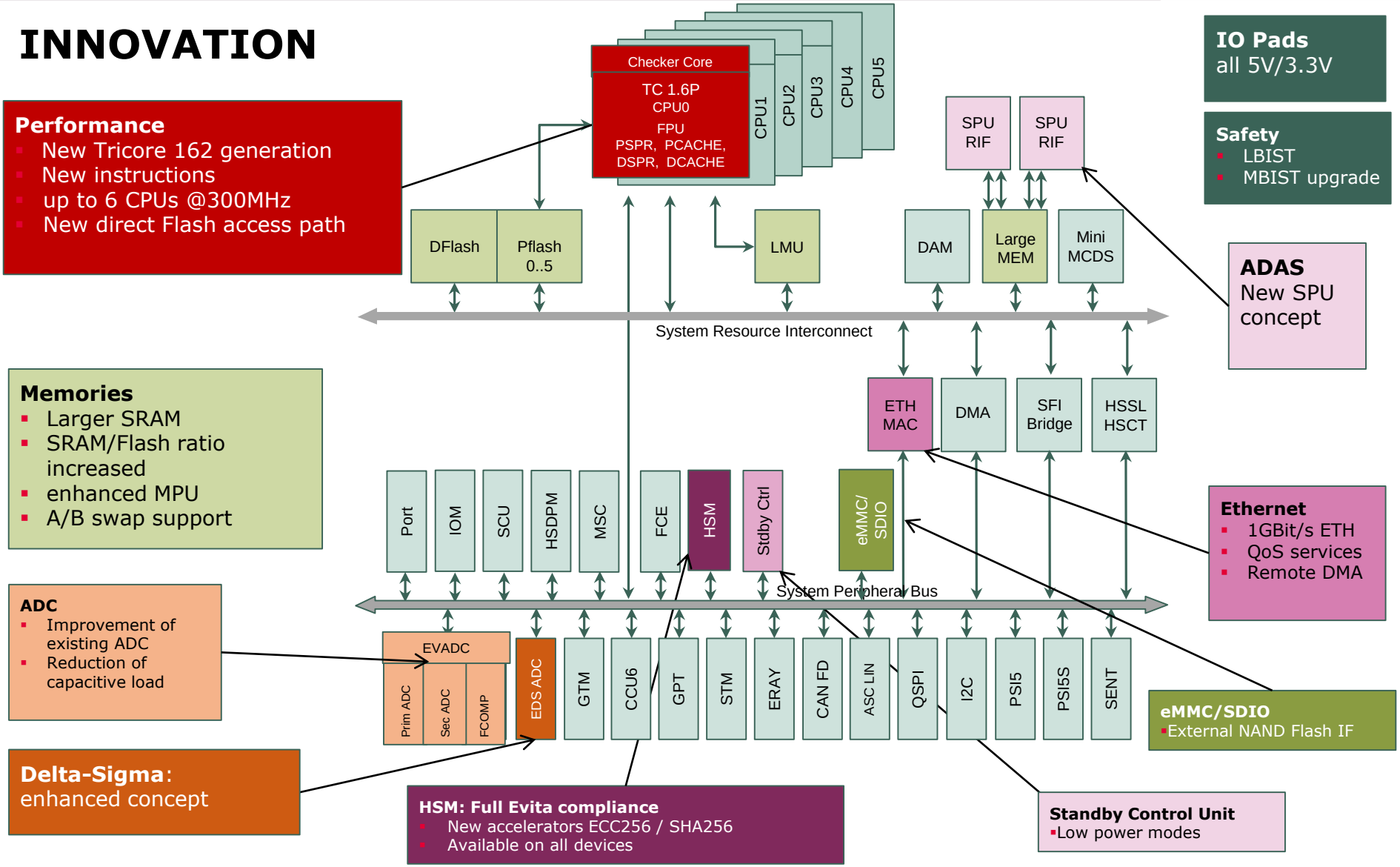
Connectivity

- Ethernet: up to 2x 1Gb
- CAN FD: up to 16 channels
- LIN: up to 24 channels
- eMMC IF
- HSSL: up to 2x

L - Single Lockstep Core
D - Dual Core
T - Triple Core
Q - Quadruple Core
X - Sextuple Core

AURIX™ TC3xx Architecture Evolution
(enhancements to AURIX TC2xx)

INNOVATION



Performance
- New Tricore 162 generation
- New instructions
- up to 6 CPUs @300MHz
- New direct Flash access path

Memories
- Larger SRAM
- SRAM/Flash ratio increased
- enhanced MPU
- A/B swap support

ADC
- Improvement of existing ADC
- Reduction of capacitive load

Delta-Sigma: enhanced concept

HSM: Full Evita compliance
- New accelerators ECC256 / SHA256
- Available on all devices

IO Pads
all 5V/3.3V

Safety
- LBIST
- MBIST upgrade

ADAS
New SPU concept

Ethernet
- 1GBit/s ETH
- QoS services
- Remote DMA

eMMC/SDIO
- External NAND Flash IF

Standby Control Unit
- Low power modes

AURIX TC3xx Feature Table

Feature Set		9x Series eXtension (16MB)	8x Series (10MB)	7x Series eXtended (3MB)	7x Series (6MB)	6x Series (4MB)	5x Series (4MB)	3x Series +eXtension (2MB)	3x Series (2MB)	2x Series (1MB)
TriCore 1.6	# Cores / Checker	6/4	4/2	3/3*	3/2	2/2	3/2	2/1	1/1	1/1
	Frequency	300MHz	300MHz	300MHz	300MHz	300MHz	300MHz	200MHz	200MHz	160MHZ
Accelerator	Signal processing Unit (SPU)	2xSPU					2xSPU	1xSPU		
Flash	Program Flash	16MB	10MB	9MB	6MB	4MB	4MB	2MB	2MB	1MB
	Data Flash (physical/logical)	1024kB	512kB	256kB	256kB	128kB	128kB	128kB	128kB	96kB
SRAM	Total (DMI , PMI, LMU, AMU)	6912KB	1568kB	4208kB	1136kB	672kB	2837kB	1328kB	248kB	152kB
DMA	Channels	128	128	128	128	64	64	16	16	16
ADC	Modules Primary / Sec / FC / DS	8/4/8/14	8/4/4/10	4/4/2/6	4/4/2/6	4/2/2/4	2/0/0/0	4/2/0/0	2/2/0/0	2/2/0/0
	Channels Primary / Sec / FC /DS	64/64/8/14	64/64/4/10	32/64/2/6	32/64/2/6	32/32/2/4	16/0/0/0	>16/32/0/0	16/32/0/0	16/32/0/0
Timer	GTM TIM / (A)TOM / MCS	64 / 192 / 10	56 / 152 / 7	40 / 88 / 5	40 / 88 / 5	24 / 64 / 3	-	16 / 32 / 0	16 / 32 / 0	16 / 32 / 0
	CCU / GPT modules / bit streaming	2/1/1	2/1/0	2/1/0	2/1/-	2/1/0	2/1/1	2/1/1	2/1/0	2/1/0
Interfaces	FlexRay (#/ch.)	2 /4	2/4	1/2	1/2	1/2	1/2	1/2	1/2	0/0
	CAN-FD / TT	12/1	12/1	12*/1	8/1	8/1	6/0	8/0	8/0	6/0
	QSPI / ASCLIN / I2C	6 /12/2	5 /24/2	5/12/1	5/12/1	4/12/1	4/4/0	4/12/0	4/12/0	4/6/0
	SENT / PSI5 / PSI5S	25/4/1	25/4/1	15/2/1	15/2/1	10/2/1	0/0/0	6/0/0	6/0/0	6/0/0
	HSSL / MSC / EBU	2/4/1	1/3/0	1/2/0	1/2/0	1/1/0	0/0/0	0/0/0	0/0/0	0/0/0
	Ethernet 100Mbps/1Gbps	1/1	1/1	1/1	1/1	1/1	1/1	1/1	-/-	-/-
	eMMC/SDIO	1/1		1/1				1/1		
	Radar /ext. ADC IF (RIF)	12x400Mbps LVDS	-	-	-	-	12x400Mbps LVDS	6x100Mbps LVDS	-	-
	Camera IF (CIF)	-	-	1	-	-	-	-	-	-
Security	HSM	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256	HSM+ECC256
Safety	SIL Level	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D	ASIL D
Power	EVR	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)	Yes (3.3V/5V)
	Standby Control Unit	yes	yes	yes	yes	yes	yes	yes	yes	yes

* In discussion

Agenda

1. TriCore in the CAV market
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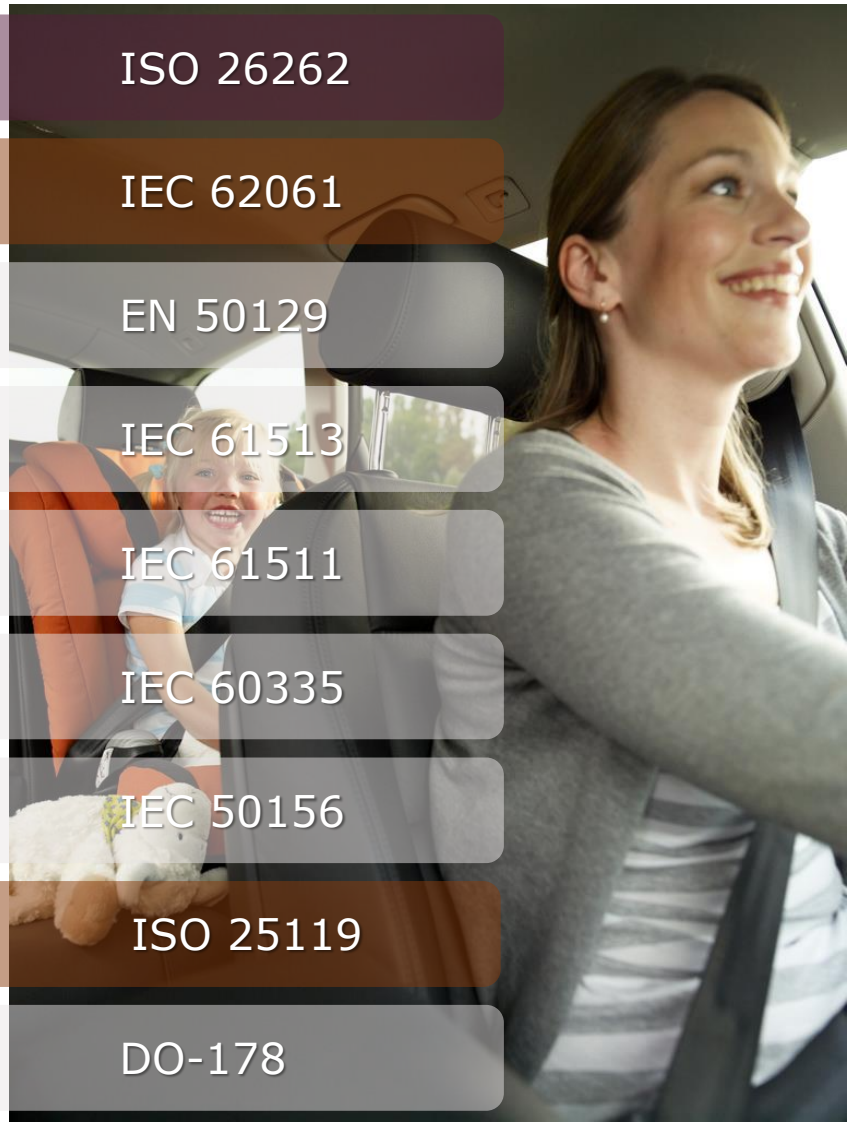
4. Aurix 2G Introduction
5. **Aurix Safety Features**
6. Aurix SW

Development of IEC61508:
relation to further safety standards

IEC 61508

Automotive	→	ISO 26262
Machinery	→	IEC 62061
Railway	→	EN 50129
Nuclear Power	→	IEC 61513
Process Industry	→	IEC 61511
Household Appliances	→	IEC 60335
Furnaces	→	IEC 50156
Agriculture	→	ISO 25119
Aviation	→	DO-178



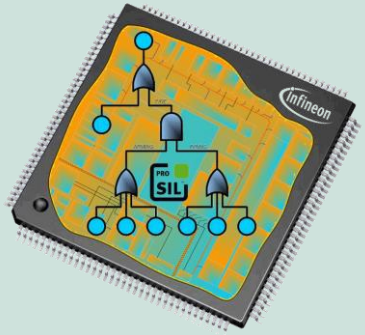
Development of IEC61508:
relation to further safety standards

Probability of Dangerouse Failure per Hour (PFHd) 10e-9	SIL IEC 61508	SIL EN 62061	PL EN ISO 13849	AgPL ISO 25119	ASIL ISO 26262
10e-8	4	-	-	-	-
10e-7	3	3	e	e	D
10e-6	2	2	d	d	C
					B
3x10e-6	1	1	c	c	A
10e-5			b	b	
1,00E-03	-	-	a	a	QM
	-	-	-	QM	

PL (Performance Level) SIL (Safety Integrity Level)

AURIX Safety: Cornerstones

Hardware designed for functional safety



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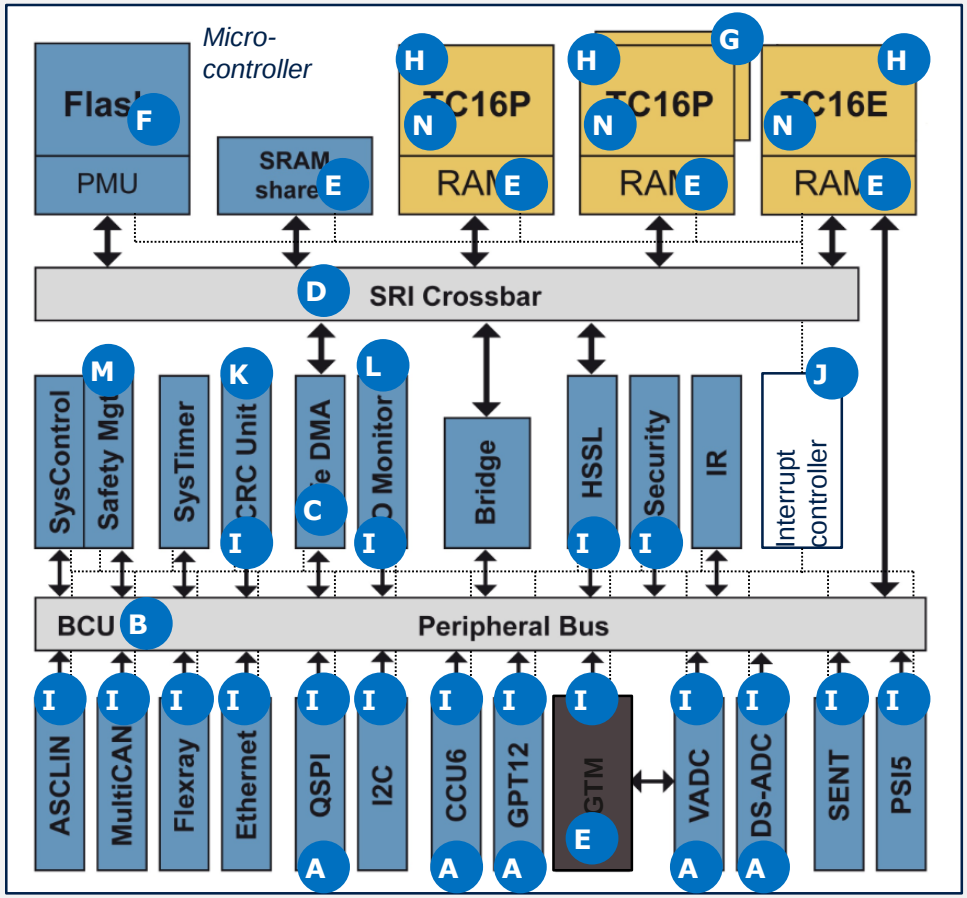
Safety Documentation

+

Software drivers for functional safety

ISO 26262 part of Infineon's standardized development process

AURIX –HW measures supporting safety



System

- **A** Redundant, spatially separated peripherals
- **B** Bus Monitoring Unit
- **C** Safe DMA
- **D** Safe SRI
- **E** FLASH ECC (DECTED with enhancements to detect multi bit failures)
- **F** SRAM ECC (SECDED with enhancements to detect multi bit failures)
- **G** Lockstep core
- **H** Memory protection core
- **I** Memory protection peripherals
- **J** Safe Interrupt Processing
- **K** Flexible CRC Engine (FCE)
- **L** IO Monitor
- **M** Clock Monitoring
- **N** CPU self tests (90% Latent Fault Metric)

IEC 61508 documentation

AURIX™ for CAV and industrial safety applications

Safety documents:

- FMEDA based on IEC61508
- Safety manual which contains IEC61508 data

Available now

Safety Case:

- Infineon will not provide the IEC61508 safety case, safety case will be based only on ISO26262
- Safety case has to be done at the system level by the customer

Safety Support:

- Will be handled by PDH and can be booked from customer directly at a PDH partner

Infineon Partners are published on:
www.infineon.com/pdh

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Infineon AURIX Software offering

Reduction of customer SW development

Commercial Basic Software

- **AUTOSAR MCAL**:
  - MC-ISAR Basic (Base, MEM, COM Basic)
  - MC-ISAR COM Enhanced
  - MCAL Complex Driver MCD and Demo code
- **Safety driver:** support of external watch dogs in discussion

Free tool/ example code

- iLLD: Infineon low level driver
- ACT : AURIX configuration tool
- FreeOSEK
- Free compiler
- Free debugger
- DSP library

Commercial Value Software

- SHE+ security driver:
  - Supporting latest security requirements

Auxiliary Tools and Software

- C Model
- Simulink model (RADAR only)

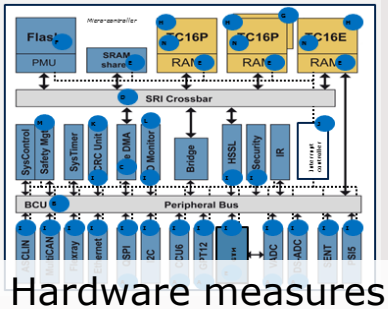
Software Design Services

- Customer specific driver
- On customer request

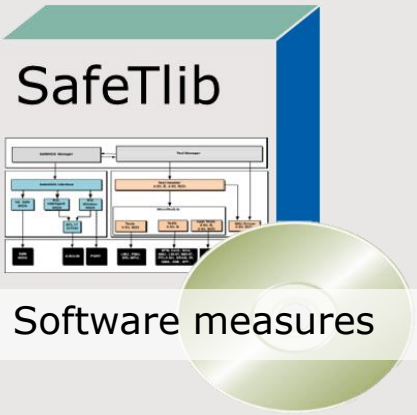
AURIX TC2xx to TC3xx

Improved safety deployment reduces SW DI effort

AURIX TC2xx



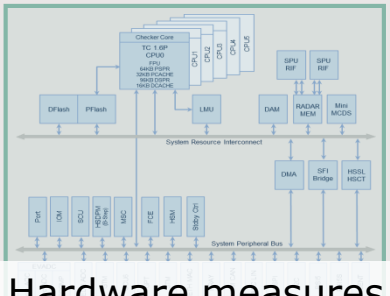
Hardware measures



Software measures

- ISO26262 compliant HW measurements
- Software implementation with SafeTLib

AURIX TC3xx



Hardware measures

Software measures

- Software measures integrated into hardware LBIST
- Software based self test(SBST) for non lockstep core

Part of your life. Part of tomorrow.

Infineon