21.4 I2C Registers

NOTE: All bits defined as reserved must be written by software with 0s, for preserving future compatibility. When read, any reserved bit returns 0. Also, note that it is good software practice to use complete mask patterns for setting or testing individually bit fields within a register.

21.4.1 I2C Registers

Table 21-8 lists the memory-mapped registers for the I2C. All register offset addresses not listed in Table 21-8 should be considered as reserved locations and the register contents should not be modified.

Table 21-8. I2C REGISTERS

Offset	Acronym	Register Name	Section
00h	I2C_REVNB_LO		Section 21.4.1.1
04h	I2C_REVNB_HI		Section 21.4.1.2
10h	I2C_SYSC		Section 21.4.1.3
24h	I2C_IRQSTATUS_RAW		Section 21.4.1.4
28h	I2C_IRQSTATUS		Section 21.4.1.5
2Ch	I2C_IRQENABLE_SET		Section 21.4.1.6
30h	I2C_IRQENABLE_CLR		Section 21.4.1.7
34h	I2C_WE		Section 21.4.1.8
38h	I2C_DMARXENABLE_SET		Section 21.4.1.9
3Ch	I2C_DMATXENABLE_SET		Section 21.4.1.10
40h	I2C_DMARXENABLE_CLR		Section 21.4.1.11
44h	I2C_DMATXENABLE_CLR		Section 21.4.1.12
48h	I2C_DMARXWAKE_EN		Section 21.4.1.13
4Ch	I2C_DMATXWAKE_EN		Section 21.4.1.14
90h	I2C_SYSS		Section 21.4.1.15
94h	I2C_BUF		Section 21.4.1.16
98h	I2C_CNT		Section 21.4.1.17
9Ch	I2C_DATA		Section 21.4.1.18
A4h	I2C_CON		Section 21.4.1.19
A8h	I2C_OA		Section 21.4.1.20
ACh	I2C_SA		Section 21.4.1.21
B0h	I2C_PSC		Section 21.4.1.22
B4h	I2C_SCLL		Section 21.4.1.23
B8h	I2C_SCLH		Section 21.4.1.24
BCh	I2C_SYSTEST		Section 21.4.1.25
C0h	I2C_BUFSTAT		Section 21.4.1.26
C4h	I2C_OA1		Section 21.4.1.27
C8h	I2C_OA2		Section 21.4.1.28
CCh	I2C_OA3		Section 21.4.1.29
D0h	I2C_ACTOA		Section 21.4.1.30
D4h	I2C_SBLOCK		Section 21.4.1.31

21.4.1.5 I2C_IRQSTATUS Register (offset = 28h) [reset = 0h]

I2C_IRQSTATUS is shown in Figure 21-20 and described in Table 21-13.

This register provides core status information for interrupt handling, showing all active and enabled events and masking the others. The fields are read-write. Writing a 1 to a bit will clear it to 0, that is, clear the IRQ. Writing a 0 will have no effect, that is, the register value will not be modified. Only enabled, active events will trigger an actual interrupt request on the IRQ output line. For all the internal fields of the I2C_IRQSTATUS register, the descriptions given in the I2C_IRQSTATUS_RAW subsection are valid.

Figure 21-20. I2C_IRQSTATUS Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 21-13. I2C_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	Reserved	R	0h	
14	XDR	R/W	0h	Transmit draining IRQ enabled status. 0x0 = Transmit draining inactive 0x1 = Transmit draining enabled
13	RDR	R/W	0h	Receive draining IRQ enabled status. 0x0 = Receive draining inactive 0x1 = Receive draining enabled
12	BB	R/W	0h	Bus busy enabled status. Writing into this bit has no effect. 0x0 = Bus is free 0x1 = Bus is occupied
11	ROVR	R/W	0h	Receive overrun enabled status. Writing into this bit has no effect. 0x0 = Normal operation 0x1 = Receiver overrun
10	XUDF	R/W	0h	Transmit underflow enabled status. Writing into this bit has no effect. 0x0 = Normal operation 0x1 = Transmit underflow
9	AAS	R/W	0h	Address recognized as slave IRQ enabled status. 0x0 = No action 0x1 = Address recognized
8	BF	R/W	0h	Bus Free IRQ enabled status. 0x0 = No action 0x1 = Bus free

21.4.1.6 I2C_IRQENABLE_SET Register (offset = 2Ch) [reset = 0h]

I2C_IRQENABLE_SET is shown in Figure 21-21 and described in Table 21-14.

All 1-bit fields enable a specific interrupt event to trigger an interrupt request. Writing a 1 to a bit will enable the field. Writing a 0 will have no effect, that is, the register value will not be modified. For all the internal fields of the I2C_IRQENABLE_SET register, the descriptions given in the I2C_IRQSTATUS_RAW subsection are valid.

Figure 21-21. I2C_IRQENABLE_SET Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved	XDR_IE	RDR_IE	Reserved	ROVR	XUDF	AAS_IE	BF_IE
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-14. I2C_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	Reserved	R	0h	
14	XDR_IE	R/W	0h	Transmit draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0x0 = Transmit draining interrupt disabled 0x1 = Transmit draining interrupt enabled
13	RDR_IE	R/W	0h	Receive draining interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. 0x0 = Receive draining interrupt disabled 0x1 = Receive draining interrupt enabled
12	Reserved	R	0h	
11	ROVR	R/W	0h	Receive overrun enable set. 0x0 = Receive overrun interrupt disabled 0x1 = Receive draining interrupt enabled
10	XUDF	R/W	0h	Transmit underflow enable set. 0x0 = Transmit underflow interrupt disabled 0x1 = Transmit underflow interrupt enabled
9	AAS_IE	R/W	0h	Addressed as slave interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0x0 = Addressed as slave interrupt disabled 0x1 = Addressed as slave interrupt enabled
8	BF_IE	R/W	0h	Bus free interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0x0 = Bus free interrupt disabled 0x1 = Bus free interrupt enabled
7	AERR_IE	R/W	0h	Access error interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0x0 = Access error interrupt disabled 0x1 = Access error interrupt enabled

Table 21-14. I2C_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	STC_IE	R/W	0h	Start condition interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0x0 = Start condition interrupt disabled 0x1 = Start condition interrupt enabled
5	GC_IE	R/W	0h	General call interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]. 0x0 = General call interrupt disabled 0x1 = General call interrupt enabled
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]. 0x0 = Transmit data ready interrupt disabled 0x1 = Transmit data ready interrupt enabled
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]. 0x0 = Receive data ready interrupt disabled 0x1 = Receive data ready interrupt enabled
2	ARDY_IE	R/W	0h	Register access ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]. 0x0 = Register access ready interrupt disabled 0x1 = Register access ready interrupt enabled
1	NACK_IE	R/W	0h	No acknowledgment interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]. 0x0 = Not Acknowledge interrupt disabled 0x1 = Not Acknowledge interrupt enabled
0	AL_IE	R/W	0h	Arbitration lost interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]. 0x0 = Arbitration lost interrupt disabled 0x1 = Arbitration lost interrupt enabled

21.4.1.7 I2C_IRQENABLE_CLR Register (offset = 30h) [reset = 0h]

I2C_IRQENABLE_CLR is shown in Figure 21-22 and described in Table 21-15.

All 1-bit fields clear a specific interrupt event. Writing a 1 to a bit will disable the interrupt field. Writing a 0 will have no effect, that is, the register value will not be modified. For all the internal fields of the I2C_IRQENABLE_CLR register, the descriptions given in the I2C_IRQSTATUS_RAW subsection are valid.

Figure 21-22. I2C_IRQENABLE_CLR Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved	XDR_IE	RDR_IE	Reserved	ROVR	XUDF	AAS_IE	BF_IE
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-15. I2C_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	Reserved	R	0h	
14	XDR_IE	R/W	0h	Transmit draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]. 0x0 = Transmit draining interrupt disabled 0x1 = Transmit draining interrupt enabled
13	RDR_IE	R/W	0h	Receive draining interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]. 0x0 = Receive draining interrupt disabled 0x1 = Receive draining interrupt enabled
12	Reserved	R	0h	
11	ROVR	R/W	0h	Receive overrun enable clear. 0x0 = Receive overrun interrupt disabled 0x1 = Receive draining interrupt enabled
10	XUDF	R/W	0h	Transmit underflow enable clear. 0x0 = Transmit underflow interrupt disabled 0x1 = Transmit underflow interrupt enabled
9	AAS_IE	R/W	0h	Addressed as slave interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]. 0x0 = Addressed as slave interrupt disabled 0x1 = Addressed as slave interrupt enabled
8	BF_IE	R/W	0h	Bus Free interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]. 0x0 = Bus free interrupt disabled 0x1 = Bus free interrupt enabled
7	AERR_IE	R/W	0h	Access error interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]. 0x0 = Access error interrupt disabled 0x1 = Access error interrupt enabled

Table 21-15. I2C_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	STC_IE	R/W	0h	Start condition interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]. 0x0 = Start condition interrupt disabled 0x1 = Start condition interrupt enabled
5	GC_IE	R/W	0h	General call interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]. 0x0 = General call interrupt disabled 0x1 = General call interrupt enabled
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]. 0x0 = Transmit data ready interrupt disabled 0x1 = Transmit data ready interrupt enabled
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable set. Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY] 0x0 = Receive data ready interrupt disabled 0x1 = Receive data ready interrupt enabled
2	ARDY_IE	R/W	0h	Register access ready interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]. 0x0 = Register access ready interrupt disabled 0x1 = Register access ready interrupt enabled
1	NACK_IE	R/W	0h	No acknowledgment interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]. 0x0 = Not Acknowledge interrupt disabled 0x1 = Not Acknowledge interrupt enabled
0	AL_IE	R/W	0h	Arbitration lost interrupt enable clear. Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]. 0x0 = Arbitration lost interrupt disabled 0x1 = Arbitration lost interrupt enabled

21.4.1.17 I2C_CNT Register (offset = 98h) [reset = 0h]

I2C_CNT is shown in Figure 21-32 and described in Table 21-25.

CAUTION: During an active transfer phase (between STT having been set to 1 and reception of ARDY), no modification must be done in this register. Changing it may result in an unpredictable behavior. This read/write register is used to control the numbers of bytes in the I2C data payload.

Figure 21-32. I2C_CNT Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
DCOUNT							
R/W-0h							

7	6	5	4	3	2	1	0
DCOUNT							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-25. I2C_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15-0	DCOUNT	R/W	0h	Data count. I2C Master Mode only (receive or transmit F/S). This 16-bit countdown counter decrements by 1 for every byte received or sent through the I2C interface. A write initializes DCOUNT to a saved initial value. A read returns the number of bytes that are yet to be received or sent. A read into DCOUNT returns the initial value only before a start condition and after a stop condition. When DCOUNT reaches 0, the core generates a stop condition if a stop condition was specified (I2C_CON.STP = 1) and the ARDY status flag is set to 1 in the I2C_IRQSTATUS_RAW register. Note that DCOUNT must not be reconfigured after I2C_CON.STT was enabled and before ARDY is received. Note 1: In case of I2C mode of operation, if I2C_CON.STP = 0, then the I2C asserts SCL = 0 when DCOUNT reaches 0. The CPU can then reprogram DCOUNT to a new value and resume sending or receiving data with a new start condition (restart). This process repeats until the CPU sets to 1 the I2C_CON.STP bit. The ARDY flag is set each time DCOUNT reaches 0 and DCOUNT is reloaded to its initial value. Values after reset are low (all 16 bits). Note 2: Since for DCOUNT = 0, the transfer length is 65536, the module does not allow the possibility to initiate zero data bytes transfers. 0x0 = Data counter = 65536 bytes (216) 0x1 = Data counter = 1 bytes 0xFFFF = Data counter = 65535 bytes (216 - 1)

21.4.1.18 I2C_DATA Register (offset = 9Ch) [reset = 0h]

I2C_DATA is shown in Figure 21-33 and described in Table 21-26.

This register is the entry point for the local host to read data from or write data to the FIFO buffer.

Figure 21-33. I2C_DATA Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 21-26. I2C_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	Reserved	R	0h	
7-0	DATA	R/W	0h	Transmit/Receive data FIFO endpoint. When read, this register contains the received I2C data. When written, this register contains the byte value to transmit over the I2C data. In SYSTEST loop back mode (I2C_SYSTEST: TMODE = 11), this register is also the entry/receive point for the data. Values after reset are unknown (all 8-bits). Note: A read access, when the buffer is empty, returns the previous read data value. A write access, when the buffer is full, is ignored. In both events, the FIFO pointers are not updated and an Access Error (AERR) Interrupt is generated.

21.4.1.19 I2C_CON Register (offset = A4h) [reset = 0h]

I2C_CON is shown in Figure 21-34 and described in Table 21-27.

During an active transfer phase (between STT having been set to 1 and reception of ARDY), no modification must be done in this register (except STP enable). Changing it may result in an unpredictable behavior.

Figure 21-34. I2C_CON Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
I2C_EN	Reserved	OPMODE		STB	MST	TRX	XSA
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

7	6	5	4	3	2	1	0
XOA0	XOA1	XOA2	XOA3	Reserved		STP	STT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 21-27. I2C_CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0h	
15	I2C_EN	R/W	0h	I2C module enable. When this bit is cleared to 0, the I2C controller is not enabled and reset. When 0, receive and transmit FIFOs are cleared and all status bits are set to their default values. All configuration registers (I2C_IRQENABLE_SET, I2C_IRQWAKE_SET, I2C_BUF, I2C_CNT, I2C_CON, I2C_OA, I2C_SA, I2C_PSC, I2C_SCLL and I2C_SCLH) are not reset, they keep their initial values and can be accessed. The CPU must set this bit to 1 for normal operation. Value after reset is low. 0x0 = Controller in reset. FIFO are cleared and status bits are set to their default value. 0x1 = Module enabled
14	Reserved	R	0h	
13-12	OPMODE	R/W	0h	Operation mode selection. These two bits select module operation mode. Value after reset is 00. 0x0 = I2C Fast/Standard mode 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved
11	STB	R/W	0h	Start byte mode (I2C master mode only). The start byte mode bit is set to 1 by the CPU to configure the I2C in start byte mode (I2C_SA = 0000 0001). See the Philips I2C spec for more details [1]. Value after reset is low. 0x0 = Normal mode 0x1 = Start byte mode

Table 21-27. I2C_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MST	R/W	0h	Master/slave mode (I2C mode only). When this bit is cleared, the I2C controller is in the slave mode and the serial clock (SCL) is received from the master device. When this bit is set, the I2C controller is in the master mode and generates the serial clock. Note: This bit is automatically cleared at the end of the transfer on a detected stop condition, in case of arbitration lost or when the module is configured as a master but addressed as a slave by an external master. Value after reset is low. 0x0 = Slave mode 0x1 = Master mode
9	TRX	R/W	0h	Transmitter/receiver mode (i2C master mode only). When this bit is cleared, the I2C controller is in the receiver mode and data on data line SDA is shifted into the receiver FIFO and can be read from I2C_DATA register. When this bit is set, the I2C controller is in the transmitter mode and the data written in the transmitter FIFO via I2C_DATA is shifted out on data line SDA. Value after reset is low. The operating modes are defined as follows: MST = 0, TRX = x, Operating Mode = Slave receiver. MST = 0, TRX = x, Operating Mode = Slave transmitter. MST = 1, TRX = 0, Operating Modes = Master receiver. MST = 1, TRX = 0, Operating Modes = Master transmitter. 0x0 = Receiver mode 0x1 = Transmitter mode
8	XSA	R/W	0h	Expand slave address. (I2C mode only). When set, this bit expands the slave address to 10-bit. Value after reset is low. 0x0 = 7-bit address mode 0x1 = 10-bit address mode
7	XOA0	R/W	0h	Expand own address 0. (I2C mode only). When set, this bit expands the base own address (OA0) to 10-bit. Value after reset is low. 0x0 = 7-bit address mode 0x1 = 10-bit address mode
6	XOA1	R/W	0h	Expand own address 1. (I2C mode only). When set, this bit expands the first alternative own address (OA1) to 10-bit. Value after reset is low. 0x0 = 7-bit address mode 0x1 = 10-bit address mode
5	XOA2	R/W	0h	Expand own address 2. (I2C mode only). When set, this bit expands the second alternative own address (OA2) to 10-bit. Value after reset is low. 0x0 = 7-bit address mode. (I2C mode only). 0x1 = 10-bit address mode
4	XOA3	R/W	0h	Expand own address 3. When set, this bit expands the third alternative own address (OA3) to 10-bit. Value after reset is low. 0x0 = 7-bit address mode 0x1 = 10-bit address mode

Table 21-27. I2C_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	Reserved	R	0h	
1	STP	R/W	0h	Stop condition (I2C master mode only). This bit can be set to a 1 by the CPU to generate a stop condition. It is reset to 0 by the hardware after the stop condition has been generated. The stop condition is generated when DCOUNT passes 0. When this bit is not set to 1 before the end of the transfer (DCOUNT = 0), the stop condition is not generated and the SCL line is hold to 0 by the master, which can re-start a new transfer by setting the STT bit to 1. Value after reset is low 0x0 = No action or stop condition detected 0x1 = Stop condition queried
0	STT	R/W	0h	Start condition (I2C master mode only). This bit can be set to a 1 by the CPU to generate a start condition. It is reset to 0 by the hardware after the start condition has been generated. The start/stop bits can be configured to generate different transfer formats. Value after reset is low. Note: DCOUNT is data count value in I2C_CNT register. STT = 1, STP = 0, Conditions = Start, Bus Activities = S-A-D. STT = 0, STP = 1, Conditions = Stop, Bus Activities = P. STT = 1, STP = 1, Conditions = Start-Stop (DCOUNT=n), Bus Activities = S-A-D..(n)..D-P. STT = 1, STP = 0, Conditions = Start (DCOUNT=n), Bus Activities = S-A-D..(n)..D. 0x0 = No action or start condition detected 0x1 = Start condition queried

21.4.1.21 I2C_SA Register (offset = ACh) [reset = 0h]

I2C_SA is shown in Figure 21-36 and described in Table 21-29.

CAUTION: During an active transfer phase (between STT having been set to 1 and reception of ARDY), no modification must be done in this register. Changing it may result in an unpredictable behavior. This register is used to specify the addressed I2C module 7-bit or 10-bit address (slave address).

Figure 21-36. I2C_SA Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved						SA	
R-0h						R/W-0h	

7	6	5	4	3	2	1	0
SA							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-29. I2C_SA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	Reserved	R	0h	
9-0	SA	R/W	0h	Slave address. This field specifies either: A 10-bit address coded on SA [9:0] when XSA (Expand Slave Address, I2C_CON[8]) is set to 1. or A 7-bit address coded on SA [6:0] when XSA (Expand Slave Address, I2C_CON[8]) is cleared to 0. In this case, SA [9:7] bits must be cleared to 000 by application software. Value after reset is low (all 10 bits).

21.4.1.22 I2C_PSC Register (offset = B0h) [reset = 0h]

I2C_PSC is shown in Figure 21-37 and described in Table 21-30.

CAUTION: During an active mode (I2C_EN bit in I2C_CON register is set to 1), no modification must be done in this register. Changing it may result in an unpredictable behavior. This register is used to specify the internal clocking of the I2C peripheral core.

Figure 21-37. I2C_PSC Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
PSC							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-30. I2C_PSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	Reserved	R	0h	
7-0	PSC	R/W	0h	Fast/Standard mode prescale sampling clock divider value. The core uses this 8-bit value to divide the system clock (SCLK) and generates its own internal sampling clock (ICLK) for Fast and Standard operation modes. The core logic is sampled at the clock rate of the system clock for the module divided by (PSC + 1). Value after reset is low (all 8 bits). 0x0 = Divide by 1 0x1 = Divide by 2 0xFF = Divide by 256

21.4.1.23 I2C_SCLL Register (offset = B4h) [reset = 0h]

I2C_SCLL is shown in Figure 21-38 and described in Table 21-31.

CAUTION: During an active mode (I2C_EN bit in I2C_CON register is set to 1), no modification must be done in this register. Changing it may result in an unpredictable behavior. This register is used to determine the SCL low time value when master.

Figure 21-38. I2C_SCLL Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
SCLL							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-31. I2C_SCLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	Reserved	R	0h	
7-0	SCLL	R/W	0h	Fast/Standard mode SCL low time. I2C master mode only, (FS). This 8-bit value is used to generate the SCL low time value (tLOW) when the peripheral is operated in master mode. tLOW = (SCLL + 7) * ICLK time period, Value after reset is low (all 8 bits).

21.4.1.24 I2C_SCLH Register (offset = B8h) [reset = 0h]

I2C_SCLH is shown in Figure 21-39 and described in Table 21-32.

CAUTION: During an active mode (I2C_EN bit in I2C_CON register is set to 1), no modification must be done in this register. Changing it may result in an unpredictable behavior. This register is used to determine the SCL high time value when master.

Figure 21-39. I2C_SCLH Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved							
R-0h							

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
SCLH							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 21-32. I2C_SCLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	Reserved	R	0h	
7-0	SCLH	R/W	0h	Fast/Standard mode SCL low time. I2C master mode only, (FS). This 8-bit value is used to generate the SCL high time value (tHIGH) when the peripheral is operated in master mode. - tHIGH = (SCLH + 5) * ICLK time period. Value after reset is low (all 8 bits).