PCA9554; PCA9554A

8-bit I²C-bus and SMBus I/O port with interrupt

Rev. 9 — 19 March 2013 Product data sheet

1. General description

The PCA9554 and PCA9554A are 16-pin CMOS devices that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/SMBus applications and were developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, and so on.

The PCA9554/PCA9554A consist of an 8-bit Configuration register (Input or Output selection); 8-bit Input Port register, 8-bit Output Port register and an 8-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master. Although pin-to-pin and I²C-bus address compatible with the PCF8574 series, software changes are required due to the enhancements and are discussed in *Application Note AN469*.

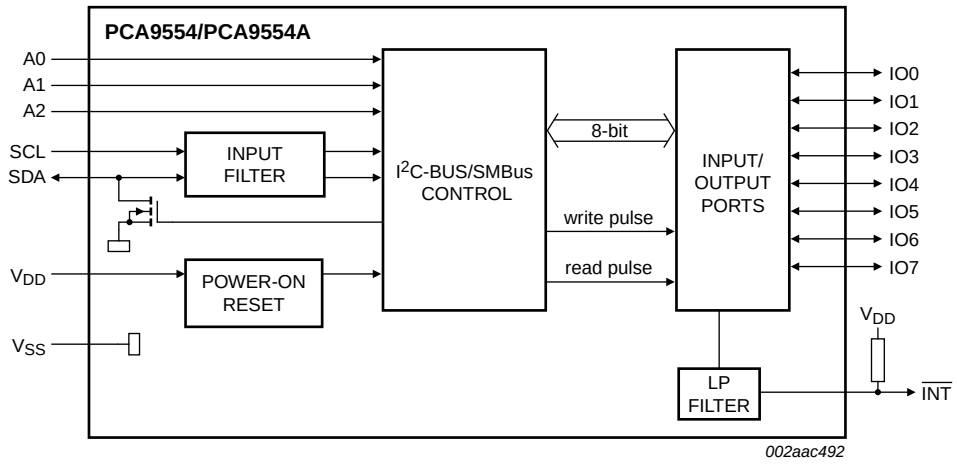
The PCA9554/PCA9554A open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus. The PCA9554A is identical to the PCA9554 except that the fixed I²C-bus address is different allowing up to sixteen of these devices (eight of each) on the same I²C-bus/SMBus.

2. Features and benefits

- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 Hz to 400 kHz clock frequency

4. Block diagram



All I/Os are set to inputs at reset.

Fig 1. Block diagram of PCA9554/PCA9554A

6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally '1' when no external signal externally applied because of the internal pull-up resistors.

Table 5. Register 0 - Input Port register bit description

Bit	Symbol	Access	Value	Description
7	I7	read only	X	determined by externally applied logic level
6	I6	read only	X	
5	I5	read only	X	
4	I4	read only	X	
3	I3	read only	X	
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6. Register 1 - Output Port register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	O7	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Table 7. Register 2 - Polarity Inversion register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	inverts polarity of Input Port register data
6	N6	R/W	0*	0 = Input Port register data retained (default value)
5	N5	R/W	0*	1 = Input Port register data inverted
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

Table 8. Register 3 - Configuration register bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins
6	C6	R/W	1*	0 = corresponding port pin enabled as an output
5	C5	R/W	1*	1 = corresponding port pin configured as input (default value)
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

6.2 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9554/PCA9554A in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9554/PCA9554A registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.3 Interrupt output

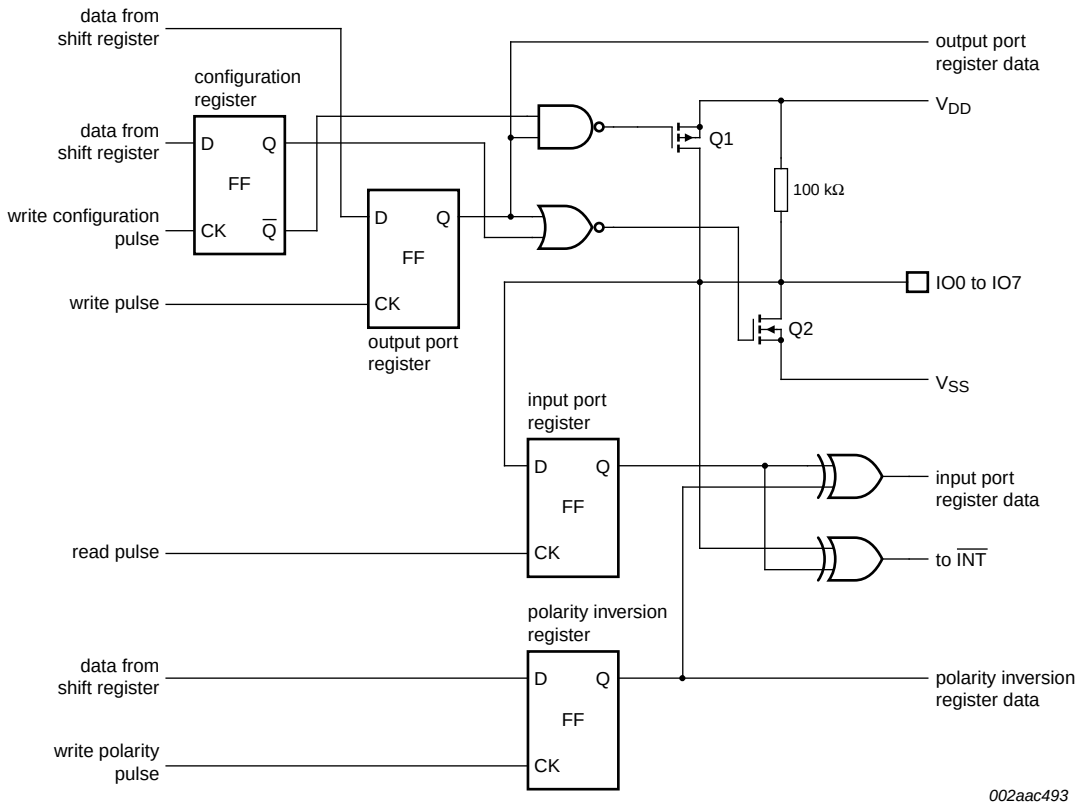
The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read.

Note that changing an I/O from and output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

6.4 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ.) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS}.



Remark: At power-on reset, all registers return to default values.

Fig 8. Simplified schematic of IO0 to IO7

6.5 Device address

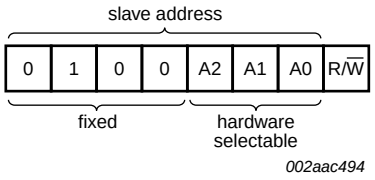


Fig 9. PCA9554 device address

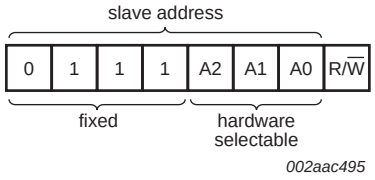


Fig 10. PCA9554A device address

6.6 Bus transactions

Data is transmitted to the PCA9554/PCA9554A registers using the Write mode as shown in Figure 11 and Figure 12. Data is read from the PCA9554/PCA9554A registers using the Read mode as shown in Figure 13 and Figure 14. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

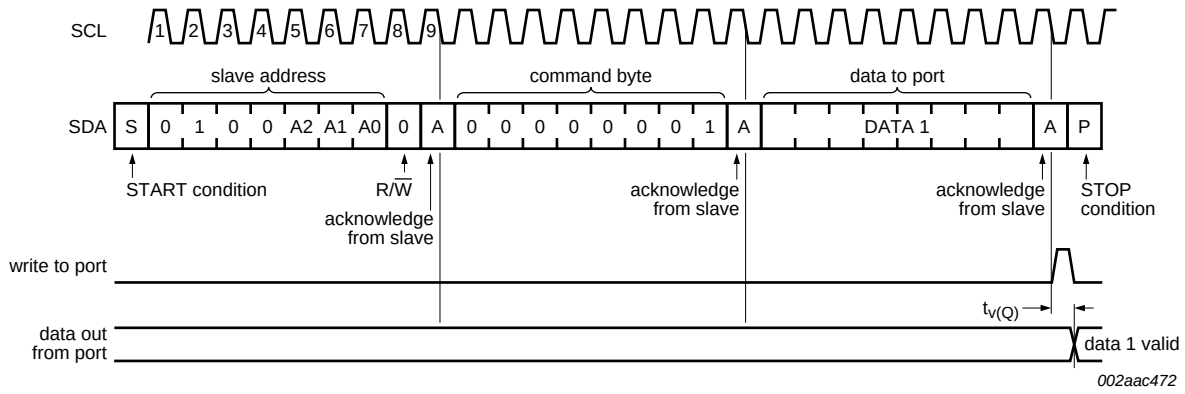


Fig 11. Write to Output Port register

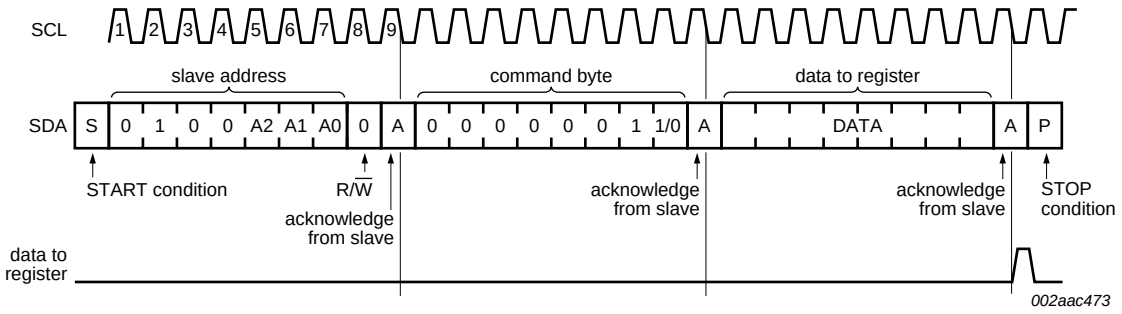


Fig 12. Write to Configuration register or Polarity Inversion register

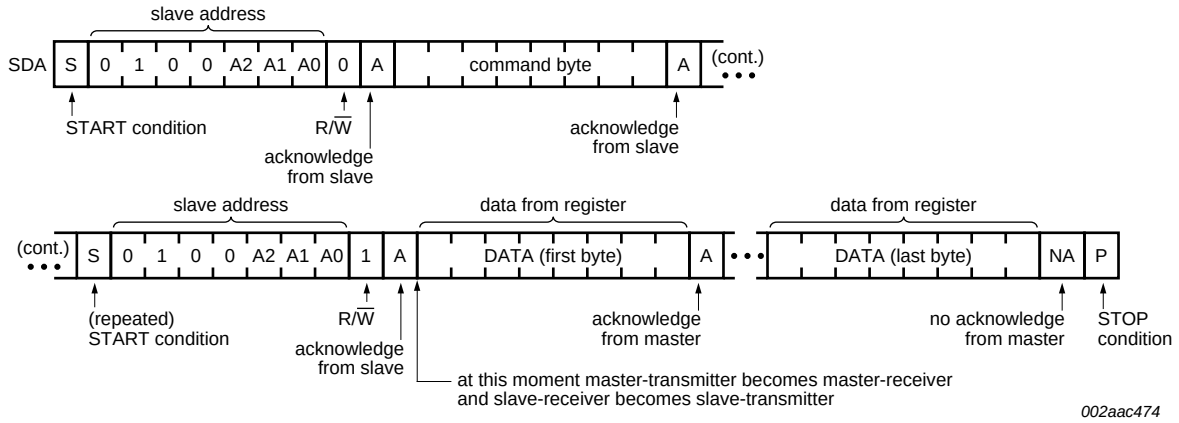
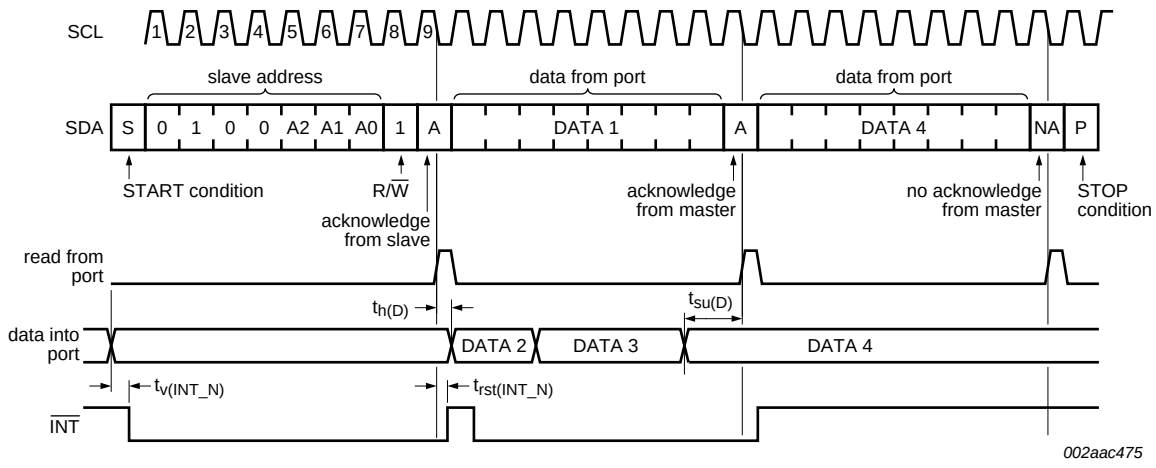


Fig 13. Read from register



This figure assumes the command byte has previously been programmed with 00h.

Transfer of data can be stopped at any moment by a STOP condition.

Fig 14. Read Input Port register