Table 9-9. DDR PHY to IO Pin Mapping (continued)

Macro Pin	CMD0	CMD1	CMD2	DATA0	DATA1
9	ddr_a9	ddr_casn	Unconn	ddr_dqs1	ddr_dqs0
10	ddr_a6	ddr_rasn	Unconn	ddr_dqsn1	ddr_dqsn0

9.3 CONTROL_MODULE Registers

Table 9-10 lists the memory-mapped registers for the CONTROL_MODULE. All other register offset addresses not listed in Table 9-10 should be considered as reserved locations and the register contents should not be modified.

Table 9-10. CONTROL_MODULE REGISTERS

Offset	Acronym	Register Description	Section
0h	control_revision		Section 9.3.1
4h	control_hwinfo		Section 9.3.2
10h	control_sysconfig		Section 9.3.3
40h	control_status		Section 9.3.4
110h	control_emif_sdram_config		Section 9.3.5
41Ch	cortex_vbbldo_ctrl		Section 9.3.5
428h	core_sldo_ctrl		Section 9.3.6
42Ch	mpu_sldo_ctrl		Section 9.3.7
444h	clk32kdivratio_ctrl		Section 9.3.8
448h	bandgap_ctrl		Section 9.3.9
44Ch	bandgap_trim		Section 9.3.10
458h	pll_clkinpulow_ctrl		Section 9.3.11
468h	mosc_ctrl		Section 9.3.12
470h	deepsleep_ctrl		Section 9.3.13
50Ch	dpll_pwr_sw_status		Section 9.3.14
600h	device_id		Section 9.3.15
604h	dev_feature		Section 9.3.16
608h	init_priority_0		Section 9.3.17
60Ch	init_priority_1		Section 9.3.18
610h	mmu_cfg		Section 9.3.19
614h	tptc_cfg		Section 9.3.20
620h	usb_ctrl0		Section 9.3.21
624h	usb_sts0		Section 9.3.22
628h	usb_ctrl1		Section 9.3.23
62Ch	usb_sts1		Section 9.3.24
630h	mac_id0_lo		Section 9.3.25
634h	mac_id0_hi		Section 9.3.26
638h	mac_id1_lo		Section 9.3.27
63Ch	mac_id1_hi		Section 9.3.28
644h	dcan_raminit		Section 9.3.29
648h	usb_wkup_ctrl		Section 9.3.30
650h	gmii_sel		Section 9.3.31
664h	pwmss_ctrl		Section 9.3.32
670h	mreqprio_0		Section 9.3.33
674h	mreqprio_1		Section 9.3.34
690h	hw_event_sel_grp1		Section 9.3.35

Table 9-10. CONTROL_MODULE REGISTERS (continued)

Offset	Acronym	Register Description	Section
694h	hw_event_sel_grp2		Section 9.3.36
698h	hw_event_sel_grp3		Section 9.3.37
69Ch	hw_event_sel_grp4		Section 9.3.38
6A0h	smrt_ctrl		Section 9.3.39
6A4h	mpuss_hw_debug_sel		Section 9.3.40
6A8h	mpuss_hw_dbg_info		Section 9.3.41
770h	vdd_mpu_opp_050		Section 9.3.42
774h	vdd_mpu_opp_100		Section 9.3.43
778h	vdd_mpu_opp_120		Section 9.3.44
77Ch	vdd_mpu_opp_turbo		Section 9.3.45
7B8h	vdd_core_opp_050		Section 9.3.46
7BCh	vdd_core_opp_100		Section 9.3.47
7D0h	bb_scale		Section 9.3.48
7F4h	usb_vid_pid		Section 9.3.49
7FCh	efuse_sma		Section 9.3.50
800h	conf_gpmc_ad0	See the device datasheet for information on default pin mux configurations. Note that the device ROM may change the default pin mux for certain pins based on the SYSBOOT mode settings.	Section 9.3.51
804h	conf_gpmc_ad1		Section 9.3.51
808h	conf_gpmc_ad2		Section 9.3.51
80Ch	conf_gpmc_ad3		Section 9.3.51
810h	conf_gpmc_ad4		Section 9.3.51
814h	conf_gpmc_ad5		Section 9.3.51
818h	conf_gpmc_ad6		Section 9.3.51
81Ch	conf_gpmc_ad7		Section 9.3.51
820h	conf_gpmc_ad8		Section 9.3.51
824h	conf_gpmc_ad9		Section 9.3.51
828h	conf_gpmc_ad10		Section 9.3.51
82Ch	conf_gpmc_ad11		Section 9.3.51
830h	conf_gpmc_ad12		Section 9.3.51
834h	conf_gpmc_ad13		Section 9.3.51
838h	conf_gpmc_ad14		Section 9.3.51
83Ch	conf_gpmc_ad15		Section 9.3.51
840h	conf_gpmc_a0		Section 9.3.51
844h	conf_gpmc_a1		Section 9.3.51
848h	conf_gpmc_a2		Section 9.3.51
84Ch	conf_gpmc_a3		Section 9.3.51
850h	conf_gpmc_a4		Section 9.3.51
854h	conf_gpmc_a5		Section 9.3.51
858h	conf_gpmc_a6		Section 9.3.51
85Ch	conf_gpmc_a7		Section 9.3.51
860h	conf_gpmc_a8		Section 9.3.51
864h	conf_gpmc_a9		Section 9.3.51
868h	conf_gpmc_a10		Section 9.3.51
86Ch	conf_gpmc_a11		Section 9.3.51
870h	conf_gpmc_wait0		Section 9.3.51
874h	conf_gpmc_wpn		Section 9.3.51

Table 9-10. CONTROL_MODULE REGISTERS (continued)

Offset	Acronym	Register Description	Section
878h	conf_gpmc_ben1		Section 9.3.51
87Ch	conf_gpmc_csn0		Section 9.3.51
880h	conf_gpmc_csn1		Section 9.3.51
884h	conf_gpmc_csn2		Section 9.3.51
888h	conf_gpmc_csn3		Section 9.3.51
88Ch	conf_gpmc_clk		Section 9.3.51
890h	conf_gpmc_advn_ale		Section 9.3.51
894h	conf_gpmc_oen_ren		Section 9.3.51
898h	conf_gpmc_wen		Section 9.3.51
89Ch	conf_gpmc_ben0_cle		Section 9.3.51
8A0h	conf_lcd_data0		Section 9.3.51
8A4h	conf_lcd_data1		Section 9.3.51
8A8h	conf_lcd_data2		Section 9.3.51
8ACh	conf_lcd_data3		Section 9.3.51
8B0h	conf_lcd_data4		Section 9.3.51
8B4h	conf_lcd_data5		Section 9.3.51
8B8h	conf_lcd_data6		Section 9.3.51
8BCh	conf_lcd_data7		Section 9.3.51
8C0h	conf_lcd_data8		Section 9.3.51
8C4h	conf_lcd_data9		Section 9.3.51
8C8h	conf_lcd_data10		Section 9.3.51
8CCh	conf_lcd_data11		Section 9.3.51
8D0h	conf_lcd_data12		Section 9.3.51
8D4h	conf_lcd_data13		Section 9.3.51
8D8h	conf_lcd_data14		Section 9.3.51
8DCh	conf_lcd_data15		Section 9.3.51
8E0h	conf_lcd_vsync		Section 9.3.51
8E4h	conf_lcd_hsync		Section 9.3.51
8E8h	conf_lcd_pclk		Section 9.3.51
8ECh	conf_lcd_ac_bias_en		Section 9.3.51
8F0h	conf_mmc0_dat3		Section 9.3.51
8F4h	conf_mmc0_dat2		Section 9.3.51
8F8h	conf_mmc0_dat1		Section 9.3.51
8FCh	conf_mmc0_dat0		Section 9.3.51
900h	conf_mmc0_clk		Section 9.3.51
904h	conf_mmc0_cmd		Section 9.3.51
908h	conf_mii1_col		Section 9.3.51
90Ch	conf_mii1_crs		Section 9.3.51
910h	conf_mii1_rx_er		Section 9.3.51
914h	conf_mii1_tx_en		Section 9.3.51
918h	conf_mii1_rx_dv		Section 9.3.51
91Ch	conf_mii1_txd3		Section 9.3.51
920h	conf_mii1_txd2		Section 9.3.51
924h	conf_mii1_txd1		Section 9.3.51
928h	conf_mii1_txd0		Section 9.3.51
92Ch	conf_mii1_tx_clk		Section 9.3.51
930h	conf_mii1_rx_clk		Section 9.3.51

Table 9-10. CONTROL_MODULE REGISTERS (continued)

Offset	Acronym	Register Description	Section
934h	conf_mii1_rxd3		Section 9.3.51
938h	conf_mii1_rxd2		Section 9.3.51
93Ch	conf_mii1_rxd1		Section 9.3.51
940h	conf_mii1_rxd0		Section 9.3.51
944h	conf_rmii1_ref_clk		Section 9.3.51
948h	conf_mdio		Section 9.3.51
94Ch	conf_mdc		Section 9.3.51
950h	conf_spi0_sclk		Section 9.3.51
954h	conf_spi0_d0		Section 9.3.51
958h	conf_spi0_d1		Section 9.3.51
95Ch	conf_spi0_cs0		Section 9.3.51
960h	conf_spi0_cs1		Section 9.3.51
964h	conf_ecap0_in_pwm0_out		Section 9.3.51
968h	conf_uart0_ctsn		Section 9.3.51
96Ch	conf_uart0_rtsn		Section 9.3.51
970h	conf_uart0_rxd		Section 9.3.51
974h	conf_uart0_txd		Section 9.3.51
978h	conf_uart1_ctsn		Section 9.3.51
97Ch	conf_uart1_rtsn		Section 9.3.51
980h	conf_uart1_rxd		Section 9.3.51
984h	conf_uart1_txd		Section 9.3.51
988h	conf_i2c0_sda		Section 9.3.51
98Ch	conf_i2c0_scl		Section 9.3.51
990h	conf_mcasp0_aclkx		Section 9.3.51
994h	conf_mcasp0_fsx		Section 9.3.51
998h	conf_mcasp0_axr0		Section 9.3.51
99Ch	conf_mcasp0_ahclkr		Section 9.3.51
9A0h	conf_mcasp0_aclkr		Section 9.3.51
9A4h	conf_mcasp0_fsr		Section 9.3.51
9A8h	conf_mcasp0_axr1		Section 9.3.51
9ACh	conf_mcasp0_ahclkx		Section 9.3.51
9B0h	conf_xdma_event_intr0		Section 9.3.51
9B4h	conf_xdma_event_intr1		Section 9.3.51
9B8h	conf_warmrstn		Section 9.3.51
9C0h	conf_nnmi		Section 9.3.51
9D0h	conf_tms		Section 9.3.51
9D4h	conf_tdi		Section 9.3.51
9D8h	conf_tdo		Section 9.3.51
9DCh	conf_tck		Section 9.3.51
9E0h	conf_trstn		Section 9.3.51
9E4h	conf_emu0		Section 9.3.51
9E8h	conf_emu1		Section 9.3.51
9F8h	conf_rtc_pwronrstn		Section 9.3.51
9FCh	conf_pmic_power_en		Section 9.3.51
A00h	conf_ext_wakeup		Section 9.3.51
A04h	conf_rtc_kaldo_enn		Section 9.3.51
A1Ch	conf_usb0_drvvbus		Section 9.3.51

Table 9-10. CONTROL_MODULE REGISTERS (continued)

Offset	Acronym	Register Description	Section
A34h	conf_usb1_drvvbus		Section 9.3.51
E00h	cqdetect_status		Section 9.3.52
E04h	ddr_io_ctrl		Section 9.3.53
E0Ch	vtp_ctrl		Section 9.3.54
E14h	vref_ctrl		Section 9.3.55
F90h	tpcc_evt_mux_0_3		Section 9.3.56
F94h	tpcc_evt_mux_4_7		Section 9.3.57
F98h	tpcc_evt_mux_8_11		Section 9.3.58
F9Ch	tpcc_evt_mux_12_15		Section 9.3.59
FA0h	tpcc_evt_mux_16_19		Section 9.3.60
FA4h	tpcc_evt_mux_20_23		Section 9.3.61
FA8h	tpcc_evt_mux_24_27		Section 9.3.62
FACh	tpcc_evt_mux_28_31		Section 9.3.63
FB0h	tpcc_evt_mux_32_35		Section 9.3.64
FB4h	tpcc_evt_mux_36_39		Section 9.3.65
FB8h	tpcc_evt_mux_40_43		Section 9.3.66
FBCh	tpcc_evt_mux_44_47		Section 9.3.67
FC0h	tpcc_evt_mux_48_51		Section 9.3.68
FC4h	tpcc_evt_mux_52_55		Section 9.3.69
FC8h	tpcc_evt_mux_56_59		Section 9.3.70
FCCh	tpcc_evt_mux_60_63		Section 9.3.71
FD0h	timer_evt_capt		Section 9.3.72
FD4h	ecap_evt_capt		Section 9.3.73
FD8h	adc_evt_capt		Section 9.3.74
1000h	reset_iso		Section 9.3.75
1318h	dpll_pwr_sw_ctrl		Section 9.3.76
131Ch	ddr_cke_ctrl		Section 9.3.77
1320h	sma2		Section 9.3.78
1324h	m3_txev_eoi		Section 9.3.79
1328h	ipc_msg_reg0		Section 9.3.80
132Ch	ipc_msg_reg1		Section 9.3.81
1330h	ipc_msg_reg2		Section 9.3.82
1334h	ipc_msg_reg3		Section 9.3.83
1338h	ipc_msg_reg4		Section 9.3.84
133Ch	ipc_msg_reg5		Section 9.3.85
1340h	ipc_msg_reg6		Section 9.3.86
1344h	ipc_msg_reg7		Section 9.3.87
1404h	ddr_cmd0_ioctrl		Section 9.3.88
1408h	ddr_cmd1_ioctrl		Section 9.3.89
140Ch	ddr_cmd2_ioctrl		Section 9.3.90
1440h	ddr_data0_ioctrl		Section 9.3.91
1444h	ddr_data1_ioctrl		Section 9.3.92

9.3.51 conf_<module>_<pin> Register (offset = 800h–A34h)

See the device datasheet for information on default pin mux configurations. Note that the device ROM may change the default pin mux for certain pins based on the SYSBOOT mode settings.

See Table 9-10, *Control Module Registers Table*, for the full list of offsets for each module/pin configuration.

conf_<module>_<pin> is shown in Figure 9-54 and described in Table 9-61.

Figure 9-54. conf_<module>_<pin> Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							

23	22	21	20	19	18	17	16
Reserved				Reserved			
R-0h				R-0h			

15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved	conf_<module>_<pin>_slewctrl	conf_<module>_<pin>_rxactive	conf_<module>_<pin>_putypesel	conf_<module>_<pin>_puden	conf_<module>_<pin>_mmode		
R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 9-61. conf_<module>_<pin> Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	
19-7	Reserved	R	0h	
6	conf_<module>_<pin>_slewctrl	R/W	X	Select between faster or slower slew rate 0: Fast 1: Slow Reset value is pad-dependent.
5	conf_<module>_<pin>_rxactive	R/W	1h	Input enable value for the PAD 0: Receiver disabled 1: Receiver enabled
4	conf_<module>_<pin>_putypesel	R/W	X	Pad pullup/pulldown type selection 0: Pulldown selected 1: Pullup selected Reset value is pad-dependent.
3	conf_<module>_<pin>_puden	R/W	X	Pad pullup/pulldown enable 0: Pullup/pulldown enabled 1: Pullup/pulldown disabled Reset value is pad-dependent.
2-0	conf_<module>_<pin>_mmode	R/W	X	Pad functional signal mux select. Reset value is pad-dependent.