20.1.5.9 TCLR Register (offset = 38h) [reset = 0h]

TCLR is shown in Figure 20-17 and described in Table 20-19.

When the TCM field passed from (00) to any other combination then the TCAR_IT_FLAG and the edge detection logic are cleared. The ST bit of TCLR register may be updated from the OCP interface or reset due to one-shot overflow. The OCP interface update has the priority.

Figure 20-17. TCLR Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved	GPO_CFG	CAPT_MODE	PT	TRG		TCM	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
SCPWM	CE	PRE	PTV			AR	ST
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 20-19. TCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	Reserved	R	0h	
14	GPO_CFG	R/W	0h	General purpose output this register drives directly the PORGPOCFG output pin 0x0 = PORGPOCFG drives 0 and configures the timer pin as an output. 0x1 = PORGPOCFG drives 1 and configures the timer pin as an input.
13	CAPT_MODE	R/W	0h	Capture mode. 0x0 = Single capture 0x1 = Capture on second event
12	PT	R/W	0h	Pulse or toggle mode on PORTIMERPWM output pin 0x0 = Pulse 0x1 = Toggle
11-10	TRG	R/W	0h	Trigger output mode on PORTIMERPWM output pin 0x0 = No trigger 0x1 = Trigger on overflow 0x2 = Trigger on overflow and match 0x3 = Reserved
9-8	TCM	R/W	0h	Transition Capture Mode on PIEVENTCAPT input pin 0x0 = No capture 0x1 = Capture on low to high transition 0x2 = Capture on high to low transition 0x3 = Capture on both edge transition
7	SCPWM	R/W	0h	This bit should be set or clear while the timer is stopped or the trigger is off 0x0 = Clear the PORTIMERPWM output pin and select positive pulse for pulse mode 0x1 = Set the PORTIMERPWM output pin and select negative pulse for pulse mode

Table 20-19. TCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CE	R/W	0h	0x0 = Compare mode is disabled 0x1 = Compare mode is enabled
5	PRE	R/W	0h	Prescaler enable 0x0 = The TIMER clock input pin clocks the counter 0x1 = The divided input pin clocks the counter
4-2	PTV	R/W	0h	Pre-scale clock Timer value
1	AR	R/W	0h	0x0 = One shot timer 0x1 = Auto-reload timer
0	ST	R/W	0h	In the case of one-shot mode selected (AR = 0), this bit is automatically reset by internal logic when the counter is overflowed. 0x0(READ) = Stop timeOnly the counter is frozen 0x1 = Start timer

20.1.5.10 TCRR Register (offset = 3Ch) [reset = 0h]

TCRR is shown in Figure 20-18 and described in Table 20-20.

The TCRR register is a 32-bit register, 16-bit addressable. The MCU can perform a 32-bit access or two 16-bit accesses to access the register . Note that since the OCP clock is completely asynchronous with the timer clock, some synchronization is done in order to make sure that the TCRR value is not read while it is being incremented. In 16-bit mode the following sequence must be followed to read the TCRR register properly: First, perform an OCP Read Transaction to Read the lower 16-bit of the TCRR register (offset = 28h). When the TCRR is read and synchronized, the lower 16-bit LSBs are driven onto the output OCP data bus and the upper 16-bit MSBs of the TCRR register are stored in a temporary register. Second, perform an OCP Read Transaction to read the upper 16-bit of the TCRR register (offset = 2Ah). During this Read, the value of the upper 16-bit MSBs that has been temporary register is forwarded onto the output OCP data bus. So, to read the value of TCRR correctly, the first OCP read access has to be to the lower 16-bit (offset = 28h), followed by OCP read access to the upper 16-bit (offset = 2Ah). As the TCRR is updated using more sources (shadow_in_tcrr, incremented value of tcrr, TLDR and 0), a priority order will be defined: The first priority is the OCP update. The second is the reload way (triggered through TTGR reg. or following an auto-reload overflow). The third is the one-shot overflow reset to 0. The last is the incremented value.

Figure 20-18. TCRR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMER_COUNTER																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 20-20. TCRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIMER_COUNTER	R/W	0h	Value of TIMER counter

20.1.5.11 TLDR Register (offset = 40h) [reset = 0h]

TLDR is shown in Figure 20-19 and described in Table 20-21.

LOAD_VALUE must be different than the timer overflow value (FFFF FFFFh).

Figure 20-19. TLDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAD_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 20-21. TLDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOAD_VALUE	R/W	0h	Timer counter value loaded on overflow in auto-reload mode or on TTGR write access

20.1.5.14 TMAR Register (offset = 4Ch) [reset = 0h]

TMAR is shown in Figure 20-22 and described in Table 20-24.

The compare logic consists of a 32-bit wide, read/write data TMAR register and logic to compare counter s current value with the value stored in the TMAR register.

Figure 20-22. TMAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARE_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 20-24. TMAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMPARE_VALUE	R/W	0h	Value to be compared to the timer counter

20.1.5.5 IRQSTATUS Register (offset = 28h) [reset = 0h]

IRQSTATUS is shown in Figure 20-13 and described in Table 20-15.

Component interrupt request status. Check the corresponding secondary status register. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).

Figure 20-13. IRQSTATUS Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved					TCAR_IT_FLAG	OVF_IT_FLAG	MAT_IT_FLAG
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 20-15. IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	Reserved	R	0h	
2	TCAR_IT_FLAG	R/W	0h	IRQ status for Capture 0x0(W) = No action 0x0(R) = No event pending 0x1(W) = Clear pending event, if any 0x1(R) = IRQ event pending
1	OVF_IT_FLAG	R/W	0h	IRQ status for Overflow 0x0(W) = No action 0x0(R) = No event pending 0x1(W) = Clear pending event, if any 0x1(R) = IRQ event pending
0	MAT_IT_FLAG	R/W	0h	IRQ status for Match 0x0(W) = No action 0x0(R) = No event pending 0x1(W) = Clear pending event, if any 0x1(R) = IRQ event pending

20.1.5.6 IRQENABLE_SET Register (offset = 2Ch) [reset = 0h]

IRQENABLE_SET is shown in Figure 20-14 and described in Table 20-16.

Component interrupt request enable. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.

Figure 20-14. IRQENABLE_SET Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved					TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 20-16. IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	Reserved	R	0h	
2	TCAR_EN_FLAG	R/W	0h	IRQ enable for Capture 0x0(W) = No action 0x0(R) = IRQ event is disabled 0x1(W) = Set IRQ enable 0x1(R) = IRQ event is enabled
1	OVF_EN_FLAG	R/W	0h	IRQ enable for Overflow 0x0(W) = No action 0x0(R) = IRQ event is disabled 0x1(W) = Set IRQ enable 0x1(R) = IRQ event is enabled
0	MAT_EN_FLAG	R/W	0h	IRQ enable for Match 0x0(W) = No action 0x0(R) = IRQ event is disabled 0x1(W) = Set IRQ enable 0x1(R) = IRQ event is enabled

20.1.5.7 IRQENABLE_CLR Register (offset = 30h) [reset = 0h]

IRQENABLE_CLR is shown in Figure 20-15 and described in Table 20-17.

Component interrupt request enable. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.

Figure 20-15. IRQENABLE_CLR Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							
7	6	5	4	3	2	1	0
Reserved					TCAR_EN_FLAG	OVF_EN_FLAG	MAT_EN_FLAG
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 20-17. IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	Reserved	R	0h	
2	TCAR_EN_FLAG	R/W	0h	IRQ enable for Capture 0x0(W) = No action 0x0(R) = IRQ event is disabled 0x1(W) = Clear IRQ enable 0x1(R) = IRQ event is enabled
1	OVF_EN_FLAG	R/W	0h	IRQ enable for Overflow 0x0(W) = No action 0x0(R) = IRQ event is disabled 0x1(W) = Clear IRQ enable 0x1(R) = IRQ event is enabled
0	MAT_EN_FLAG	R/W	0h	IRQ enable for Match 0x0(W) = No action 0x0(R) = IRQ event is disabled 0x1(W) = Clear IRQ enable 0x1(R) = IRQ event is enabled