Lab. Practice 3 (Extra part)

4x4-bit multipliers

Objective

- Modify the 4x4-bit multiplier based on adders to reduce the combinational path delay using segmentation registers.
- Use the test bench in the VC (no modifications allowed)
- Obtain:
  - Minimum period (Max. Frequency)
  - Minimum input arrival time before clock
  - Maximum output required time after clock
- Compare with previous results

Implementation