COMP4300

Lab Exercise One, Spring 2021

Objective

This lab is aimed at getting you familiar with using the ModelSim simulator. The circuits you will be simulating should be familiar to you from your digital logic course.

Instructions

Write a VHDL program consisting of a single entity whose architecture is a single process that implements an XOR gate. That is, a circuit which behaves as specified in the following truth table. You should implement your architecture as a single process.

- ```
  inputs            |outputs
  ```
- ```
  ------------------+---------------
  ```
- ```
  a_in     b_in     | result
  ```
- ```
  ------------------+---------------
  ```
- ```
  0        0        | 0
  ```
- ```
  0        1        | 1
  ```
- ```
  1        0        | 1
  ```
- ```
  1        1        | 0
  ```

Use exactly the names given above for the signals. All your signals should be of type `bit` (NOT integer).

Deliverables

Please turn in the following things for this lab, as a single zip file:

- o   The file with your VHDL code.
- o   A screen shot of your exhaustive simulation.
- o   A screen shot of a successful compilation of your code.

Due Date

January 29, 2021 at 11:59pm.