FOX-1 Camera Board

Software Group

Mitch Davis, Kevin Burns

Virginia Tech

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Overview

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Key Components

System Architecture

- Processor: STM32L151ZDT6
- Operating System: ChibiOS/RT

Hardware Capabilities

- 32MHz Processor @ 238 uA/MHz
- 382 KB ECC Flash, 48 KB ECC SRAM, 12 KB ECC EEPROM
- 382 KB Dual-Port DRAM FIFO
- 1Mb 40MHz SPI MRAM
- 400 kHz SCCB (I2C compatible) Camera Control
- Two 19.2 kbaud UART

Operating System

Key Features

- 1.2-5.5 KiB Kernel Size
- 128 thread priority levels
- Preemptive scheduling, Round-Robin schedular for like priorities
- Mutexes, Semaphores, Events, Message Queues
- Thread-safe Heap
- Hardware Abstraction Layer with DMA support for STM32L1
- GPLv3

JPEG Compressor

jpegant

- JPEG Compressor code is based off the jpegant lightweight JPEG library
- Integer DCT
- Low memory footprint
- GPLv2 (Author will re-release under GPLv3 per our request)

Task Diagram

Task Diagram

System Operation Flowchart

System Operation Flowchart

Programming Task List

Programming Task List

State of Development

- STM32L152xB Development Boards received on Tuesday
- Existing STM32F4 code ported and runs successfully as of Tuesday
- OV7670 SCCB Interface is in work
- Need to discuss interface communications with IHU folks