

2022/06/17

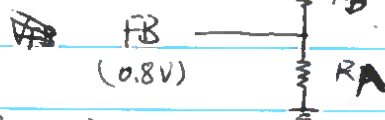
RV1 - potencionmeter - adjustable resistor

- Freq pin - resistor - GND

↓
determine frequency (switches) $320\text{ kHz} \sim 2.25\text{ MHz}$

RV2 - ITH pin.

$V_{FB} = 0.8\text{ V}$



$$\left(\frac{R_B}{R_A} + 1 \right) \cdot \frac{R_A + R_B}{R_A} \times 0.8 = V_{out}$$

✶ V_{FB} : Regulated Feedback Voltage

$I_{TH} \text{ voltage} = 1.2\text{ V}$

★ LTC780 is tested in a feedback loop that senses V_{ITH} to a specified voltage and measures the resultant V_{FB}

Pin 8: ITH: Error Amplifier Outputs and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

Main Control Loop.

→ Current mode step-down architecture

Top MOSFET on - RS latch (clock)

off - main current comparator $ICMP$ resets RS latch

↑
the peak inductor current and resets the latch is controlled by ITH pin

↓
output of EA error amplifier

Compare signal at V_{FB}

and internal 0.800 V reference

If load current \uparrow $V_{FB} \downarrow$ (due to less current flow in this branch.)

Thus $V_{FB} < \text{reference } 0.800\text{ V}$

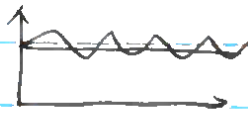
EA increases ITH voltage until the average inductor current matches the new load current

ITH \rightarrow Optimization of control loop behavior.

\rightarrow DC coupled and AC filtered close-loop response test point
直流耦合和交流滤波

Coupling: 2个以及2个以上电路元件输入输出之间存在紧密配合与相互影响

DC coupled: DC & AC



\rightarrow Phase margin & damping factor & Bandwidth (2nd order system)

can be estimated by this point

percentage of overshoot seen at pin ITH

\downarrow examining the rise time at this pin

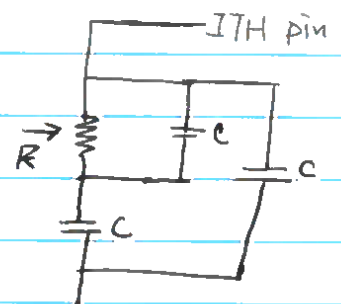
\Rightarrow ITH pin waveforms will give a sense of the overall loop stability without breaking the feedback loop

ITH series RC-CC filter sets the dominant pole-zero loop compensation.

Loop gain increase by increasing RC

Loop bandwidth increase by decreasing CC

If RC increase as same factor as CC decrease
zero freq keeps the same, same phase shift
in the most critical freq range of feedback loop



Stability of closed-loop system.

RV3 & RV4 for SPDT: SN74LVC1G3157

B0, B1 pin

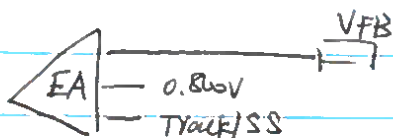
This is for setpoint circuit - providing Track/SS pin.

Track/SS \rightarrow External tracking & Soft-start point

LTC78W regulates V_{FB} = smaller 0.8 or Voltage at Track/SS pin

\rightarrow Internal 10mA pull-up current source connected.

\rightarrow Capacitor to GND at this pin sets the ramp time to final V_{out} .



Shutdown & Start-Up

$V_{IN} < 1.6V$ shuts down the main control loop

$< 0.7V$ disable controller and internal circuit.

$V_{IN} \leq 8V$. (absolute max rating of)

$\leq 10\mu A$

internal 11V voltage clamp

Start-up of controller's output voltage V_{out} is controlled by Track/SS pin.

① $V_{SS} < 0.8V$ internal reference $\Rightarrow V_{FB} = V_{SS}$ instead of $0.8V$

② V_{SS} - Capacitor (external) SS - Cap - SGND \Rightarrow Soft-start $10\mu A$ internal pull-up current.

V_{SS} from $0V$ to $0.8V$ gradually (or $5V$)

V_{out} from $0V$ to final value

③ V_{out} track another supply.

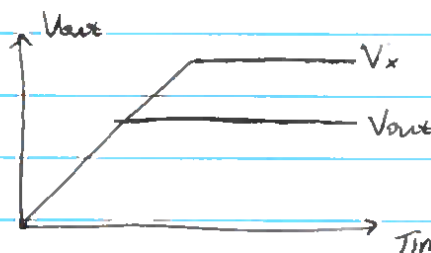
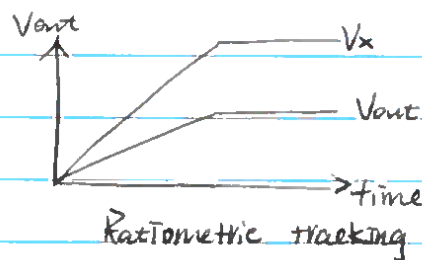
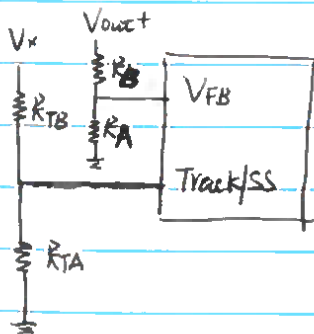
SS - ~~another~~ external resistor divider from another supply to GND

Total soft start time = $t_{ss} = C_{ss} \cdot \frac{0.8V}{10\mu A}$



③ V_{out} track V_x

$$\frac{V_x}{V_{out}} = \frac{R_A}{R_{TrackA}} \times \frac{R_{TrackA}^2 + R_{TrackB}^2}{R_A + R_B}$$



$\Rightarrow R_A = R_{TrackA}$
 $R_B = R_{TrackB}$