Electronic Load:

This circuit might not be able to test in bread board: 1) LTspice to simulate the performance 2) Build one with high ohmic shunt resistance and check the control principle of the electronic load.

First of all, the MOSFET model that use in the LTspice can be specified into a suitable version. This can be achieved by setting C:\Program Files\LTC\LTspiceXVII\lib\cmp\standard.MOS, add new MOSFET model here in the standard library for MOSFET. Open LTspice -> Edit -> Component -> nmos/pmos -> right click on the item -> pick new MOSFET -> select the import MOSFET model. (Notice, the standard file in the library may also appears at: C:\Users\Yixuan\AppData\Local\LTspiceXVII\lib\cmp\standard.MOS, if the specific model can not be found by "pick new MOSFET", better to correct both standard files at these two directions.)

Not all MOSFET has their spice model that can be found online. I can start with MOSFET with spice model, if the circuit work, then i can transfer the parameters of new MOSFE into spice model layout, and then check it with the old circuit again.

The spice model parameters of MOSFET stands for:

https://help.simetrix.co.uk/8.4/simetrix/simulator_reference/topics/analogdevicereference_mosfet.htm

Name	Model Parameters	Units	Default
LEVEL	Model type (1, 2, or 3)		1
L	Channel length	meters	DEFL
W	Channel width	meters	DEFW
LD	Lateral diffusion length	meters	0
WD	Lateral diffusion width	meters	0
VTO	Zero-bias threshold voltage	volts	0
KP	Transconductance	Amps/Volts2	2.00E-05
GAMMA	Bulk threshold parameter	Volts1/2	0
PHI	Surface potential	Volts	0.6
LAMBDA	Channel-length modulation (LEVEL = 1or 2)	Volts-1	0
RD	Drain ohmic resistance	Ohms	0
RS	Source ohmic resistance	Ohms	0
RG	Gate ohmic resistance	Ohms	0
RB	Bulk ohmic resistance	Ohms	0
RDS	Drain-source shunt resistance	Ohms	infinity
RSH	Drain-source diffusion sheet resistance	Ohms/meter2	0
IS	Bulk p-n saturation current	Amps	1.00E-14
JS	Bulk p-n saturation/current area	Amps/meters2	0
PB	Bulk p-n potential	Volts	0.8
CBD	Bulk-drain zero-bias p-n capacitance	Farads	0
CBS	Bulk-source zero-bias p-n capacitance		
CJ	Bulk p-n zero-bias bottom capacitance/length	Farads/meters2	0
CJSW	Bulk p-n zero-bias perimeter capacitance/length	Farads/meters	
MJ	Bulk p-n bottom grading coefficient		0.5
MJSW	Bulk p-n sidewall grading coefficient		0.33
FC	Bulk p-n forward-bias capacitance coefficient		0.5
CGSO	Gate-source overlap capacitance/channel width	Farads/meters	0
CGDO	Gate-drain overlap capacitance/channel width	Farads/meters	0
CGBO	Gate-bulk overlap capacitance/channel width	Farads/meters	0
NSUB	Substate doping density	1/centimeter3	0
NSS	Surface-state density	1/centimeter2	0
NFS	Fast surface-state density	1/centimeter3	0
TOX	Oxide thickness	meters	infinity
TPG	Gate material type		
	(opposite of substrate/ same as substrate/aluminum)		
XJ	Metallurgical junction depth	meters	0
UCRIT	Mobility degradation critical field (LEVEL = 2)	Volts/centimete	1.00E+04
UEXP	Mobility degradation exponent (LEVEL = 2)		0
UTRA	(Not Used) mobility degradation transverse field coefficient		
VMAX	Maximum drift velocity	meters/seconds	0
NEFF	Channel charge coefficient (LEVEL = 2)		1
XQC	Fraction of channel charge attributed to drain		1
DELTA	Width effect on threshold		0
THETA	Mobility modulation (LEVEL = 3)	Volts-1	0
ETA	Static feedback (LEVEL = 3)		0
KAPPA	Saturation field factor (LEVEL=3)		0.2
KF	Flicker noise coefficient		0
AF	Flicker noise exponent		1

Buck converter - electronic load requirements:

(Lab course: 1-5V voltage output & 4A max current output)

Experiment: Minimum load resistance:

Vload = 5V & Iload = 4A -> Rload = 1.25Ω

Vload = 3.3V & Iload = 4A -> Rload = 0.825Ω

Vload = 1.75V & Iload = 3.9A -> Rload = 0.45Ω

Experiment idea: minimum output voltage with maximum output current can get the minimum load resistance that required for this course.

However, the buck converter cannot provide high current output when output voltage reference set too low.

When Vout was set to 1V, and current cannot reach to 4A even when setting the slide potentiometer to the lowest side.

(This is because the smallest number for the slide potentiometer is around 0.4Ω)

Then slightly increase the reference output voltage, and check the maximum output current it can achieve.

When Vout was set to 1.8V, the output current can achieve 3.9A and the output voltage was dropped to 1.75V, getting 0.45Ω load resistance.

The lab course also require students to explore the converter performance when the outputs are shorted.

This simply means directly connected Vout+ and Vout-. When the outputs were shorted, the buck converter will stop converting energy - Vout immediately drops to 0.5V ~ 1V and Iout suddenly increase to 5A.

The range for set reference output voltage (1~5V), I might need to find a power MOSFET with very small on-state resistance. Since the smallest resistance at load determined by MOSFET Ron and Rshunt, the smallest total resistance at load should smaller than 0.2 Ohm (because 1V/5A =0.2 Ohm) to pretend a short circuit. Therefore, if we use 0.05Ω shunt resistor, the room for Ron of MOSFET is 0.15Ω (150mΩ).

Requirement for electronic load changed to Vds = 1~5V & Id = 0~5A (Id ≥ 5A for short circuit requirement)

MOSFET model for LTspice can be found at https://my.centralsemi.com/content/engineering/spicemodels.

- N-channel MOSFET with high current: CXDM3069N 30V & 6.9A & 0.435Ω (Ron)

.model CXDM3069N NMOS(Level=1 Vto=1.40 Kp=0.259 Gamma=1.74 Phi=0.75 Lambda=2.08m Rd=60.9m Rs=60.9m Is=3.45p Pb=0.800 Mj=0.460 Cbd=2.96n Cbs=3.56n Cgso=564n Cgdo=470n Cgbo=4.77u)

The max power dissipation Pd = 1.2W

The power rating is not suitable (at least 30W), and Ron is too large.

- N-channel power MOSFET: CDM2206-800LR 800V & 6A & 0.8Ω (Ron)

The max power dissipation Pd = 110W

.model CDM2206-800LR NMOS (LEVEL=3 L=2.0000E-6 W=5.4000 KP=1.0356E-6 RS=10.000E-3 RD=.73326 VTO=3.5822 RDS=18.779E9 TOX=2.0000E-6 CGSO=56.380E-12 CGDO=4.3192E-12 CBD=4.6166E-9 MJ=1.2434 PB=3 RG=9.2692 RB=1.0000E-3 GAMMA=0 KAPPA=0)

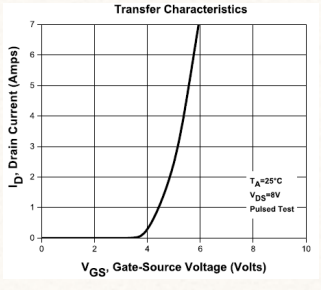
The Ron is too large, it cannot be used for short circuit.

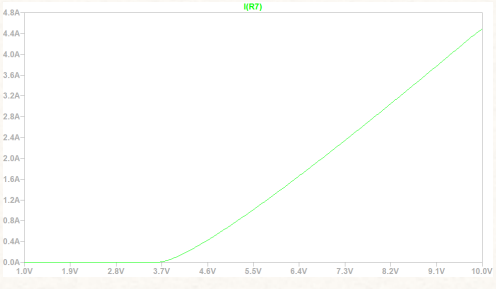
- N-channel power MOSFET: CDM7-700LR 700V & 7A & 0.48Ω (Ron)

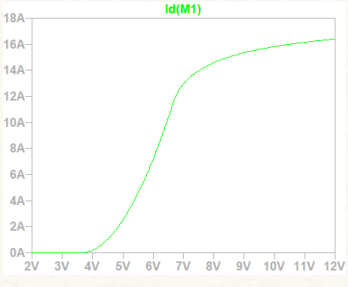
The max power dissipation Pd = 36W

.MODEL CDM7-700LR NMOS (LEVEL=3 L=2.0000E-6 W=5.1000 KP=1.0421E-6 RS=10.000E-3 RD=.42985 VTO=3.6039 RDS=11.667E9 TOX=2.0000E-6 CGSO=47.717E-12 CGDO=4.3175E-12 CBD=3.3036E-9 MJ=.82872 PB=3 RG=10.731 RB=1.0000E-3 GAMMA=0 KAPPA=0)

The Ron cannot be used for short circuit design. But it is good enough for resistance-variable load. (Used in LTspice simulation first)







LTspice simulation: The MOSFET characteristic curve from simulation does not match the data sheet.

CDM7-700LR - Id vs Vgs curve when Vds = 8V: At Vgs = 6V, Id should be around 7A but the simulation only shows 1.2A.

The spice model cannot correctly describe the MOSFET performance.

-> One way is to change parameters in the spice model in order to match data sheet performance.

Hard to find the correct number that suits the original parameters. Vds = 10~30V & Ron ≤ 0.48Ω (0.48Ω for Vgs = 10V & Id=3.5A)

-> Another way is to build a lower current version prototype of a electronic load. ✓

-> Or find another power MOSFET spice model, which is more accurate ✓ (if it can be found, it will be the best solution)

LTspice simulation mistake: Rshunt is set too big, affecting the MOSFET performance. Now remove Rshunt.

The MOSFET characteristic curve from simulation exactly matches the data sheet.

CDM7-700LR - Id vs Vgs curve when Vds =10V: At Vgs = 6V, Id is 7A.