Power Engineering Laboratory (MSc)

Buck Converter Lab – Dr. Paul Judge

Week 3

Welcome to the third week of the power electronics components of this module. As with week 2, this will involve a mixture of experimental work and simulation work using LTspice. You may wish to prioritise the experimental work during the allocated lab session and work on the LTSpice exercises in your own time outside of the lab.

Guidance on PowerPoint:

20% of the marks for the overall Buck Converter Lab are allocated to a PowerPoint which you will use to record your results. One joint PowerPoint should be submitted per group of students.

- The purpose of the PowerPoint is as an aid for you during the viva examination. It should be neatly presented and without massive amounts of text.
- You should also not use more than the number of slides allocated for each section in the PowerPoint.
- You should only include the results you think are the most interesting. I expect students to have varying results between groups and to not all have decided to include the same figures & graphs in each set of slides.
- In some of the later sections you will be asked to investigate a particular feature or phenomenon in the buck converter. In these sections it will be up to you as the student to decided what to include on the PowerPoint slides for these sections. You will get marks for things you discover and will not lose marks for missing things.
- Remember that during the viva you will be presenting your results on a laptop screen and not on a large projector – format your slides so that text and figures are readable under this format.

Load Regulation (30 Mins Target)

The LTC7800 chip operates the buck converter in a closed loop manor. The relevant pins to explore are **V_{FB}** and **ITH** and **Track/SS.** You should read the **'Main Control Loop'** of the datasheets, as well as the relevant description and application sections for each of these pins.

1. Investigate the ability of the converter to regulate the output voltage to a constant value as the output current varies from low currents to high currents. Do you observe any differences in the converter output voltage at light loads, medium loads, and heavy loads? **(2 Slides)**

Current Limiting (20 Mins Target)

The LTC7800 chip has a current limiting function built into it. The relevant pins to explore are **Sense+**, **Sense-** and **ILIM.**

1. Investigate how the current limiting function is programmed and set. How is this different between the PCB and what the datasheet suggests? **(1 Slide)**
2. Investigate what happens to the converter as the load resistance is made smaller and smaller. **(1 Slide)**
3. Investigate what happens when the output of the converter is suddenly short-circuited – you may wish to use the oscilloscopes single mode to capture this. **(1 Slide)**

Light Load Operation (45 Mins)

The LTC7800 chip has several different operation modes it can operate under during light loads. The operation mode is controlled by the **PLLIN/MODE** pin. This function does not fully work on the version of the board we have at the moment, however it is possible to use an LTSpice model of a different circuit layout to investigate it. An additional LTSpice model 'Figure11Circuit.asc' has been provided with this week's lab-book. This model is based on the circuit shown in Figure 11 of the LTC7800 datasheet.

1. Using LTSpice, investigate the different light load operation modes of the converter and how they impact the operation, efficiency and performance of the converter. **(4 Slides)**
2. Investigate what light load mode the PCB buck converter operates in. Can this be changed on the PCB? **(1 Slide)**.

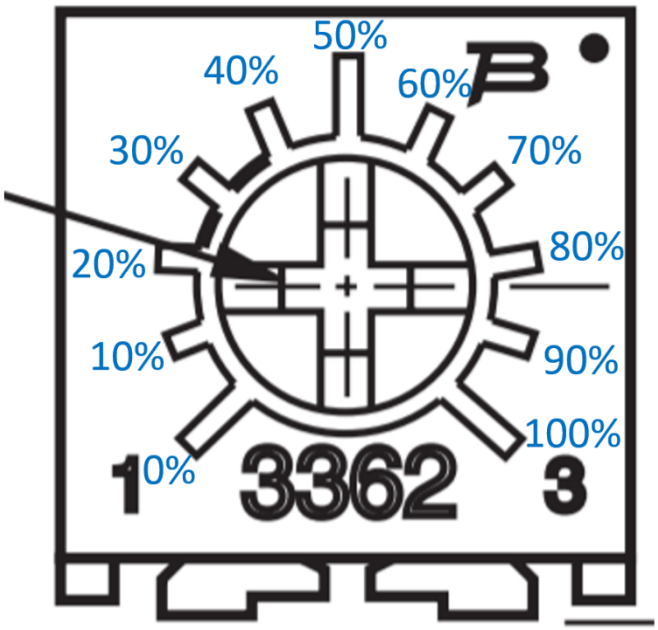
Impact of Feedback Controller Gain on Steady-State and Transient (60 Minutes Target Time)

The feedback gain of the LTC7800 main control loop can be adjusted using one of the potentiometers on the buck board. The main pin on the LTC7800 chip relating to this is the **ITH** pin, with the $\mathbf{V_{FB}}$ and **Track/SS** also playing roles in this overall control loop.

1. Investigate how the feedback gain can be adjusted on the PCB. **(1 Slide)**
2. Investigate how the feedback gain impacts the steady-state output voltage regulation of the board. **(1 Slide)**
3. Investigate how the feedback gain impacts the transient response of the converter. **(3 Slides)**
4. Investigate how the output capacitor size impacts the transient response of the converter. **(2 Slides)**
5. Investigate using the fan bank as a load. How does this compare to a resistive load under both steady-state and transient conditions? **(2 Slides)**

For transient responses you have the option of either using a step in the output voltage reference, or to use a step in the load resistance. A step in the load resistance can be achieved by using two of the load potentiometers and suddenly either connecting or disconnecting one of the two load resistors from the output of the buck converter. Ask a T&D for help if you are unsure.

Note: For the last section you may wish to be able to record the resistance of the potentiometer that sets the feedback gain. You can get an approximate value for this using the markers on the potentiometer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