JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

Homework 10

Assigned: November 28, 2019

Due: December 5, 2019, 4:00pm.

The homework should be submitted in hard copies.

1. Problem 5.25 (20 points)

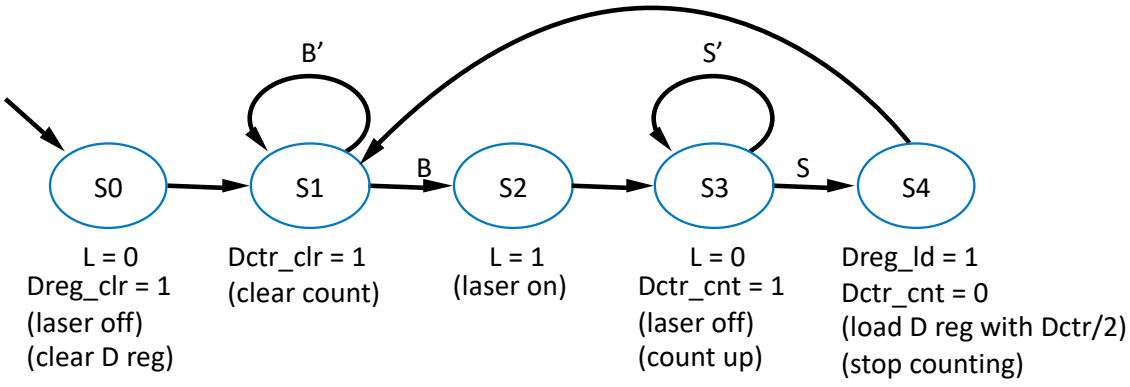
(a) Assume the 8-bit carry-ripple adder consists of 8 full-adders chained together. Each full-adder features a critical path delay of 4ns (an AND gate and a XOR gate). Thus, the total critical path delay for the 8-bit carry-ripple adder is 8*4ns = 32ns.

(b) Each full-adder's critical path features one internal wire between an AND and XOR gate and two wires that connect the full-adder's inputs and outputs. For the entire 8-bit carry-ripple adder, the 8 internal wires contribute 8ns to the critical path delay. Wires connecting full-adders together contribute 7ns to the critical path delay.

The initial ci and final co contribute 2ns to the critical path delay. Thus, the total critical path delay is 32ns (for gates) + 8ns + 7ns + 2ns = 49ns.

2. Problem 5.26 (30 points)

Inputs: B, S Outputs: L, Dreg_clr, Dreg_ld, Dctr_clr, Dctr_cnt



(a)

Inputs					Outputs							
s2	s1	s0	B	S	n2	n1	n0	L	Dreg_clr	Dreg_ld	Dctr_clr	Dctr_cnt
0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	1	0	0	1	0	1	0	0	0
0	0	0	1	0	0	0	1	0	1	0	0	0
0	0	0	1	1	0	0	1	0	1	0	0	0
0	0	1	0	0	0	0	1	0	0	0	1	0
0	0	1	0	1	0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0
0	0	1	1	1	0	1	0	0	0	0	1	0
0	1	0	0	0	0	1	1	1	0	0	0	0
0	1	0	0	1	0	1	1	1	0	0	0	0
0	1	0	1	0	0	1	1	1	0	0	0	0
0	1	0	1	1	0	1	1	1	0	0	0	0
0	1	1	0	0	0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	0	0	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0	0	1
0	1	1	1	1	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	0	0	1	0	0
1	0	0	0	1	0	0	1	0	0	1	0	0
1	0	0	1	0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	0	1	0	0	1	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0

n2 = s1's1s0B'S + s2's1s0BS

n1 = s2's1's0B + s2's1s0' + s2's1s0S'

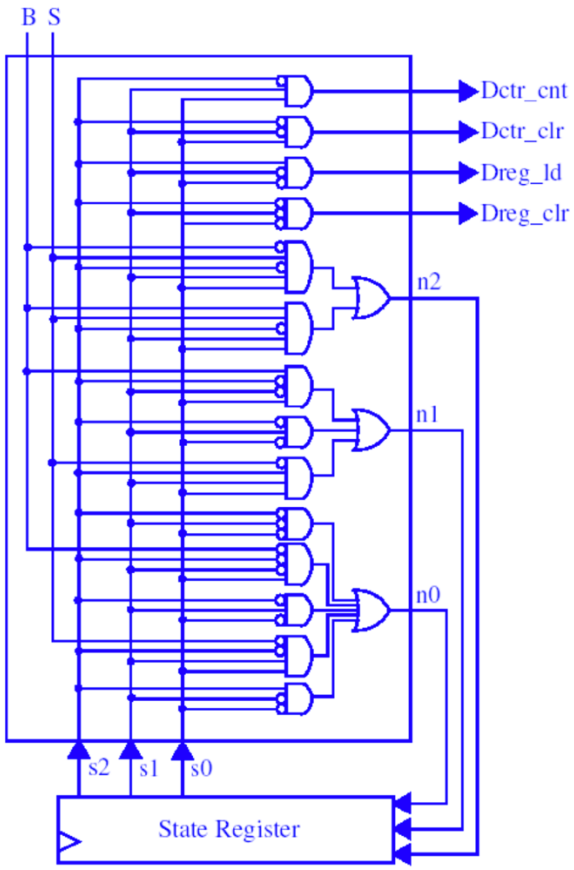
n0 = s2's1's0' + s2's1's0B' + s2's1s0' + s2's1s0S' + s2s1's0'

Dreg_clr = s2's1's0'

Dreg_ld = s2s1's0'

Dctr_clr = s2's1's0

Dctr_ctr = s2's1s0



(b) The controller features two levels of gates, resulting in a delay of 4ns. Therefore the critical path is within the up-counter, or 5ns.

(c) With a critical path of 5ns, the maximum clock frequency is 1,000,000,000/5 = 200MHz.

3. Given that an SRAM block has a 32-bit address input, each line of the memory has an address, how many lines does the memory have? (5 points)

   The SRAM block has 2^{32} lines

   If each line is a 32-bit word, how many bytes (8 bits) does the memory have? (2 points)

   It has $2^{32} * 4 = 2^{34}$ bytes

   In that case, how many transistors does the memory have for storage? (3 points)

   Each bit is stored in one SRAM cell which requires 6 transistors.

   2^{34} bytes = $2^{34} * 8$ bits = 2^{37} bits

   Number of transistors = $2^{37} * 6$

   If we use a decoder to decode the address, how big a decoder will be needed (e.g. a 3x8 decoder)? (2 points)

   32 x 2^{32} decoder

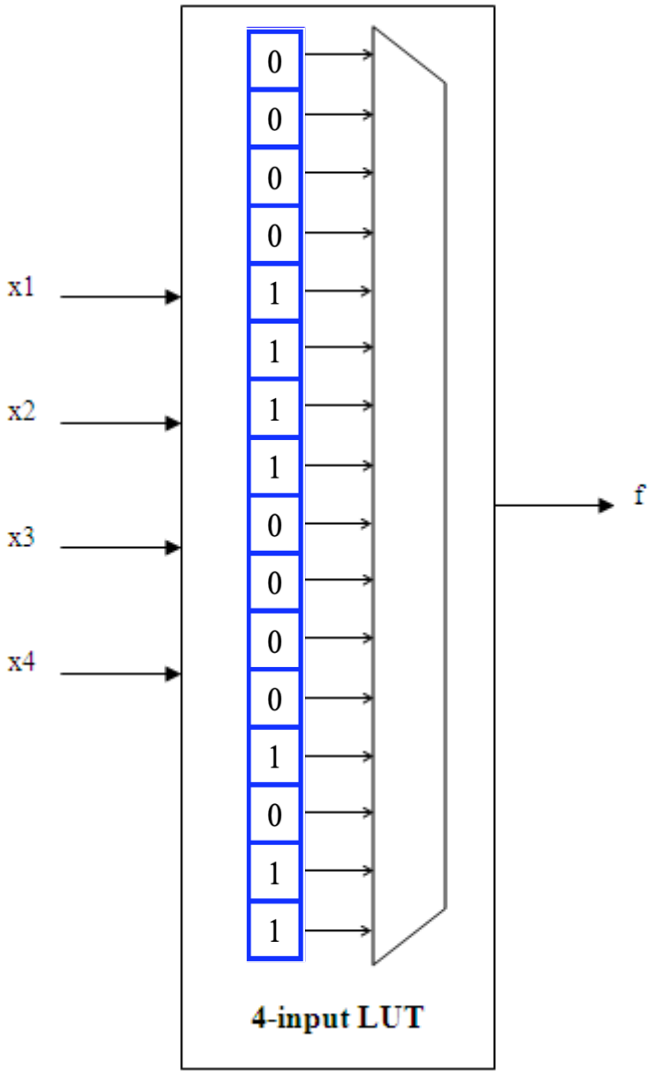
If the memory is byte addressable, i.e. each byte has an address, how many bits does the memory have? (3 points)

With 32 bits of address, we have 2^{32} addresses. If the addresses are for bytes, then we have 2^{32} bytes. Then number of bits = 2^{32} * 8 bits = 2^{35} bits.

4. Use one 4-input LUT to implement the following Boolean function (15 points)

f = x2x3'x4' + x1'x2x4 + x1'x2x3 + x1x2x3

x1	x2	x3	x4	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1



5. Problem 7.20 (20 points)