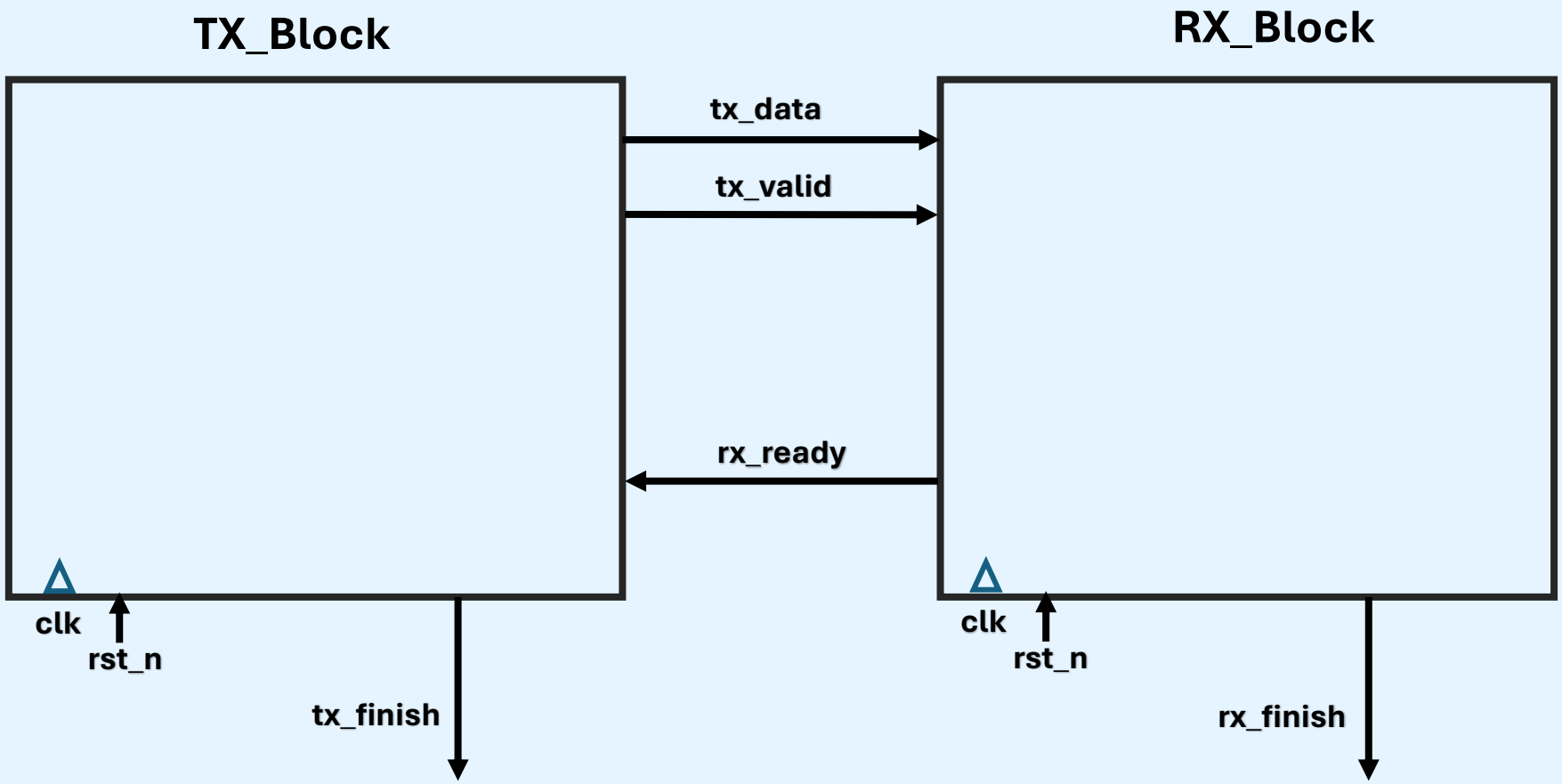
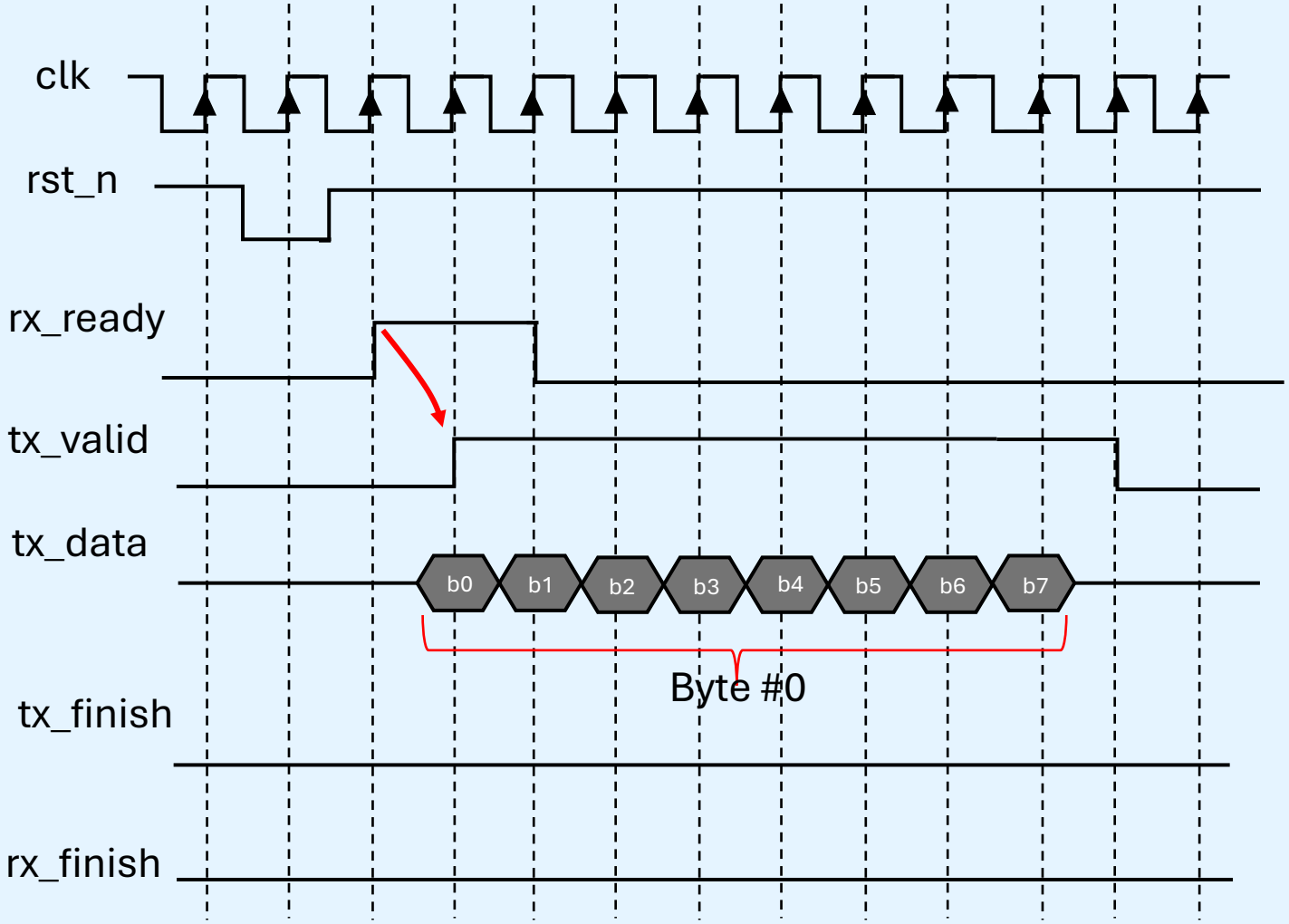
Project

Serial Communication



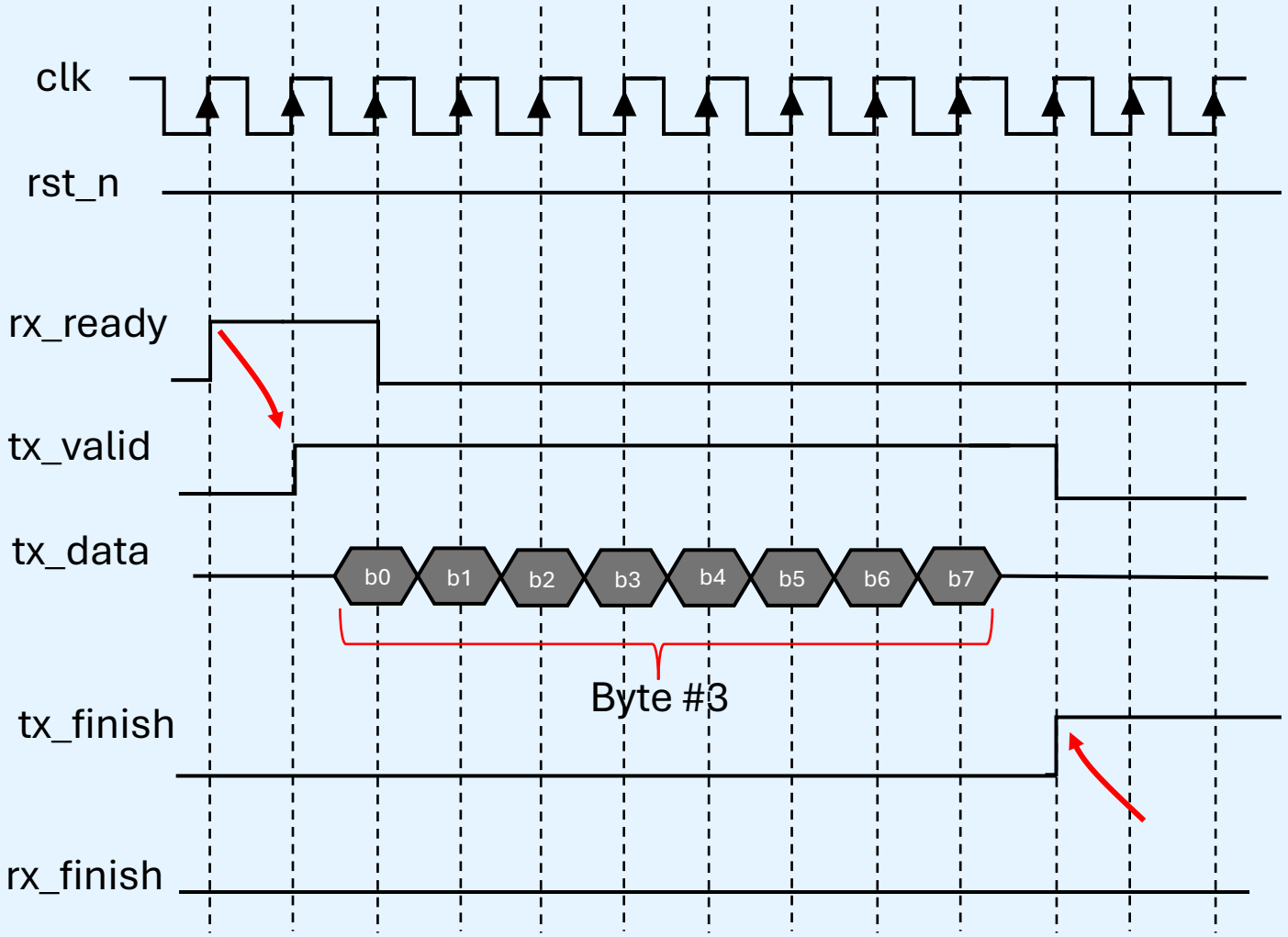
Project

Waveform



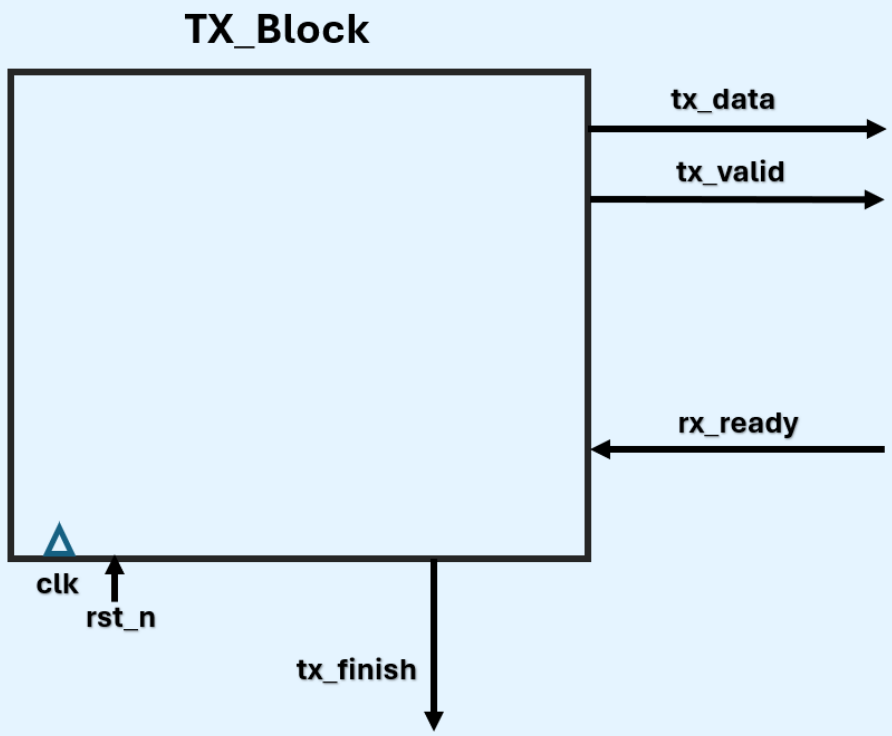
Project

Waveform



TX Block

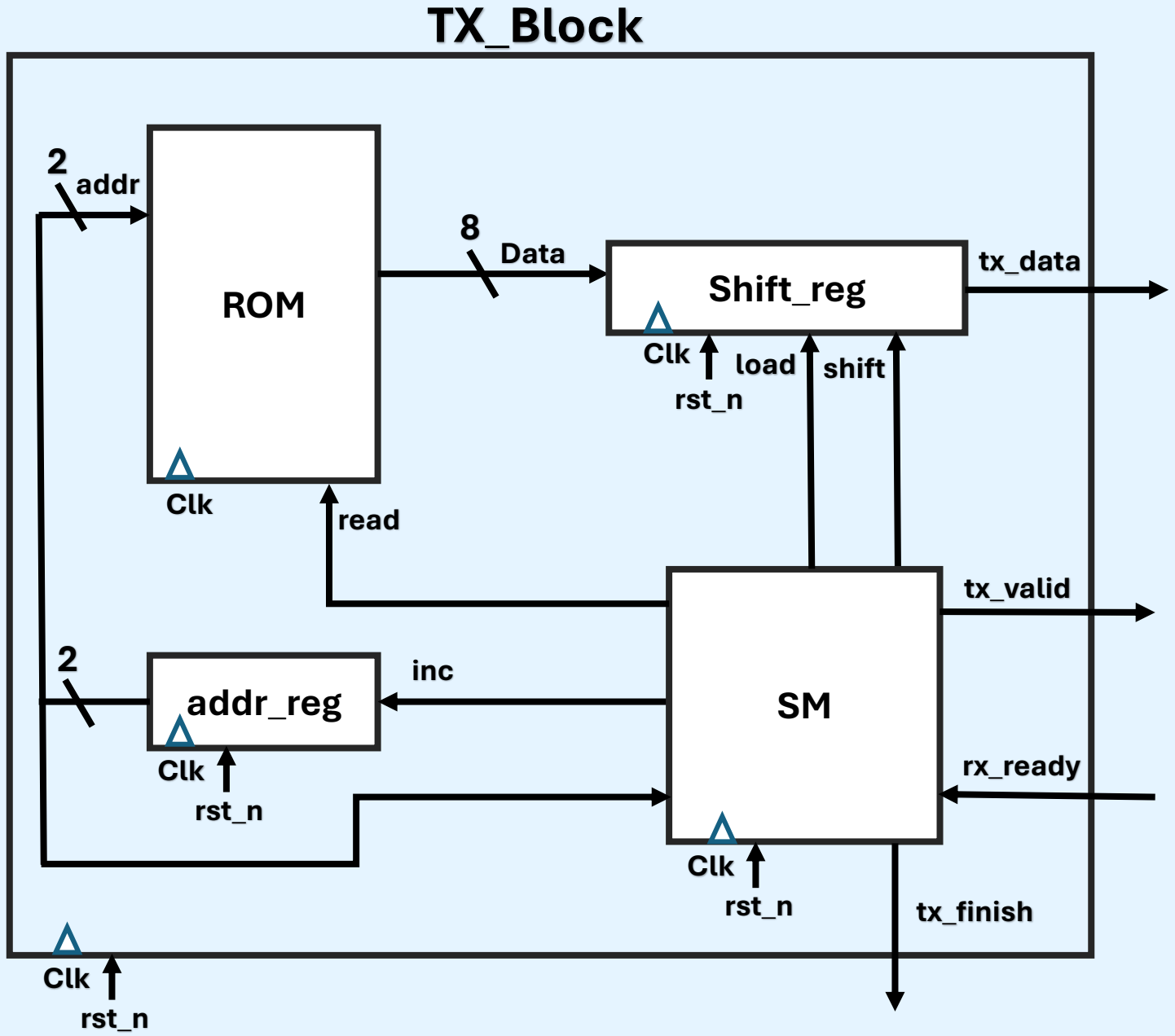
I/O definition



name	I/O	Description
clk	I	50MHz
rst_n	I	active-low
rx_ready	I	Rx block is ready to receive data
tx_valid	O	Data on the tx_data wire is valid
tx_data	O	Serial data
tx_finish	O	All data is sent

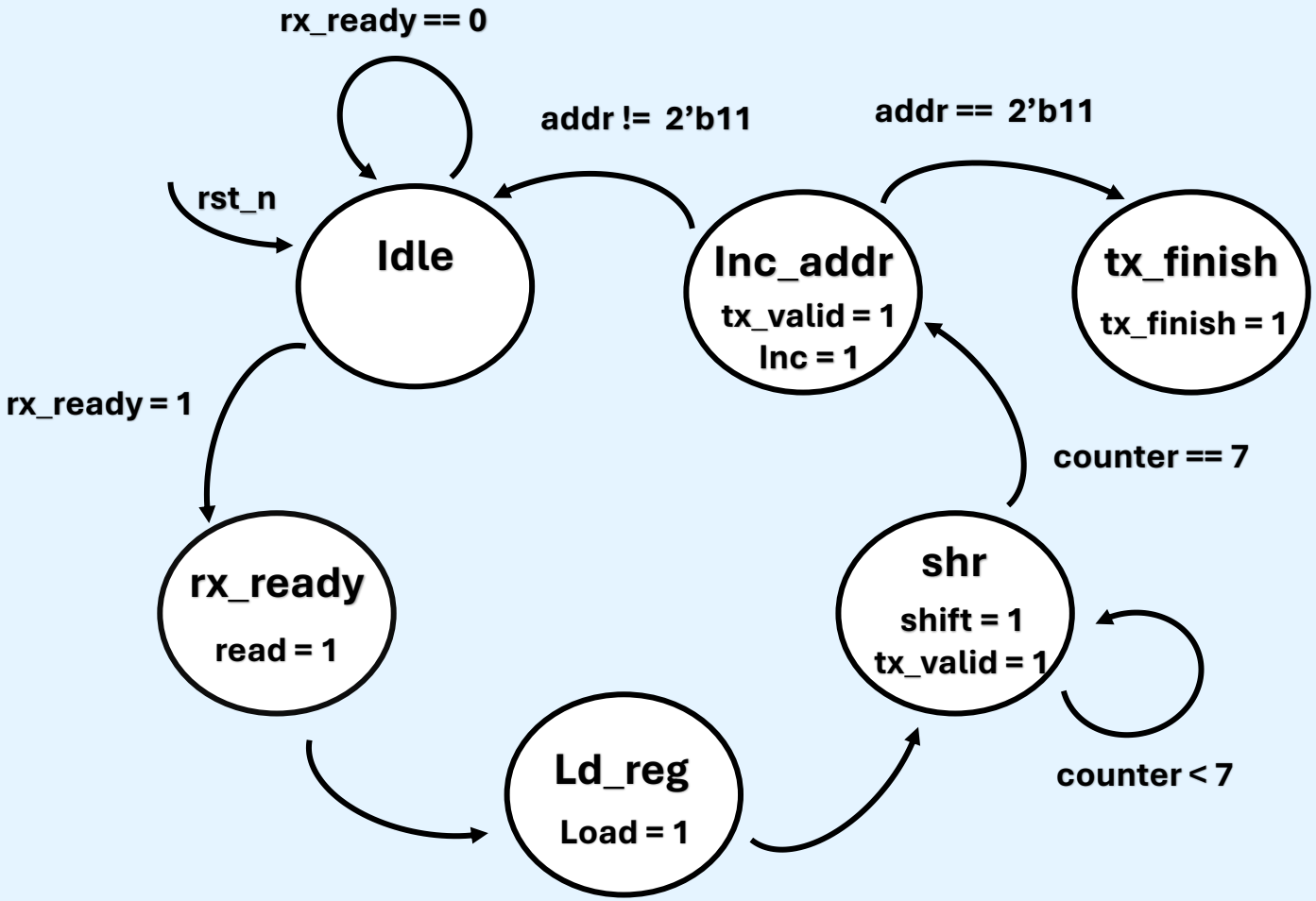
TX Block

Architecture



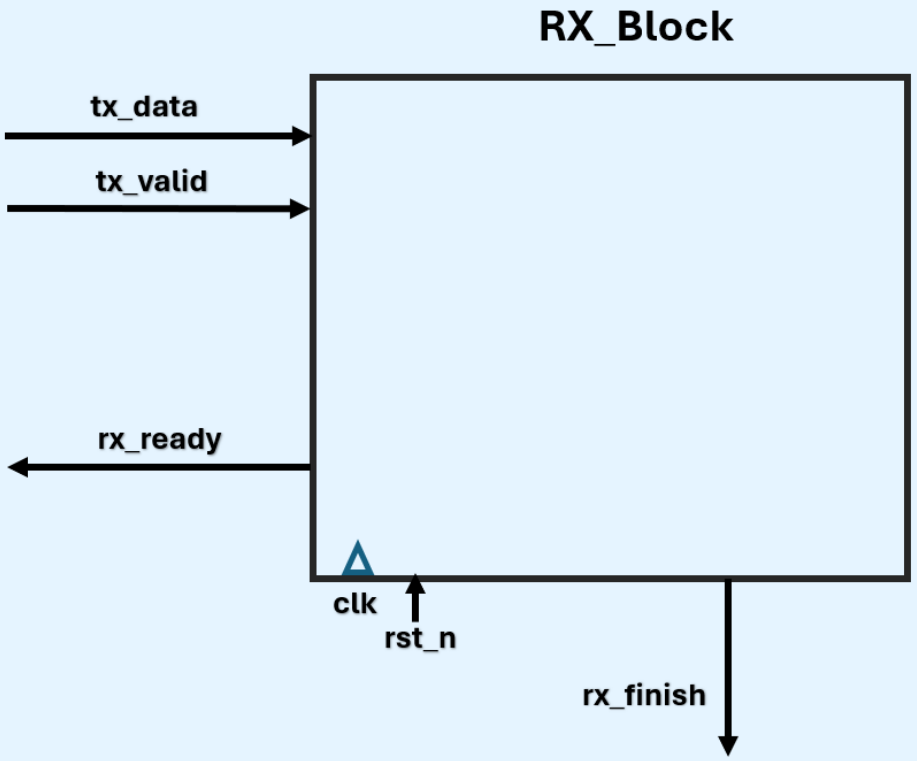
TX Block

State Machine



RX Block

I/O definition



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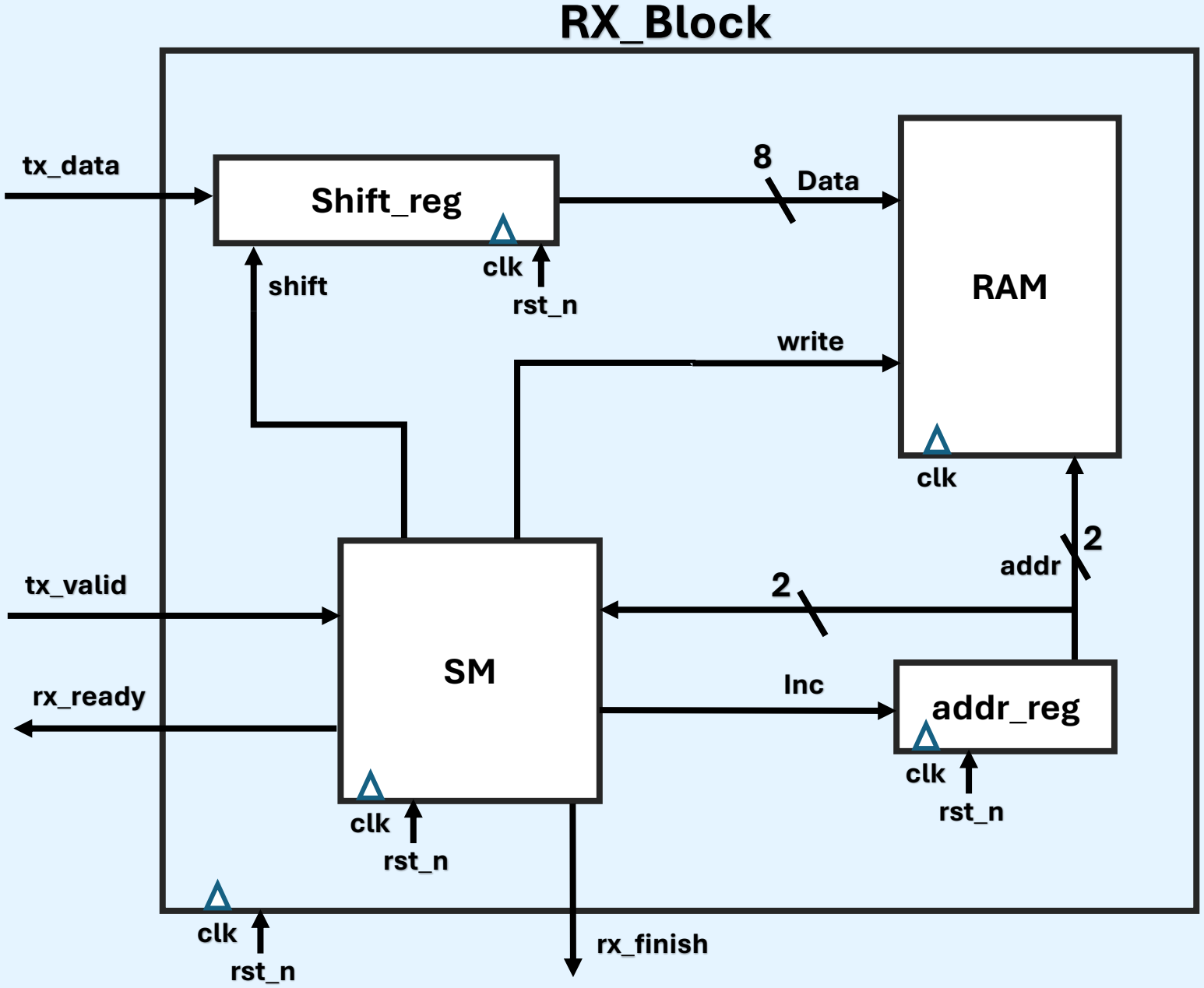
RX Block

Architecture



RX Block

State Machine