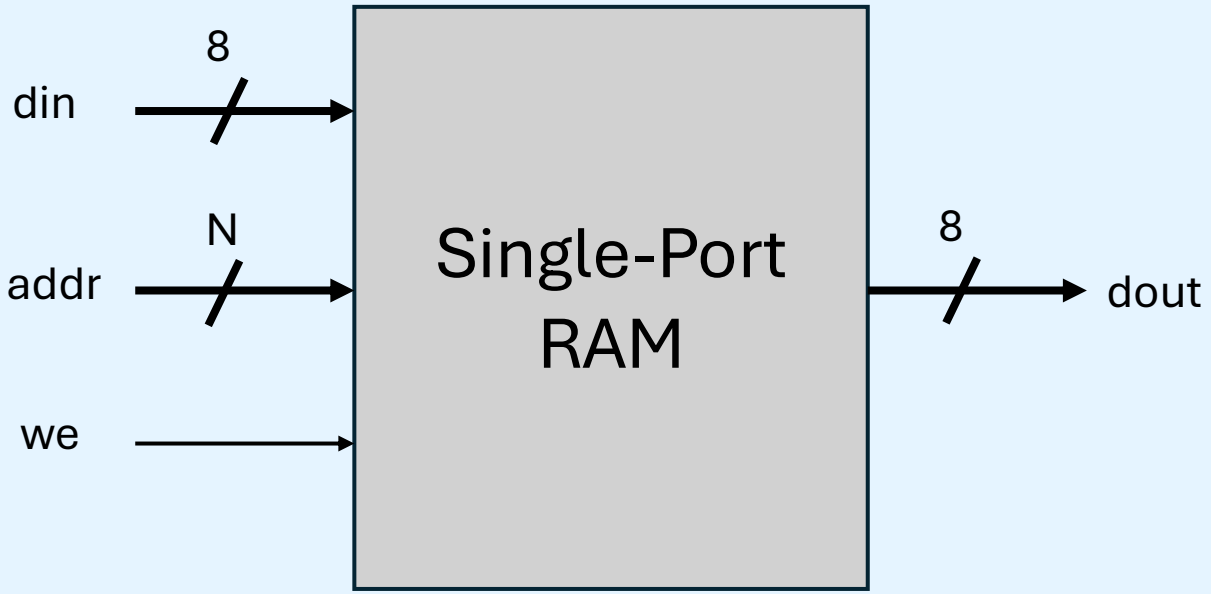
Single-Port RAM

Spec



Elements	Values
Data Width	8 bit
Depth	16
Address Width	Log2(16) = 4

Signal	Values
clk	Input
we (wire enable)	Input
addr	Input
din	Input
dout	output