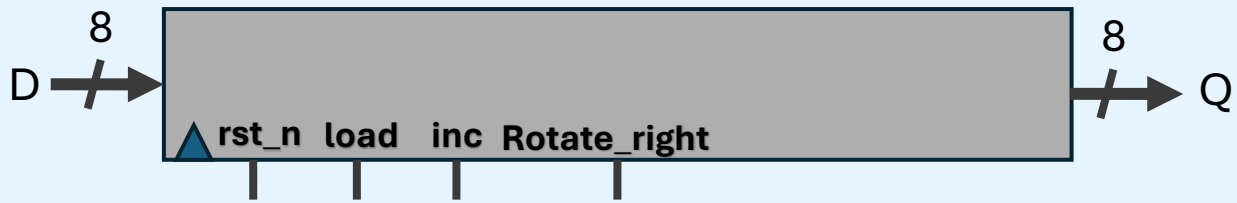
Register

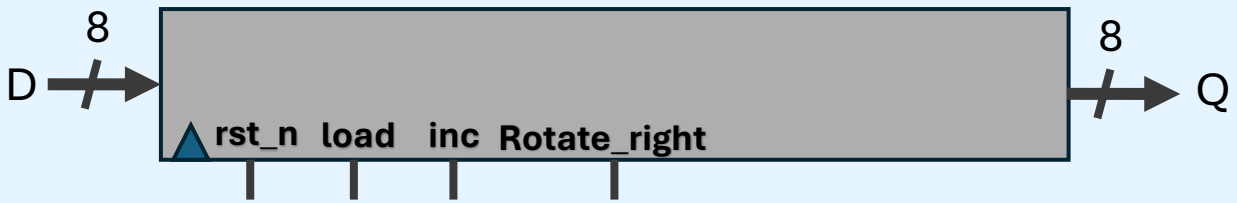
Spec



Name	Direction	Width	Description
clk	Input	1 bit	Clock signal (rising edge triggered)
reset_n	Input	1 bit	Active-low asynchronous reset
load	Input	1 bit	Load enable signal
inc	Input	1 bit	Increment enable signal
rotate_right	Input	1 bit	Rotate-right enable signal
D	Input	8 bits	Input data for load
Q	Output	8 bits	Current value of the register

Register

Functional Behavior



- The register is triggered on the **rising edge of clk**, unless **asynchronously reset**.
- The register supports **four main operations with the following Priority** (highest to lowest):
  1. **Asynchronous reset** (if reset_n == 0) → Clear Q to 8'b0
  2. **Load** (load == 1) → Load data from input D to output Q
  3. **Increment** (inc == 1) → Increment Q by 1
  4. **Rotate Right** (rotate_right == 1) → Circular right shift of Q by 1 bit
- NOTE: If No control active → Hold previous value Only