USB 3.1 ENGINEERING CHANGE NOTICE FORM

Title: Rx JTOL RJ Correction
Applied to: USB 3.1 Specification Release

Brief description of the functional changes:
Correction to the input RJ requirements specified for receiver jitter tolerance testing. The RMS RJ was changed from a value of 0.01308UI to a value of 0.0100UI by “USB 3.1 ECN SSP System Jitter Budget.pdf”. However, this updated RJ value was overlooked when submitting the ECR which modified the reference CTLE and transmit equalization requirements (published as “USB 3.1 ECN CTLE.pdf”). The transmitted RJ spec for SS gen 2 operation defined in Table 6-27 of the CTLE ECN inadvertently had the old spec value of 0.01308UI and not the new value of 0.01UI. This ECR corrects the error.

Benefits as a result of the changes:
Give designers and testers the correct information for testing jitter tolerance of Gen 2 receivers.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
No impact.

An analysis of the hardware implications:
Minimizes risk of designing or testing receivers to the wrong input RJ value.

An analysis of the software implications:
No impact.

An analysis of the compliance testing implications:
Ensures we test with the correct inputs.

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Actual Change

(a) From Text (and location): In section 6.8.2.2.1, table 6-25, page 6-37

Symbol	Parameter	Gen 1 (5GT/s)	Gen 2 (10GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.01308	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.184	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	0.8	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Preshoot=2.2 De-emphasis= -3.1	dB	1

Notes:

1. All parameters measured at TP1. The test point is shown in **Error! Reference source not found.**.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in **Error! Reference source not found.**.
5. The JTOL specs for Gen 2 comprehend jitter peaking with re-timers in the system and has a 25dB/decade slope.

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