USB Type-C ENGINEERING CHANGE NOTICE

Title: USB Type-C ECR on the SRC-to-TrySRC looping
Applied to: USB Type-C Specification Release 1.1, April 3, 2015

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Brief description of the functional changes:

If a Type-C Source has a long tVBUSoff delay, the Source may not connect with a Try.SRC machine.

First, when Source outputs the VBUS (1) and Try.SRC DRP will enter Try.SRC (2). As Rd of Try.SRC DRP is removed, Source enters Unattached.SRC (3). After tDRPTry, no connection can be made and Try.SRC DRP enters TryWait.SNK (4) and Source enters AttachWait.SRC (5).

If the residue voltage of VBUS from (1) is still not fully discharged, Try.SRC DRP will enter Attached.SNK (6) but Source cannot enter Attached.SRC as Vsafe0V is required. After VBUS is further discharged, Try.SRC DRP will enter unattached.SNK (7) & AttachedWait.SNK (8) and Source will finally enter Attached.SRC (7*) and start to output VBUS again. Try.SRC DRP returns to Try.SRC (9).

The two machines return to the original (1) and (2) states. And loop forever.

Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support

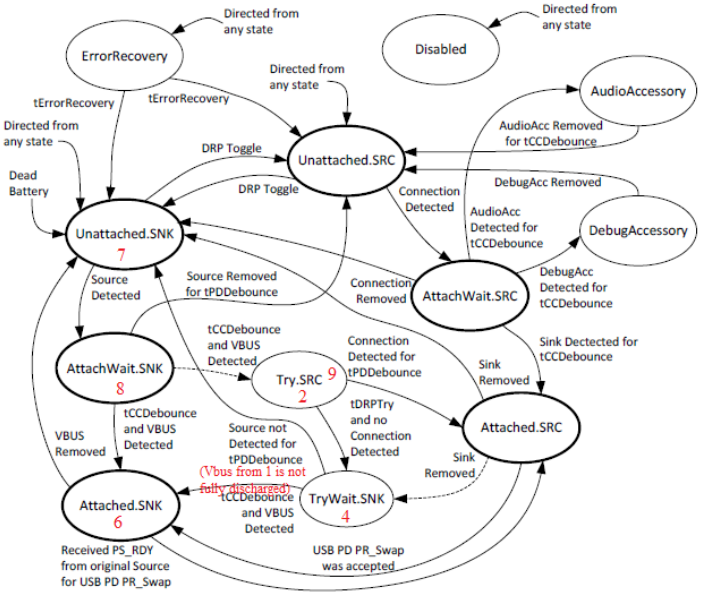
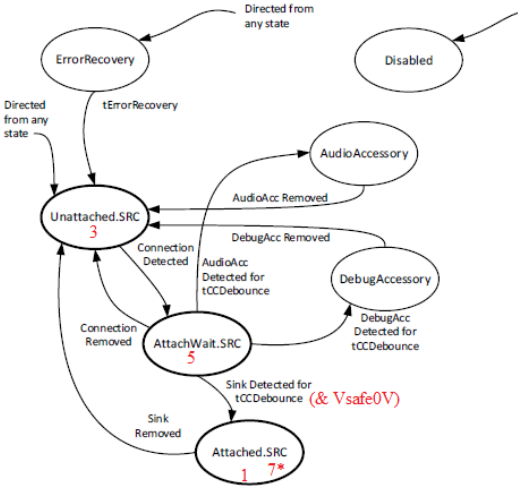


Figure 4-12 Connection State Diagram: Source



As a DRP will always leave Attached.SNK if VBUS is removed without any delay, it is necessary to ensure that the DRP entering Attached.SNK is due to VBUS supplied by the Source but not the discharging residue voltage in capacitor. A condition can be added to ensure VBUS is fully discharged once, and the detected VBUS (to enter Attached.SNK) is supplied by Attached.SRC.

The last line in 4.5.2.2.9.2 could change from:

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected.

to:

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected and VBUS is within vSafe0V, or after tTryTimeout and the SRC.Rd state has not been detected.

And Table 4-19 in 4.11.2 could change from:

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
dcSRC.DRP	30%	70%	The percent of time that a DRP shall advertise Source during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between Source and Sink roles during role resolution
tDRPTry	75 ms	150 ms	Wait time associated with the Try.SRC state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the TryWait.SNK state

to:

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
dcSRC.DRP	30%	70%	The percent of time that a DRP shall advertise Source during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between Source and Sink roles during role resolution
tDRPTry	75 ms	150 ms	Wait time associated with the Try.SRC state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the TryWait.SNK state
tTryTimeout	550ms	1100ms	Timeout for transition from Try.SRC to TryWait.SNK

One exception is legacy hosts or captive chargers (a A-to-C cable with VBUS always available) and it is the reason for the tTryTimeout timeout needed.

The additional delay of tTryTimeout here Plus the delay of tCCDebounce from TryWait.SNK to Attached.SNK can also ensure the residue VBUS fully discharged anyway. 550msec, min(tTryTimeout) + 100msec, min(tCCDebounce) > = 650msec, max(tVbusoff). The max value of tTryTimeout is set to double of min value as other timing parameters.

Benefits as a result of the changes:

It can solve the looping problem due to the slowly discharged VBUS.

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An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Try.SRC DRP state machine will take longer to connect to legacy hosts or captive chargers.

An analysis of the hardware implications:
Does not add additional BOM cost. If the PD Controller in a Source is firmware-based, a firmware update could possibly add this Vsafe0V checking and timeout. If the CC Logic controller is hardware-based and therefore unable to be updated, then it must be replaced.

An analysis of the software implications:
None.

An analysis of the compliance testing implications:
Compliance testing needs to validate this requirement.

Actual Change

(a). The last line in 4.5.2.2.9.2
changes from:

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected.

to:

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected and VBUS is within vSafe0V, or after tTryTimeout and the SRC.Rd state has not been detected.

(b). Table 4-19 in 4.11.2
change from:

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
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to:

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
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tTryTimeout	550ms	1100ms	Timeout for transition from Try.SRC to TryWait.SNK