USB 3.1 ENGINEERING CHANGE NOTICE FORM

Title: PHY 022 Link Configuration Bit
Applied to: USB Specification Version 3.1

Brief description of the functional changes:
Defines bit 5 of the link configuration symbol as the bit-level retimer transmit compliance bit. When this bit is asserted , a bit-level retimer is placed into transmit compliance mode, which is defined in Appendix E. ECR also adds a note to clarify the behavior of a retimer when bit 2 of the link configuration symbol is set.

Benefits as a result of the changes:
This capability enables compliance testing of bit-level retimers in which the clock that is used to transmit the compliance pattern is derived from a jittered input signal at the retimer receiver input. The retimer will locally generate the compliance pattern. In order to do this, the retimer must first progress through the training state machine (which is not done for compliance mode entry for hosts, devices, dual role devices and SRIS retimers).

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
No impact.

An analysis of the hardware implications:
No impact.

An analysis of the software implications:
No impact.

An analysis of the compliance testing implications:
New electrical compliance test procedures are required for bit-level retimers. Note that this is true irrespective of this ECR. The ECR simply gives a way to do a meaningful transmit compliance test on a bit-level retimer.

Actual Change

Section 6.4.1.1.3, Figure 6-5
From Text:

Table Error! No text of specified style in document.**-1. Gen 1/Gen 2 Link Configuration**

Field	TS1 Symbol 5	Description
Bit 0	0 = Normal Training 1 = Reset	Reset is set by the Host only in order to reset the device.
Bit 1	Set to 0	Reserved for future use.
Bit 2	0 = Loopback de-asserted 1 = Loopback asserted	When set, the receiving component enters digital loopback.
Bit 3	0 = Disable Scrambling de-asserted 1 = Disable Scrambling asserted	When set, the receiving component disables scrambling. When this is asserted during Gen 2 operation the training Ordered Sets are still scrambled and the disabling of scrambling begins with the first Data Block after the SDS.
Bit 4	0 = Local loopback in repeater de-asserted 1 = Local loopback in repeater asserted	When set, the nearest repeater in the link is placed into local loopback mode.
Bit 5:7	Set to 0	Reserved for future use.

To Text:

Table Error! No text of specified style in document.**-2. Gen 1/Gen 2 Link Configuration**

Field	TS1 Symbol 5	Description
Bit 0	0 = Normal Training 1 = Reset	Reset is set by the Host only in order to reset the device.
Bit 1	Set to 0	Reserved for future use.
Bit 2	0 = Loopback de-asserted 1 = Loopback asserted	When set, the receiving component enters digital loopback. A SRIS retimer shall be placed in Pass Through Loopback. A bit-level retimer shall be placed in Pass Through Loopback if bit 5 is not asserted.
Bit 3	0 = Disable Scrambling de-asserted 1 = Disable Scrambling asserted	When set, the receiving component disables scrambling. When this is asserted during Gen 2 operation the training Ordered Sets are still scrambled and the disabling of scrambling begins with the first Data Block after the SDS.
Bit 4	0 = Local loopback in repeater de-asserted 1 = Local loopback in repeater asserted	When set, the nearest repeater in the link is placed into local loopback mode.
Bit 5	0 = Bit-level retimer Tx compliance mode de-asserted 1 = Bit-level retimer Tx compliance mode asserted	When set, bit-2 shall also be set. a bit-level retimer is placed into transmit compliance mode defined in Appendix E. All other components (hosts, devices, dual role devices, non-bit-level retimers) ignore this bit.
Bit 6:7	Set to 0	Reserved for future use.