USB 3.1 ENGINEERING CHANGE NOTICE FORM

Title: PM Timers
Applied to: USB_3_1r1.0_07_31_2013

Brief description of the functional changes:

To clarify how PM_LC_Timer/PM_Entry_Timer starts and stops to avoid ambiguity and to increase the PM_LC_Timer/PM_Entry_Timer value to address the corner case where a device may issue LGO_Ux and the host happens to start an out transfer with a DP of max DPP.

Benefits as a result of the changes:

1. To enforce compliance test on PM_LC_TIMER/PM_ENTRY_TIMER with no implementation ambiguity
2. To relax the timeout value addressing the corner case when re-timer/cable delays are accounted. The change is to maximize PM_LC_Timer to minimize the corner case of host DP blocking LAU. Max PM_LC_Timer value is bounded by PM_Entry_Timer (6us). the relaxed 1-us is to accommodate for 4 re-timers with 50m cable, which compared to 3-retimer configuration, is to accommodate an additional 600-ns round-trip delay by the 4th retimer (50ns x2) and extended cable length (250ns x2).
3. To support explicit link delay timing budget by defining timing requirement for LGO_Ux processing delay.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

1. No impact to USB 3.0 ecosystem.
2. No impact to any early USB3.1 implementation.

An analysis of the hardware implications:

Any new USB 3.1 implementation complies with the Pending_HP_Timer ECN will need to comply with this ECN.

An analysis of the software implications:

None

An analysis of the compliance testing implications:

Will need to be updated

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Actual Change

(a). From Text (and location): Section 7.2.4.2.1

7.2.4.2.1 Power Management Link Timers

A port shall have three timers for link power management. First, a PM_LC_TIMER is used for a port initiating an entry request to a low power link state. It is designed to ensure a prompt entry to a low power link state. Second, a PM_ENTRY_TIMER is used for a port accepting the entry request to a low power link state. It is designed to ensure that both ports across the link are in the same low power link state regardless if the LAU or LPMA is lost or corrupted. Finally, a Ux_EXIT_TIMER is used for a port to initiate the exit from U1 or U2. It is specified to ensure that the duration of U1 or U2 exit is bounded and the latency of a header packet transmission is not compromised. The timeout values of the three timers are specified in Table 7-8.
A port shall operate the PM_LC_TIMER based on the following rules:

- A port requesting a low power link state entry shall start the PM_LC_TIMER after the last symbol of the LGO_Ux link command is sent.
- A port requesting a low power link state entry shall disable and reset the PM_LC_TIMER upon receipt of the LAU or LXU.

A port shall operate the PM_ENTRY_TIMER based on the following rules:

- A port accepting the request to enter a low power link state shall start the PM_ENTRY_TIMER after the last symbol of the LAU is sent.
- A port accepting the request to enter a low power link state shall disable and reset the PM_ENTRY_TIMER upon receipt of an LPMA or a TS1 ordered set.

(a). To Text (and location): Section 7.2.4.2.1

7.2.4.2.1 Power Management Link Timers

A port shall have three timers for link power management. First, a PM_LC_TIMER is used for a port initiating an entry request to a low power link state. It is designed to ensure a prompt entry to a low power link state. Second, a PM_ENTRY_TIMER is used for a port accepting the entry request to a low power link state. It is designed to ensure that both ports across the link are in the same low power link state regardless if the LAU or LPMA is lost or corrupted. Finally, a Ux_EXIT_TIMER is used for a port to initiate the exit from U1 or U2. It is specified to ensure that the duration of U1 or U2 exit is bounded and the latency of a header packet transmission is not compromised. The timeout values of the three timers are specified in Table 7-8.
A port shall operate the PM_LC_TIMER based on the following rules:

- A port requesting a low power link state entry shall start the PM_LC_TIMER after the last symbol of the LGO_Ux link command is sent.
- A port requesting a low power link state entry shall disable and reset PM_LC_TIMER upon receipt of the last symbol of LAU or LXU at its receiver.

A port shall operate the PM_ENTRY_TIMER based on the following rules:

- A port accepting the request to enter a low power link state shall start PM_ENTRY_TIMER after the last symbol of LAU is sent.
- A port accepting the request to enter a low power link state shall disable and reset PM_ENTRY_TIMER upon receipt of the last symbol of LPMA or detection of a TS1 ordered set at its receiver.

(b). From Text (and location): Table 7-8

Table 7-8. Link Flow Control Timers Summary

Timers	Timeout Value (µs)
PM_LC_TIMER	3
PM_ENTRY_TIMER	6
Ux_EXIT_TIMER	6000

(b). To Text (and location): Table 7-8

Table 7-8. Link Flow Control Timers Summary

Timers	Timeout Value (µs)
PM_LC_TIMER	4
PM_ENTRY_TIMER	8
Ux_EXIT_TIMER	6000

(c). From Text (and location): Section 7.5.6.1

7.5.6.1 U0 Requirements

- The port shall meet the transmitter specifications defined in Table 6-17.
- The port shall maintain the low-impedance receiver termination (R_{RX-DC}) defined in Table 6-21.
- The LFPS receiver shall be enabled.
- The port shall enable a 1-ms timer (tU0RecoveryTimeout) to measure the time interval between two consecutive link commands. This timer will be reset and restarted every time a link command is received.
- The port shall enable a 10-µs timer (tU0LTimeout). This timer shall be reset when the first symbol of any link command or packet is sent and restarted after the last symbol of any link command or packet is sent. This timer shall be active when the link is in logical idle.
- A downstream port shall transmit a single LDN when the 10-µs timer (tU0LTimeout) expires.
- An upstream port shall transmit a single LUP when the 10-µs timer (tU0LTimeout) expires.

(c). To Text (and location): Section 7.5.6.1

7.5.6.1 U0 Requirements

- The port shall meet the transmitter specifications defined in Table 6-17.
- The port shall maintain the low-impedance receiver termination (R_{RX-DC}) defined in Table 6-21.
- The LFPS receiver shall be enabled.
- The port shall enable a 1-ms timer (tU0RecoveryTimeout) to measure the time interval between two consecutive link commands. This timer will be reset and restarted every time a link command is received.
- The port shall enable a 10-µs timer (tU0LTimeout). This timer shall be reset when the first symbol of any link command or packet is sent and restarted after the last symbol of any link command or packet is sent. This timer shall be active when the link is in logical idle.
- A downstream port shall transmit a single LDN when the 10-µs timer (tU0LTimeout) expires.
- An upstream port shall transmit a single LUP when the 10-µs timer (tU0LTimeout) expires.
- A port shall acknowledge the received header packet with either LGOOD_n or LBAD within the HP response time (tDHPResponse). This is measured at a port's connector from when the first bit

of HP is received to when the first bit of either LGOOD_n or LBAD is transmitted. If a retimer is used with the port receiving HP, the HP response time shall account for the additional delay of the retimer.

- In SuperSpeed operation, tDHPResponse shall be less than 2540-ns.
- In SuperSpeedPlus operation, tDHPResponse shall be less than 1610-ns.

Note that tDHPResponse includes some worst case delay, tDPacket=2140-ns in SuperSpeed and tDPacket=910-ns in SuperSpeedPlus, when additional packets are scheduled ahead of the corresponding LGOOD_n or LBAD. It is recommended that a design respond with LGOOD_n or LBAD within 400-ns in SuperSpeed operation or 700-ns in SuperSpeedPlus operation when no packets delay the LGOOD_n or LBAD transmission. Refer to Figure E-5 of Section E.1.2.3 for details.

- A port shall acknowledge the received LGO_Ux with LAU or LXU based on the timing defined by tDHPResponse.