



**UNSE**

Universidad Nacional  
de Santiago del Estero



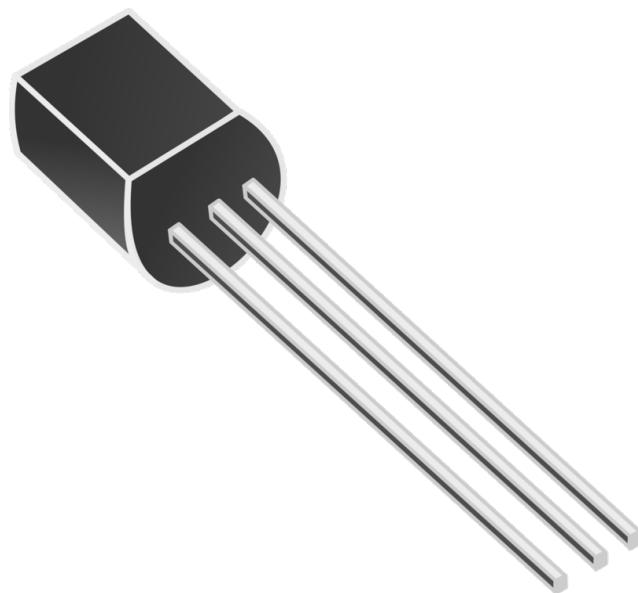
Facultad de Ciencias  
Exactas y Tecnologías

*Santiago del Estero, 19 de mayo del 2025*

*Ingeniería eléctrica*

### **TP N° 6: Cascaded Amplifier**

**Electronica II**



#### **DOCENTES:**

- Ing. Mario Gomez
- Ing. Lucas Moscatelli

#### **ALUMNO**

- Chevauchey Clément

## INDEX

Objetives	3
Introduction	3
Cascaded amplifiers	3
Materials used	3
Development	2
Selection of transistors	2
Stage 1: First common-emitter amplifier (CE1)	3
Stage 2: Second common-emitter amplifier (CE2)	4
Stage 3: Cascaded amplifier (CE1 + CE2)	5
Laboratory development	7
Circuit simulation	7
Frequency analysis	8
Conclusion	9
References	10

## Objetives

- Diseña un amplificador en cascada cuya ganancia sea de 250.
- Cumplir con una impedancia de salida de 10 kΩ y buena estabilidad.

## Introduction

### Cascaded amplifiers

A cascaded amplifier is a system composed of two or more amplifier stages connected in series, where the output of one stage feeds the input of the next. This architecture is used when a single stage cannot provide the required level of gain, impedance, or bandwidth.

The main objective of a cascaded design is to increase the total gain without sacrificing stability or distorting the signal. Mathematically, if there are two stages, the total gain of the system is:

$$A_{Total} = A_1 \cdot A_2$$

Cascaded amplifiers are fundamental in applications such as audio, instrumentation, telecommunications, and analog electronics in general, where precision, high gain, and impedance control are required.

## Materials used

- Frequency meter
  - Alternating current
  - Variable frequency
- Rigol DS1052t oscilloscope
  - 2 channels
  - 50 MHz
- Breadboard
- Power supply
  - Direct current
- BJT 337 transistor
- Capacitors
  - 2.2 μF (Input)
  - 10 μF (Output)
  - 100 μF (Bypass)
- Resistors:
  - 2.2 kΩ, 560 Ω, 180 Ω, 47 kΩ, 8.2 kΩ
  - 3.3 kΩ, 470 Ω, 220 Ω, 47 kΩ, 6.2 kΩ

## Development

### Selection of transistors

Configuration	Total gain	Output impedance	Funcion
EC + EC	High	High ( $\approx RC$ )	Output to another stage
EC + CC (follower)	Moderate–high	low	Couple resistive loads

Each stage can be optimized for a specific function:

- A common-emitter stage that provides high voltage gain.
- A common-collector stage that offers low output impedance, ideal for coupling to loads.

By combining both stages, high gain and good impedance matching are achieved, and signal integrity is improved.

The following must be taken into account:

- Proper bias of each transistor in the active region.
- Capacitor coupling, which blocks DC components between stages.
- Bandwidth depends on  $R_C$  and parasitic capacitances.

### Statement specifications

Ganancia total deseada:  $A_V = 250V$

- Output impedance:  $R_{out} = 10 K\Omega$
- Thermal voltage:  $V_T = 26mV$
- Input voltage:  $V_i = 200mV$
- Assume  $\beta = 170$

**Problem:** The common-collector does not provide gain for coupling with the first common-emitter stage, and a gain of 250 cannot be reached with a single amplifier stage → it is decided to have two common-emitter stages.

## Stage 1: First common-emitter amplifier (CE1)

The following parameters are chosen:

- Desired gain  $A_{v1} = -25$
- Collector current  $I_C = 1 \text{ mA}$

### Resistencia del emisor (sin bypass)

Since the CE is our first amplifier stage and only a gain of 25 is sought, it is decided not to use bypass in order to have less distortion and greater thermal stability.

$$R_E = \frac{V_E}{I_E} = \frac{0,1V}{1mA} = 100\Omega \rightarrow \text{The commercial value } 100 \Omega \text{ is chosen.}$$

### Base voltage

$V_E = 0,1V$  is chosen to achieve high amplification.

$$V_B = V_E + V_{BE} = 0,1 + 0,7 = 0,8V$$

### Internal emitter resistance

$$r_e = \frac{V_T}{I_E} = \frac{26mV}{1mA} = 26 \Omega$$

### Collector resistance

To ensure that the Q-point is in the active region, it is ideally placed at the center of the load line:

$$A_V = -\frac{R_C}{r_e + R_E} \rightarrow R_C = A_V \cdot (r_e + R_E) = 3,15K\Omega \rightarrow \text{The commercial value } 3.3 \text{ k}\Omega \text{ is chosen.}$$

### Q-point verification

$$V_{RC} = R_C \cdot I_C = 3,3K\Omega \cdot 1mA = 3,3 V$$

$$V_{RE} = R_E \cdot I_E = 100\Omega \cdot 1mA = 1 V$$

$$V_{CE} = V_{CC} - V_{RC} - V_{RE} = 10,7 V$$

We have:  $\frac{V_{CC}}{2} = 7,5 \rightarrow$  The Q-point ends up above, ensuring active region.

### Voltage divider R1 and R2:

$$I_B = \frac{I_C}{\beta} = \frac{1mA}{170} = 5,88\mu A \rightarrow I_{R1R2} = 10 \cdot 5,88\mu A = 58,8\mu A$$

$$R_2 = \frac{V_B}{I_{R1R2}} = \frac{0,8V}{58,8\mu A} = 13,6 k\Omega \rightarrow \text{It is decided to use } 15 k\Omega \text{ (commercial)}$$

$$R_1 = \frac{V_{CC}-V_B}{I_{R1R2}} = \frac{15V-0,8V}{58,8\mu A} = 241,4 k\Omega \rightarrow 240 k\Omega \text{ (commercial) can be used}$$

### Stage 2: Second common-emitter amplifier (CE2)

The following parameters are chosen:

- Desired gain  $A_{v1} = -10$
- Collector current  $I_C = 1 mA$

### Internal emitter resistance

$$r_e = \frac{V_T}{I_E} = \frac{26mV}{1mA} = 26 \Omega$$

### Collector resistance

To ensure that the Q-point is in the active region, it is ideally placed at the center of the load line:

$$A_V = -\frac{R_C}{r_e + R_E} \rightarrow R_C = A_V \cdot (r_e) = 260\Omega \rightarrow \text{The commercial value } 270 \Omega \text{ is chosen.}$$

Here  $R_E = 0$  because a full bypass will be used.

### Emitter resistance

Here  $V_E = 0,1V$  to achieve greater stability and lower amplification.

$$R_E = \frac{V_E}{I_E} = \frac{1V}{1mA} = 1000\Omega \rightarrow \text{The commercial value } 1 k\Omega \text{ is chosen.}$$

### capacitor $C_E$

$f_{min} = 20 Hz$  is chosen and a maximum impedance of  $\frac{R_E}{100} = 100 \Omega$

$$C_E = \frac{1}{2\pi \cdot 20 \cdot 100\Omega} = 25 \mu F \rightarrow A 79.6 \mu F capacitor can be used.$$

→ The commercial value 100  $\mu F$  is chosen.

### Base voltage

$$V_B = V_E + V_{BE} = 1 + 0,7 = 1,7V$$

### Q-point verification

$$V_{RC} = R_C \cdot I_C = 270\Omega \cdot 1mA = 0,27V$$

$$V_{RE} = R_E \cdot I_E = 1K\Omega \cdot 1mA = 1V$$

$$V_{CE} = V_{CC} - V_{RC} - V_{RE} = 13,73V$$

We have :  $\frac{V_{CC}}{2} = 7,5$  → Although the point is not centered, it is still in the active region with a wide margin.

### Voltage divider R1 and R2:

$$I_B = \frac{I_C}{\beta} = \frac{1mA}{170} = 5,88\mu A \rightarrow I_{R1R2} = 10 \cdot 5,88\mu A = 58,8\mu A$$

$$R_2 = \frac{V_B}{I_{R1R2}} = \frac{1,7V}{58,8\mu A} = 28,9 K\Omega \rightarrow It is decided to use 27 k\Omega (commercial)$$

$$R_1 = \frac{V_{CC}-V_B}{I_{R1R2}} = \frac{15V-1,7V}{58,8\mu A} = 226,1 K\Omega \rightarrow 220 k\Omega (commercial) can be used$$

### Stage 3: Cascaded amplifier (CE1 + CE2)

#### Combined total gains

Recalculating the gains with the commercial resistor values we obtain:

$$A_{V1} = -26,19$$

$$A_{V2} = -10,38$$

$$A_V = (-26,19) \cdot (-10,38) = 271,98$$

## Calculation of input and output capacitors

$f_{min} = 20 \text{ Hz}$  is chosen

$$R_{div} = \frac{240K \cdot 15K}{240K + 15K} = 14,1K\Omega$$

$$C_i = \frac{1}{2\pi \cdot 20 \cdot 14,1K\Omega} = 0,56 \mu F \rightarrow \text{A } 1 \mu F \text{ capacitor can be used.}$$

→ An output load of 10 is considered.

$C_{out} = \frac{1}{2\pi \cdot 20 \cdot 10K\Omega} = 0,8 \mu F \rightarrow \text{A } 10 \mu F \text{ capacitor can be used; a larger value is chosen so that low frequencies do not suffer as much distortion.}$

## Coupling capacitor

→ It is necessary so that the bias of the two stages does not affect each other.

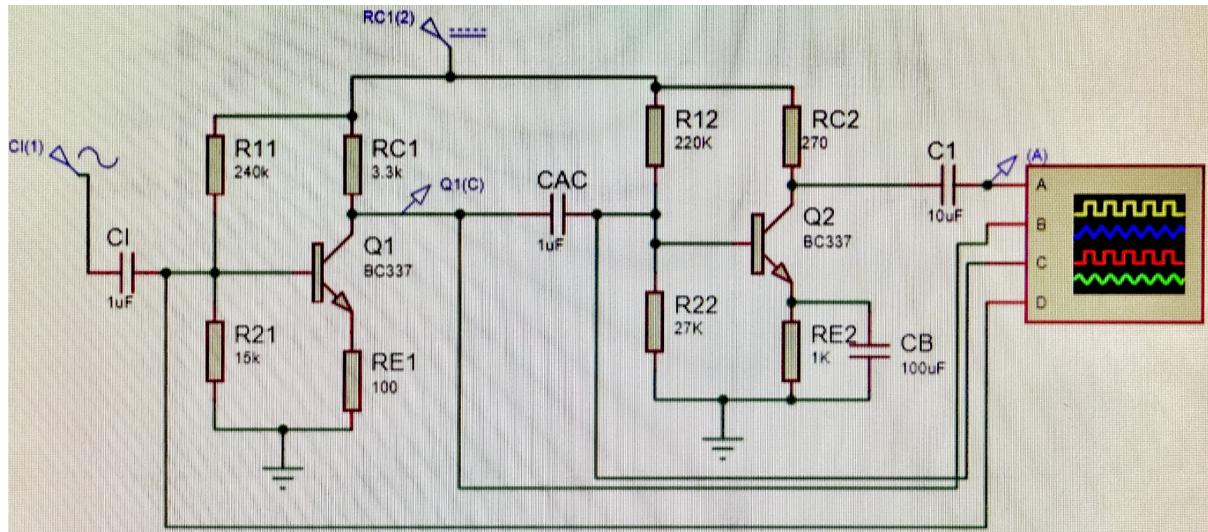
$$R_{div} = \frac{220K \cdot 27K}{220K + 27K} = 24,1K\Omega$$

$$C_{ac} = \frac{1}{2\pi \cdot 20 \cdot 24,1K\Omega} = 0,33 \mu F \rightarrow \text{A } 1 \mu F \text{ capacitor can be used.}$$

## Laboratory development

### Circuit simulation

The two stages were first assembled separately and then joined through the coupling capacitor. The input and output capacitors were connected according to the calculations.



The frequency from the frequency meter was varied from 20 Hz to 3.2 MHz, obtaining the following results:

Signals were measured at the following points:

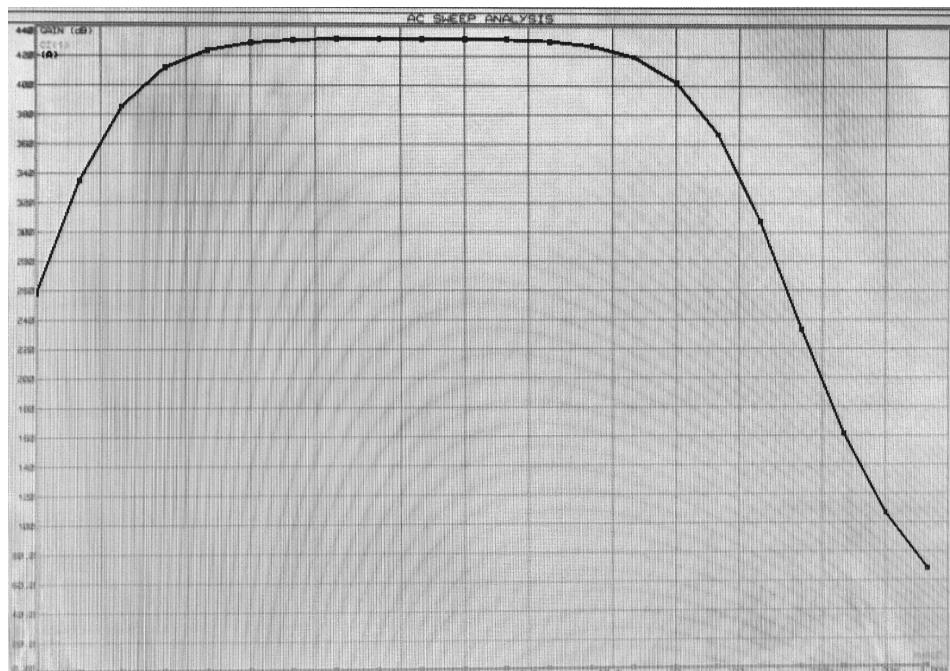
- A (input): pure sine wave
- B (collector of Q1): signal inverted with respect to the input (confirming negative gain in stage 1)
- C (base of Q2): sine wave superimposed on DC bias
- D (output): signal in phase with the input, amplified

This confirms:

- Both stages operate correctly.
- There is double phase inversion → output in phase with input.
- Proper bias in both stages.
- Correct coupling with C\_AC (interstage capacitor).

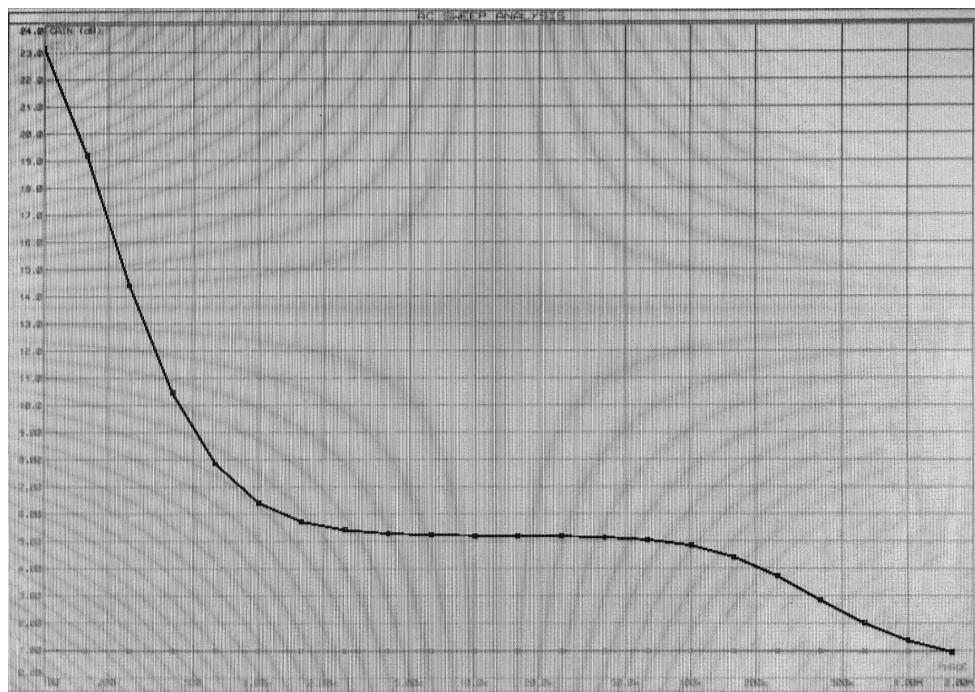
## Frequency analysis

An AC analysis sweep was performed, obtaining the following response:



↑ *Image 2<sup>1</sup>*

*Image 1<sup>2</sup>* ↓



<sup>1</sup> Labcenter Electronics. (2024). *Proteus Design Suite 8.15* [Software de simulación electrónica]. <https://www.labcenter.com>

<sup>2</sup> Labcenter Electronics. (2024). *Proteus Design Suite 8.15* [Software de simulación electrónica]. <https://www.labcenter.com>

### **Conclusion**

It was possible to design and simulate a cascaded amplifier composed of two stages in common-emitter configuration, achieving a total gain greater than the required 250. The design kept both transistors biased in the active region, ensuring thermal stability and correct operation.

During the frequency analysis, it was observed that the first stage provides an initial linear gain of approximately 24, which decreases smoothly to 18.5 at frequencies on the order of 200 kHz. When both stages are connected by a coupling capacitor, the total gain stabilized between 260 and 430, showing the reinforcement provided by the second stage.

The expected phase inversion between stages was verified, and it was confirmed that the output signal maintains the phase with respect to the input, as a result of two consecutive inversions.

Taken together, the design meets the statement's requirements, both in gain and output impedance, and demonstrates correct operation in simulation. The proposed assembly can be replicated in the laboratory with the indicated commercial values.

### References

Labcenter Electronics. (2024). *Proteus Design Suite 8.15* [Software de simulación electrónica]. <https://www.labcenter.com>

Floyd, T. L. (2012). *Principios de circuitos eléctricos* (9.<sup>a</sup> ed.). Pearson Educación.