UNSE
Universidad Nacional
de Santiago del Estero

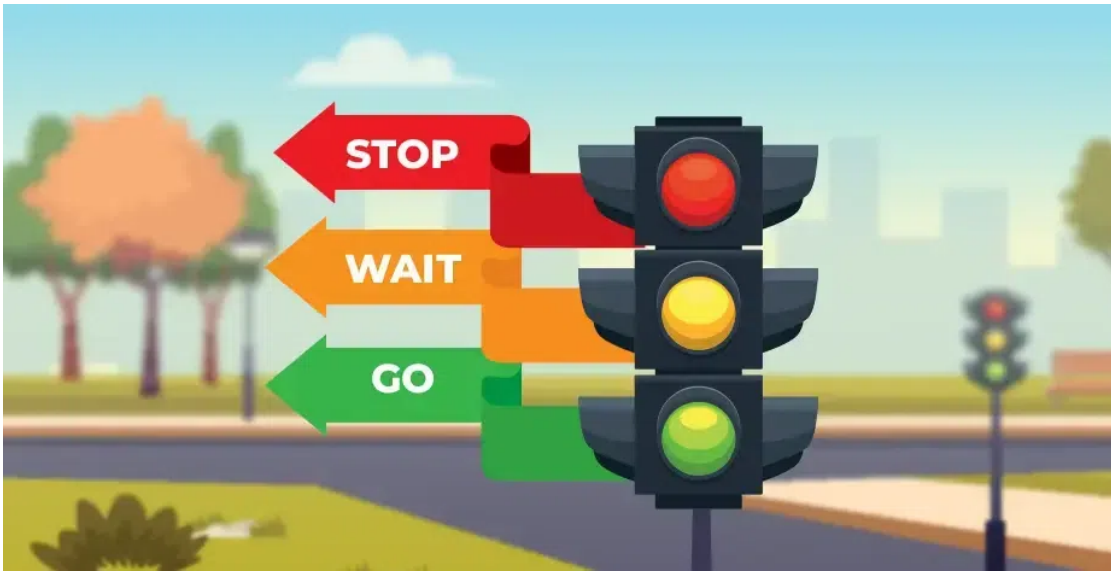
Facultad de Ciencias
Exactas y Tecnologías

Santiago del Estero, 4 de julio del 2024

Ingeniería eléctrica

TRAFFIC LIGHTS IN PROTEUS

SISTEMAS LOGICOS



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Objetives

- Design the logic gates and truth tables for a traffic light.
- Simulate the operation of two synchronized traffic lights in Proteus.

Introduction

Proteus program

Proteus is an electronic circuit design and simulation tool developed by Labcenter Electronics. It is widely used in education and industry for its ability to simulate circuits and microcontrollers.

Traffic light logic

Traffic lights regulate traffic through a sequence of lights (red, yellow, and green) that indicate when to stop, get ready, or go. Synchronizing traffic lights in an urban network improves traffic flow and reduces waiting time. Electronic controllers manage the signals, adjusting cycles and times according to traffic volume.
To simplify the simulation and the logic circuit of our traffic lights, the traffic volume will not be considered here when setting cycle times.

Determination of cycles and timing diagrams

The following cycle times are chosen:
Green: 27 seconds
Yellow: 3 seconds
Red: 27 seconds
Yellow: 3 seconds
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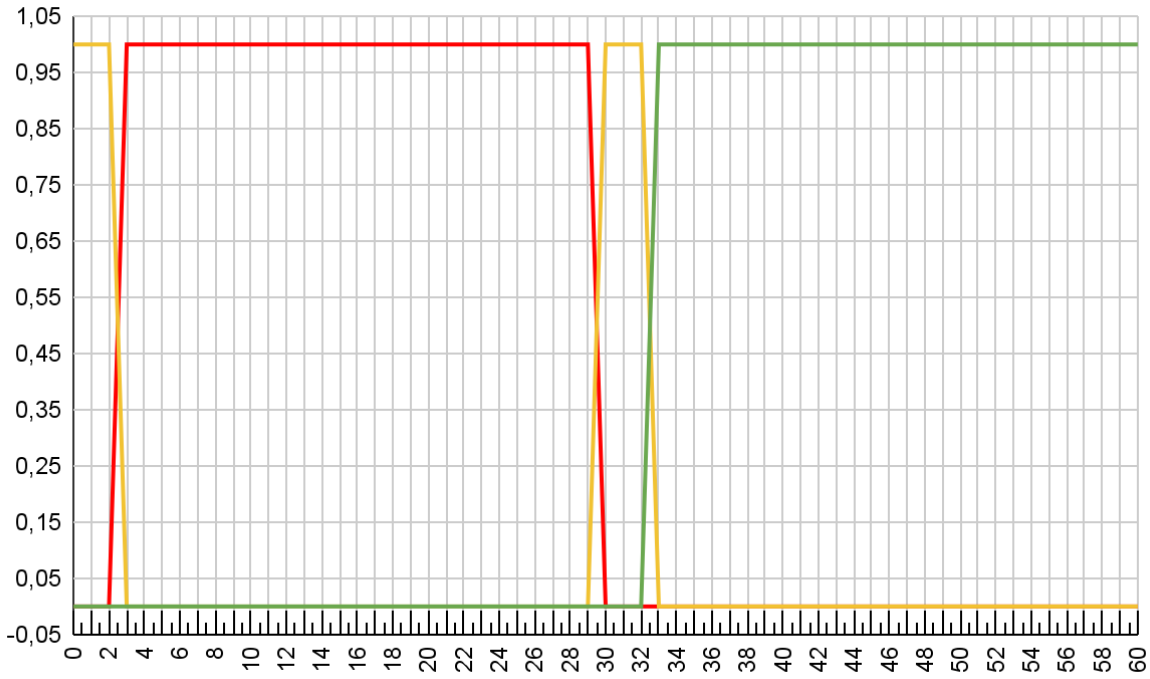
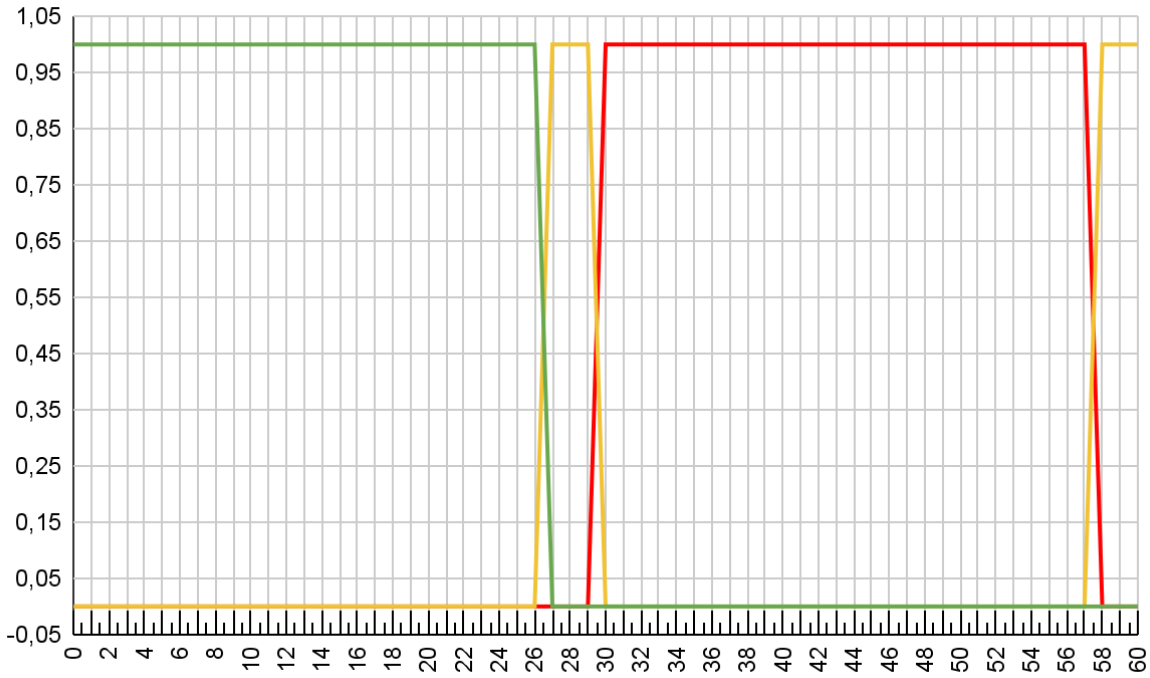
Total cycle time: 60 seconds

Light states as a function of time

Using Excel, a table of the value of each light versus time was generated and two plots were produced.
Synchronized states of the red, yellow, and green lights for each traffic light as a function of time over 60 seconds.

Timelines





It is noted that the state-change timings shown in the plots display a duration of 1 second, which will be much shorter in the Proteus simulation or in a real design.

Frequency source

Since we are working in seconds, a frequency of 1 Hz is used to simplify the circuit and avoid needing a counter or flip-flop as a frequency divider.

Conversion from base 10 seconds to base 2

It is necessary to convert the seconds from base 10 to base 2.

Two counters are used, one for the units and another for the tens, in order to display a 7-segment readout of the passing time.

$$2|7_{10} = 0010|0111$$

$$3|0_{10} = 0011|0000$$

$$3|3_{10} = 0011|0011$$

$$5|7_{10} = 0101|0111$$

$$0|3_{10} = 0000|0011$$

$$6|0_{10} = 0110|0000$$

<u>Materials used in the Proteus program</u>

- 7-segment display
- 2 decade counters (74LS90)
- 2 BCD-to-7-segment decoders (47LS248)
- AND_8 gates
- NOT gates
- OR gates
- JK flip-flops
- LEDs
- Traffic light indicators

Procedures (Version 1)

A 1 Hz frequency source was connected to two-decade counters in series in order to obtain a numeric counter capable of counting from 00 to 99.

A BCD-to-7-segment decoder was connected to each counter, and each decoder was connected to a 7-segment display, allowing the time to be viewed during the simulation.

In addition, each binary output of the decade counters was wired through a NOT gate, making the inverted state of each binary output available for later use.

A JK flip-flop was connected to each LED of the traffic lights, to be used for setting and resetting their state when the counters reach the required times.

The conversions from base-10 to base-2 times and the outputs (and complements) of the decade counters were used through 8-input AND gates to activate and deactivate the flip-flop outputs at the previously indicated times.

LEDs driven by each output of the decade counters were also added in the simulation in order to observe the binary numbers increasing over time.

Results (Final TP V1) see attachments

The simulation works correctly and the traffic lights synchronize well.

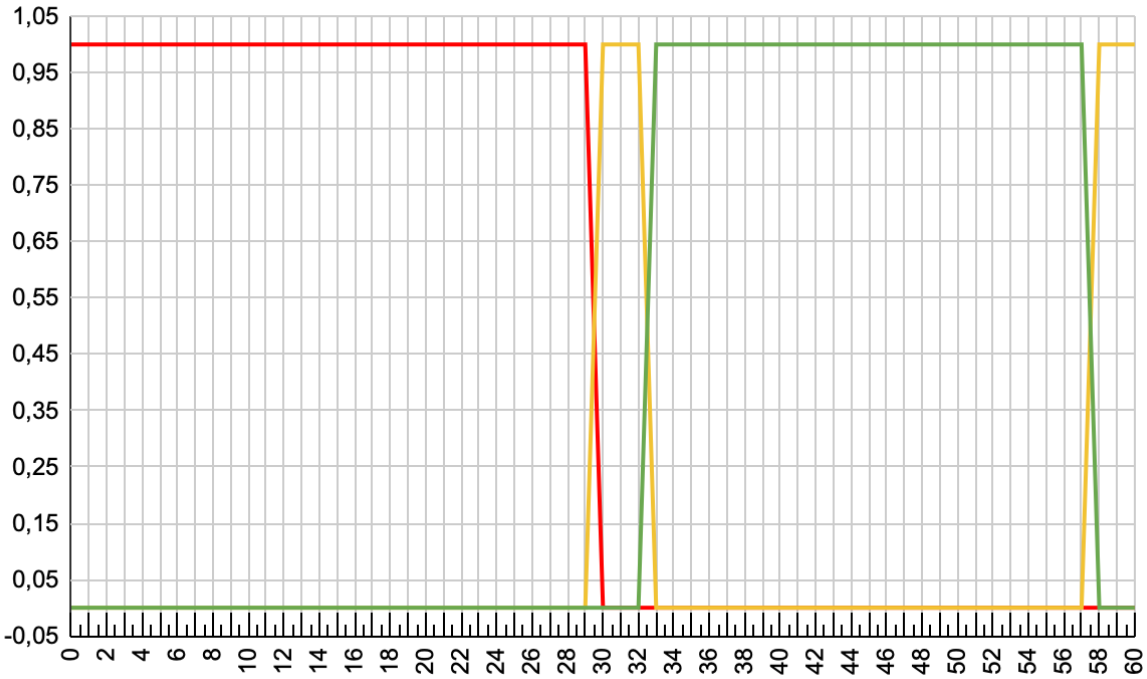
An error is observed in the yellow light timings. During the first cycle, the schedule works as required in reality: the second traffic light changes from green to yellow and from yellow to red before the first traffic light changes to yellow and then to green.

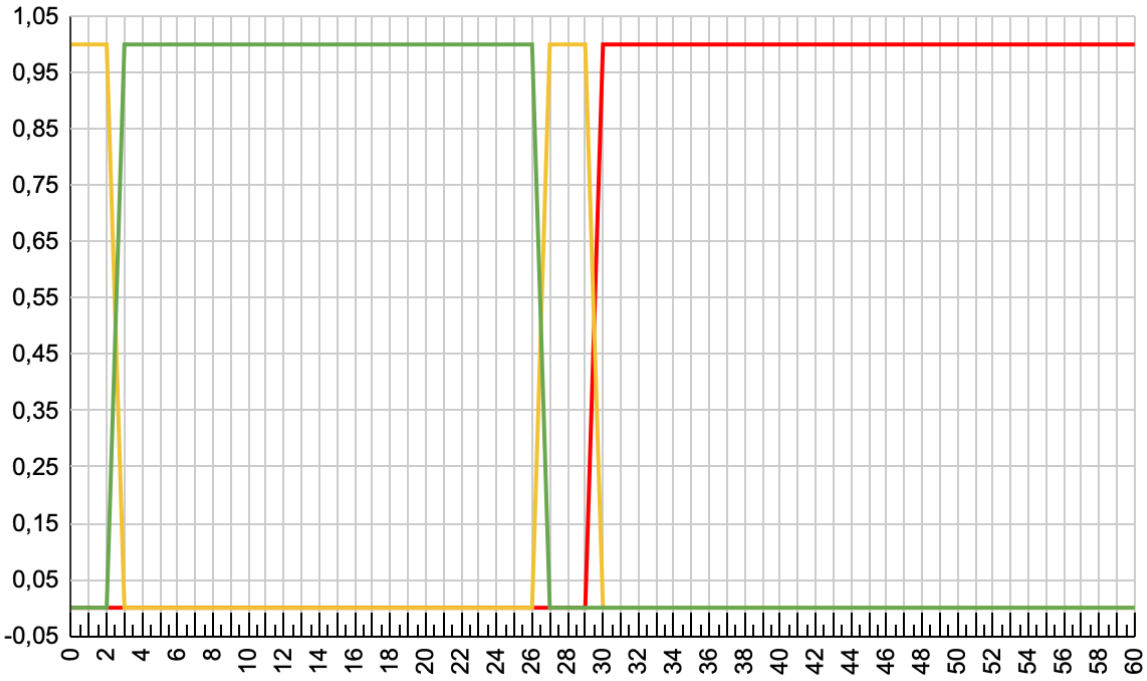
However, during the transition from the first cycle to the second, the second traffic light changes from red to yellow and yellow to green before the first traffic light changes to red.

Procedures (Final TP V2)

It was decided to modify the timelines and apply them to simulation version 1, changing the inputs of the AND gates that control the Set and Reset of the flip-flops.

The modified timelines applied during version 2 of the simulation are shown there.

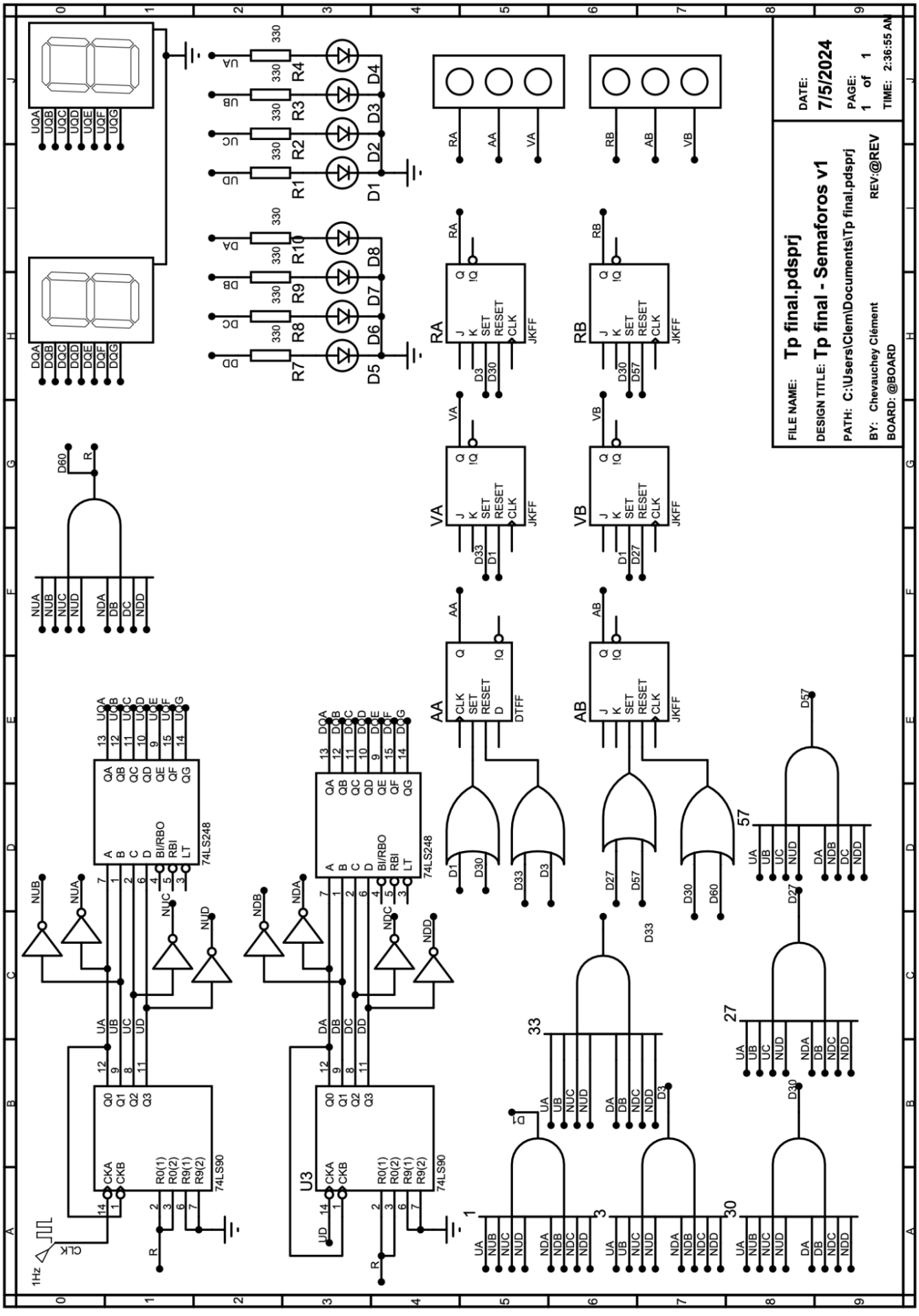




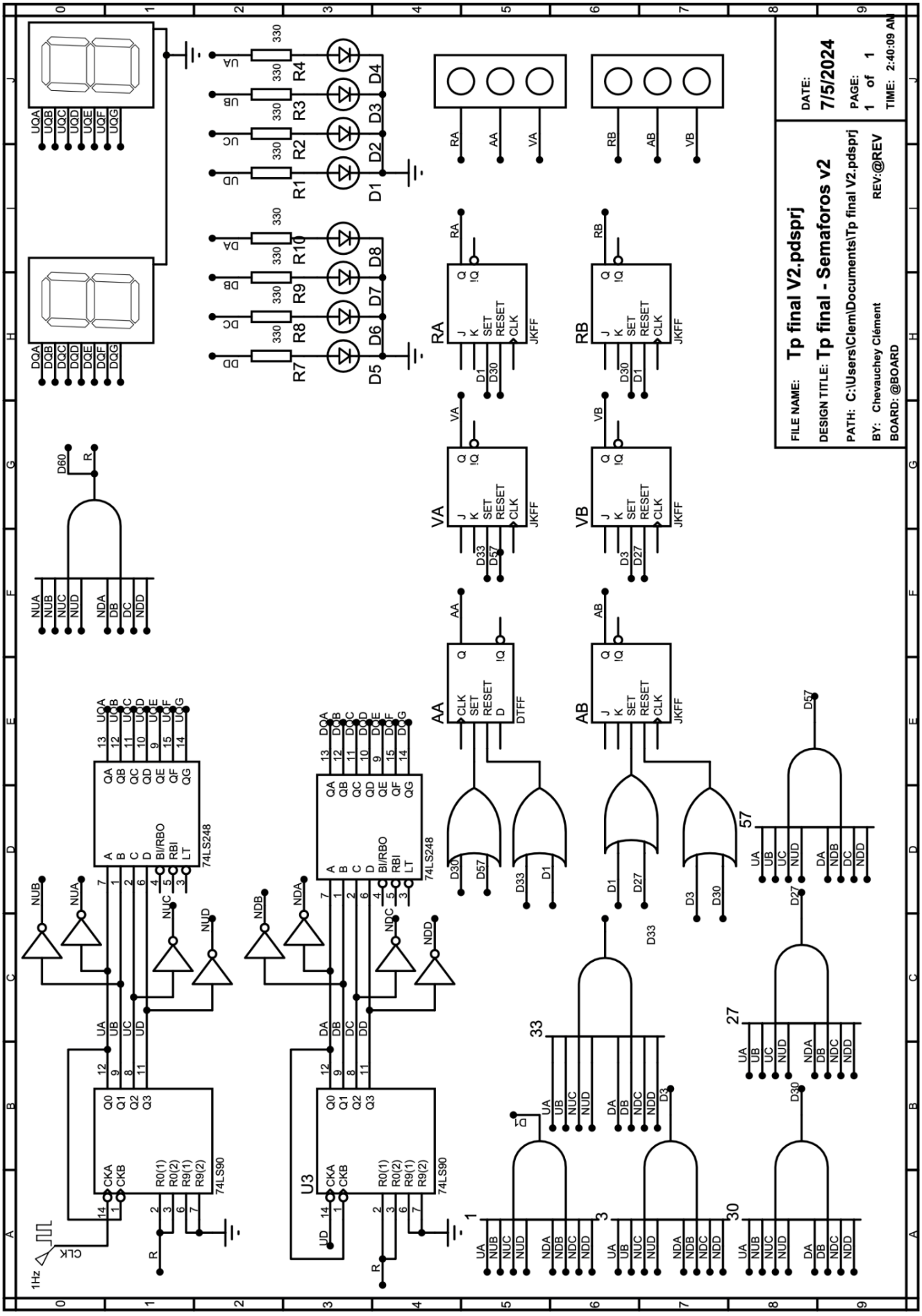
Results (Final TP V2) see attachments

In version 2 the two traffic lights meet the objectives and synchronize perfectly.

TP Final - Version 1



TP Final - Version 2



References

- Proteus - Labcenter Electronics 2024 (https://www.labcenter.com/)