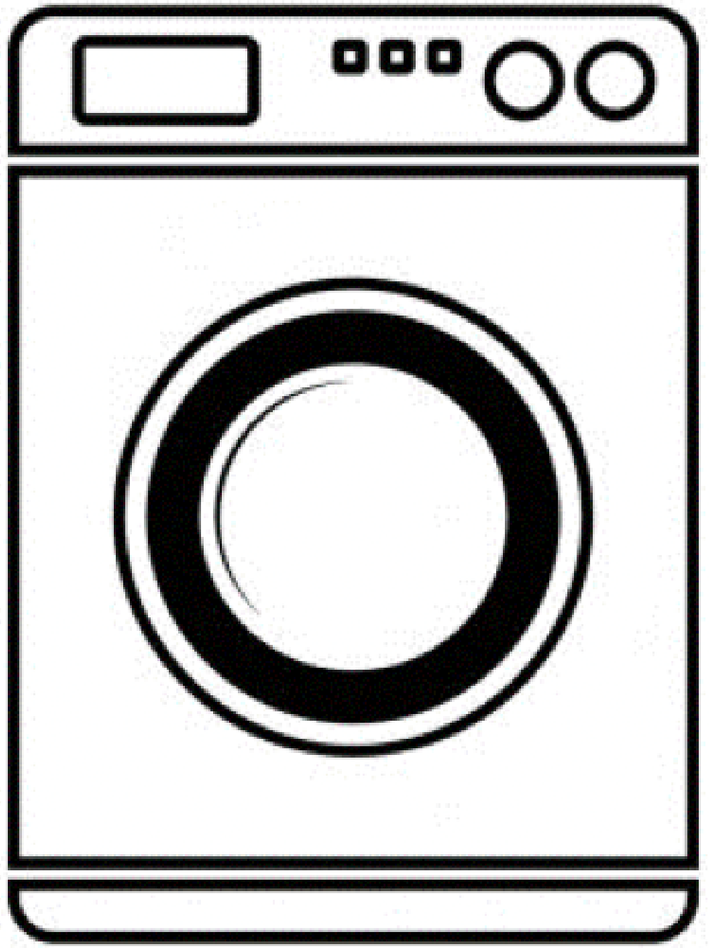
RTL Design

Automatic Washing Machine using Verilog HDL



Simulation with TestBench

Presented by: Yogesh Yadav (19ECU024)

Project requirements:

Overview of Project tasks-

- In this project, we are required to design, model, and simulate a washing machine controller, Use a two or a three-process FSM Verilog coding style for the FSM block.

- Verilog code for the timer design.

- Write a test bench to verify the operation of the timer. Synthesise the controller on FPGA and study the performance parameters (delay, FPGA resources, power consumption, and equivalent gate count).

About the Project

Implementation of automatic washing machine using Verilog HDL

OPERATIONS

- Various real-life scenarios can be represented by Finite State Machines like the control system of an automatic washing machine.
- Assigning the main stages of the process like Close the door, filling the water, adding a detergent, cycling, draining and spinning various states that can be implemented as a State Machine.
- Writing a test bench to observe the working of the machine.
- Using Xilinx ISE 14.7 to implement the control system.

Figure1: Different States of washing machine

System Design

The washing machine controller has the following functionalities:

- The washing machine has the following states: idle, soak, wash, rinse, spin.
- There are three modes of operation i.e mode1, mode2 and mode3.
- Different time durations are allocated to each mode of operation

Design Flow:

The washing machine controller has the following functionalities:

1

- The washing machine has the following consecutive states: idle, fill, wash, drain, fill, rinse, drain, and spin.
- There is one control line to the washer water feed. Choice of hot or cold water wash is done manually by the user for simplicity.

2

There are two drum rotation speeds: low speed for the wash cycle and high speed for the spin cycle. Speed control is accomplished through an electrically controlled mechanism

3

During the wash cycle, the drum direction of rotation is controlled through the agitator mechanism. The figure is the Icon for the washing machine controller indicating the main input and output lines.

4

The below figure shows the block diagram of the automatic wash machine controller, in which the user selects the start button, and the remaining process is continued on the time allocated to each state of the machine i.e. wash, fill, drain etc.

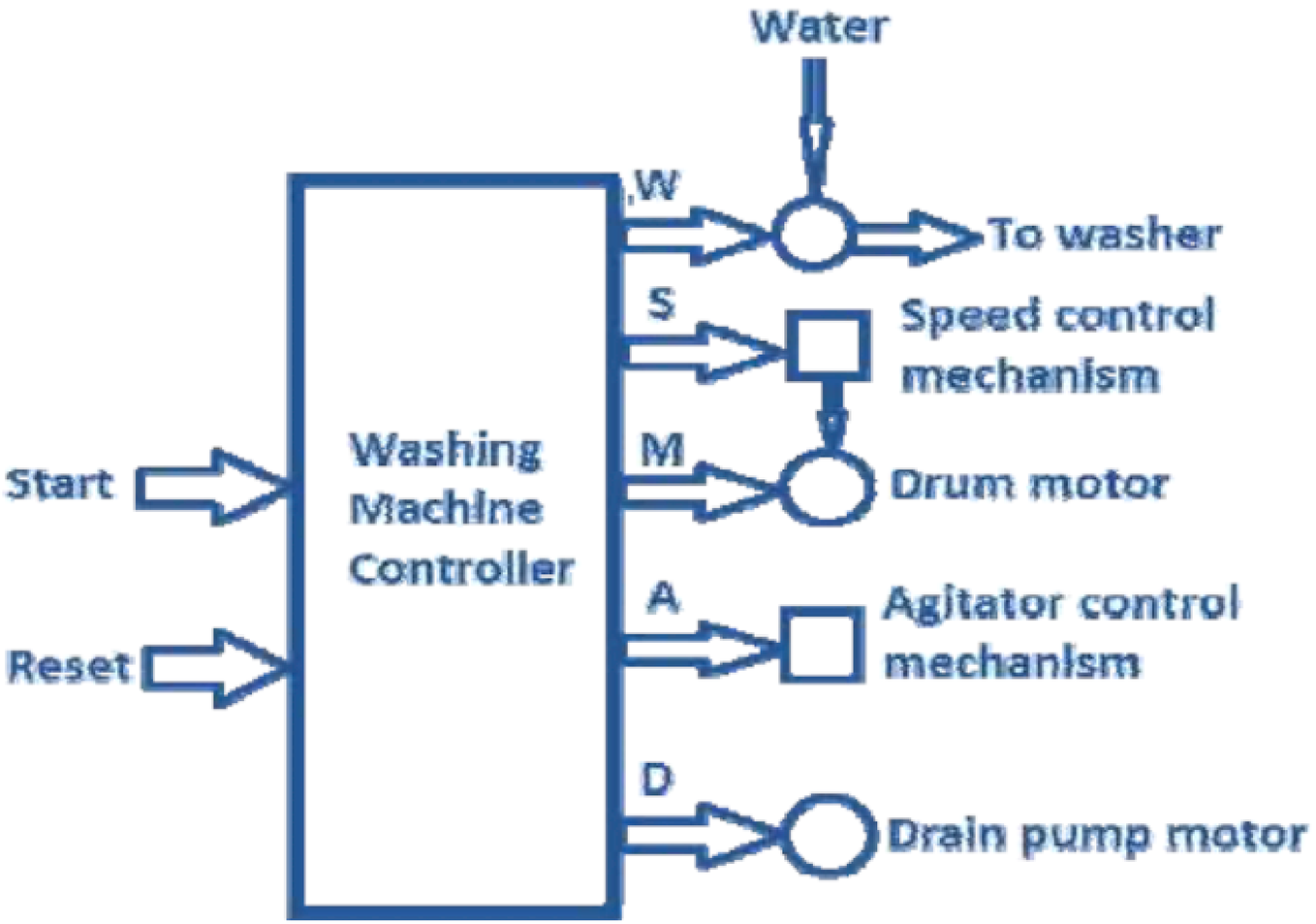
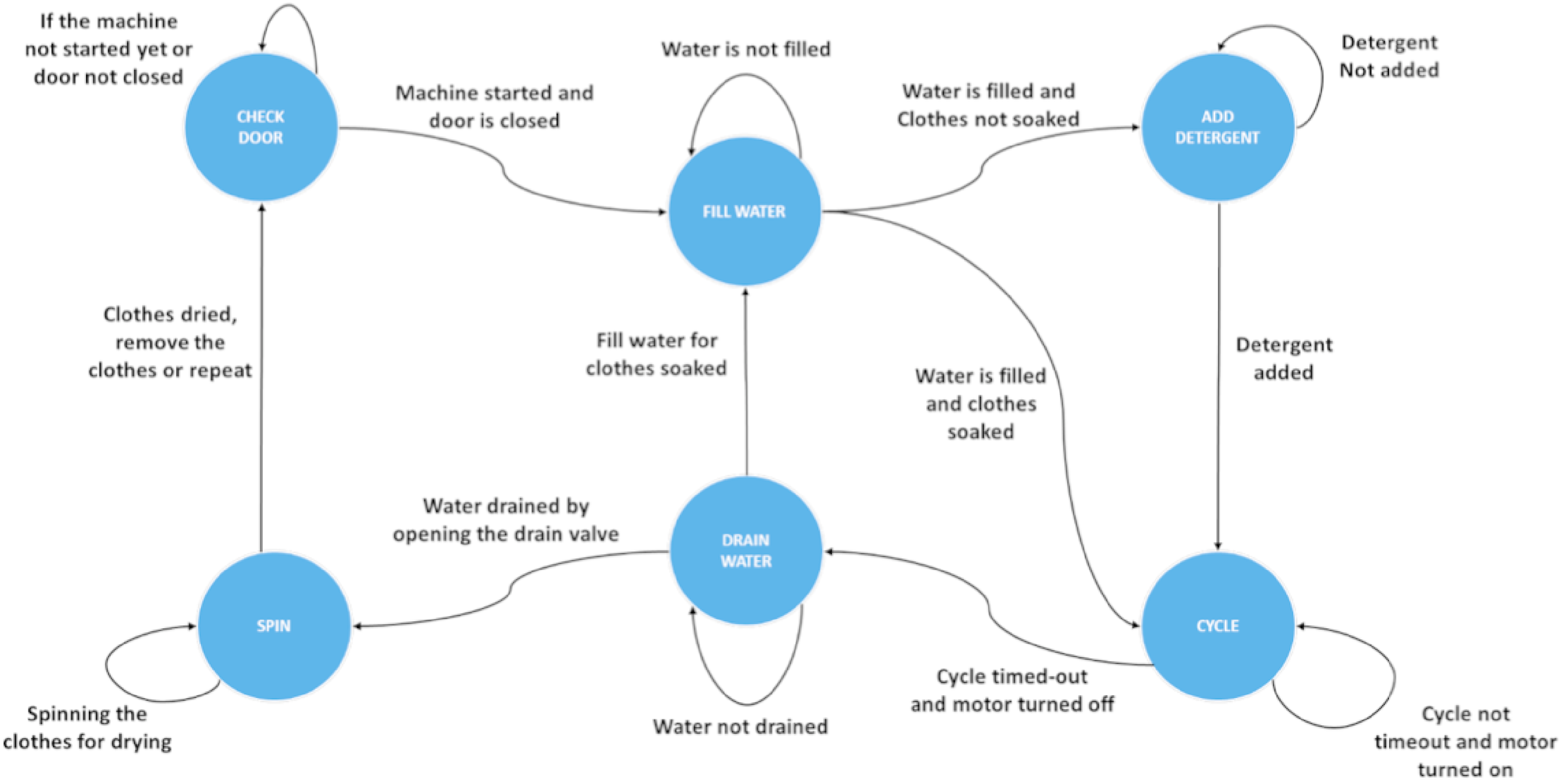


Figure 2: block diagram of washing machine


If the machine not started yet or door not closed
CHECK DOOR
Machine started and door is closed
Water is not filled
FILL WATER
Water is filled and Clothes not soaked
ADD DETERGENT
Detergent Not added
Clothes dried, remove the clothes or repeat
Fill water for clothes soaked
Water is filled and clothes soaked
Detergent added
Water drained by opening the drain valve
DRAIN WATER
SPIN
CYCLE
Spinning the clothes for drying
Water not drained
Cycle timed-out and motor turned off
Cycle not timeout and motor turned on

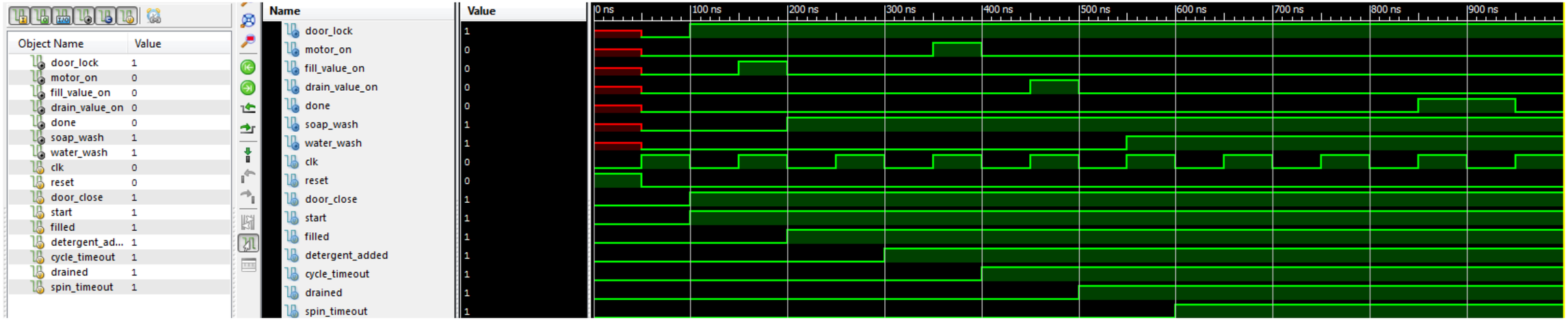
To design the washing machine the following are required to be done.

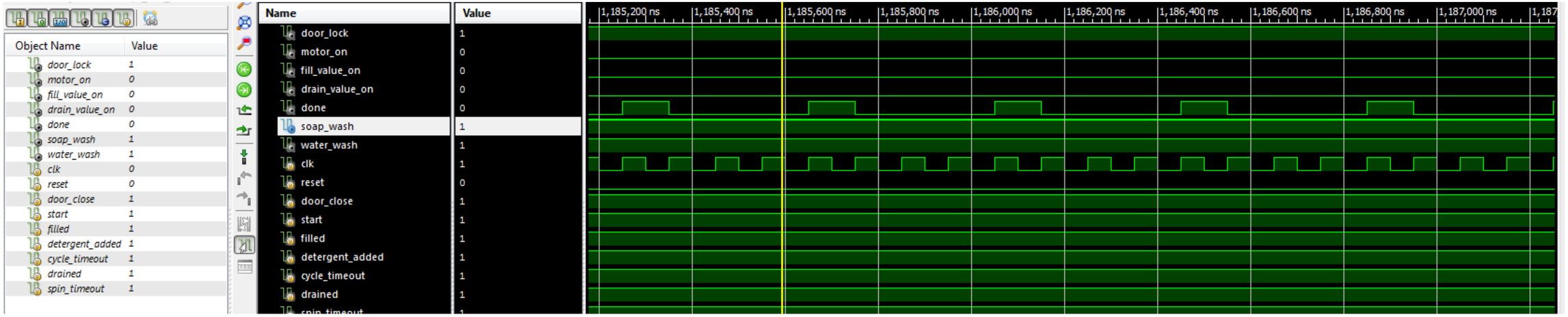
```
if(detergent_added==1)
begin
    next_state = cycle;
    motor_on = 0;
    fill_value_on = 0;
    drain_value_on = 0;
    door_lock = 1;
    soap_wash = 1;
    done = 0;
end
else
begin
    next_state = current_state;
    motor_on = 0;
    fill_value_on = 0;
    drain_value_on = 0;
    door_lock = 1;
    soap_wash = 1;
    water_wash = 0;
    done = 0;
end
```

```
if(cycle_timeout == 1)
begin
    next_state = drain_water;
    motor_on = 0;
    fill_value_on = 0;
    drain_value_on = 0;
    door_lock = 1;
    //soap_wash = 1;
    done = 0;
end
else
begin
    next_state = current_state;
    motor_on = 1;
    fill_value_on = 0;
    drain_value_on = 0;
    door_lock = 1;
    //soap_wash = 1;
    done = 0;
end
```

SIMULATION OF THE AUTOMATIC WASHING MACHINE

When the reset signal comes, all of the signals are set to enter the water state. As long as you no longer press the start button, the washing machine will automatically execute the process according to the predetermined process. The simulation results are as show.





Future Scope & Applications

1. The automatic washing machine has been implemented on Verilog HDL using Xilinx ISE.
2. The current project can be implemented on FPGA to demonstrate the code.
3. The project is based on Finite State Machine (FSM). Various other projects based on FSM can be implemented using the current project code as the basis.
4. More functionality may be included like different modes to wash the clothes based on the clothing material, temperature etc

Conclusion

Implementation of automatic washing machine using Verilog HDL

We use Verilog HDL language to design an automatic washing machine control system. We use this powerful language structure and concise code to describe the complex control logic. Through comprehend the corresponding hardware circuit and tools of Verilog HDL language to generate more than traditional logical design method which can adapt to the social development needs. We use hardware description language form digital system design which is not only flexible and convenient but also reduce the cost of development and the development cycle. This design method plays an increasingly important role in the future digital system design.

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Thank you!

Feel free to approach us
if you have any questions.