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Electronics and communication engineering

Semester VI

An implementation of Automatic washing machine using Verilog HDL

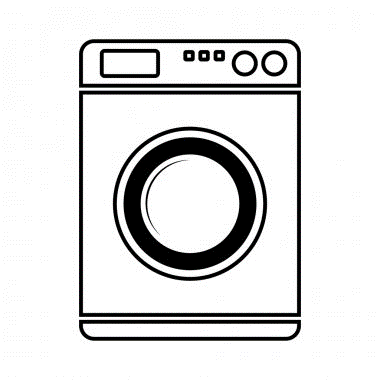
Report

Abstract

As described by digital system the language Verilog HDL is widely used in the circuit design, has its own advantages to be able to used as software language which describes hardware features that makes it efficient and has good readability, portability, etc. It's advantages not only reduce the hardware development cycle but also greatly reduce development costs. This report describes the characteristics and application of Verilog HDL and takes the automatic washing machine control system as examples to illustrate the practicality of HDL. The result of simulation shows this method is feasible and effective.

The Digital Design is simulated using Xilinx 14.1 ISE. The Verilog code for the Control System is then synthesized and implemented on Spartan 6 FPGA development board to verify its operation. This paper also demonstrates the reduction in Development Cycle by the use of Hardware Description Languages and FPGAs.

IndexTerms— Verilog HDL, FPGA, Washing Machine Control System, Finite State Machine (FSM) model, Verilog‐ Hardware description languages, Automatic Washing machine.



Introduction

# INTRODUCTION OF VERILOG HDL

With rapid development of science and technology, the design of electronic systems also produce a revolutionary change, a new class of development tools related to electronic systems are spreading quickly. Hardware Description language (HDL) is a method to description of digital circuit. HDL describes a certain function of digital circuit usually has one or more files composition. With the rapid development of electronic system design automation (EDA) and large scale programmable of logic device, HDL has hierarchical description and simulation of any electronic components characteristics, so that the circuit designers and developers could describe the feature of the circuit freely.

Verilog language is a kind of abstract level of hardware description language. This language supports the early abstract design concept, and could realize the later abstract design. It includes the hierarchical structure, which allows designers to describe the complexity of the control.

Verilog HDL is a which is not only easy to use. but also has strong function, especially the Verilog HDL industrial standardisation, conforms to the trend of microelectronics technology Verilog HDL is used in digital design modeling from the switch level to abstract algorithm design level. These constructions can not only be used to design pattern on hardware inter current behaviour, but also on hardware design of scheduling pattern.

This is a deterministic finite state transducer: for each state and input, at most one transition is possible. Moore machine, is a finite state machine whose output values are determined solely by its current state. In this paper, Mealy State Machine is used to implement the control system of washing machine. The washing machine control system generates all the control signals required for the operation of washing machine and is designed using Verilog HDL. The digital design is implemented on Spartan 6 FPGA. Use of FPGAs facilitates the reduction in development cycle.

# THE DESIGN MACHINE OF AUTOMATIC WASHING

Because the Verilog HDL has the advantage of powerful language structure and concise code for complex control logic. So, this dissertation is based on Verilog HDL to design the control system of the washing machine. The principle of automatic washing machine

All automatic washers, regardless of type, model, or make, have only four basic functions of operation: (1) fill,(2) wash, (3) pump out, and (4) extraction (spin).The important parts of the washing machine; this will also help us understand the working of the washing machine.

A) Water inlet control valve: When you load the clothes in washing machine, this valve gets opened automatically and it closes automatically depending on the total quantity of the water required.

B) Water pump: The water pump circulates water through the washing machine. It works in two directions, re-circulating the water during wash cycle and draining the water during the spin cycle.

C) Tub: There are two types of tubs in the washing machine: inner and outer. The clothes are loaded in the inner tub, where the clothes are washed, rinsed and dried. The inner tub has small holes for draining the water. The external tub covers the inner tub and supports it during various cycles of clothes washing.

D) Agitator or rotating disc: The agitator is located inside the tub of the washing machine. It performs the cleaning operation of the clothes. During the wash cycle the agitator rotates continuously and produces strong rotating currents within the water due to which the clothes also rotate inside the tub.

E) Motor of the washing machine: The motor is coupled to the agitator and produces it rotator motion.

F) Timer: The timer helps setting the wash time for the clothes manually.

G) Drain pipe: The drain pipe enables removing the dirty water from the washing that has been used for the washing purpose.

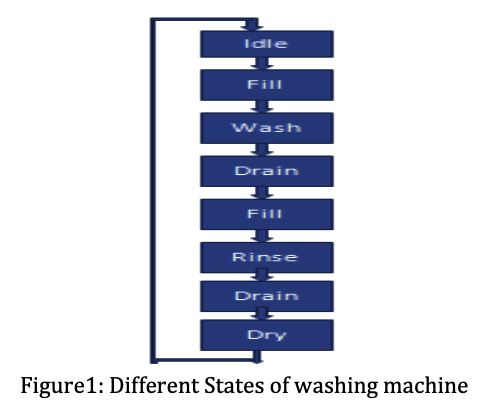
Operations

* Various real life scenarios can be represented by Finite State Machines like control system of an automatic washing machine.
* Assigning the main stages of the process like Close door, fill water, add detergent, cycle, drain and spin various states that can be implemented as a State Machine.
* Writing a test bench to observe the working of the machine.
* Using Xilinx ISE 14.7 to implement the control system.

# SYSTEM DESIGN

The washing machine controller has the following functionalities:

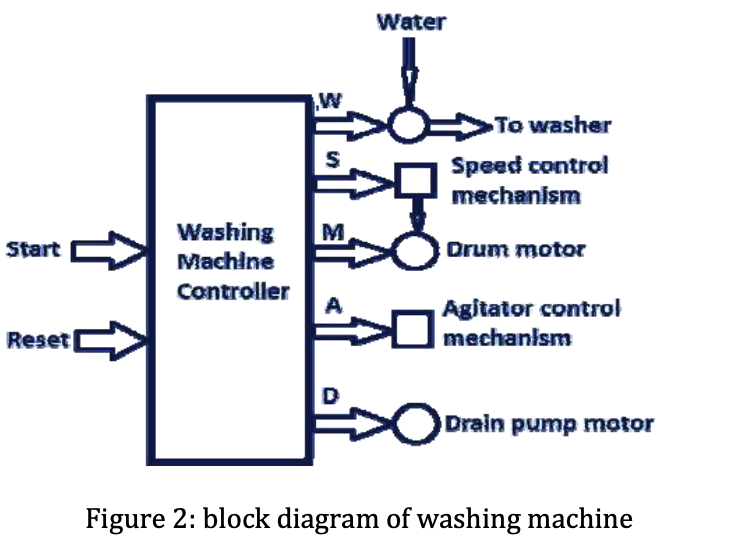
1. The wash machine has the following states: idle, soak, wash, rinse, spin.
2. There are three modes of operation i.e mode1, mode2 and mode3.

3. Different time durations are allocated to each mode of operation.

# Washing Machine Controller specifications

The washing machine controller has the following functionalities:

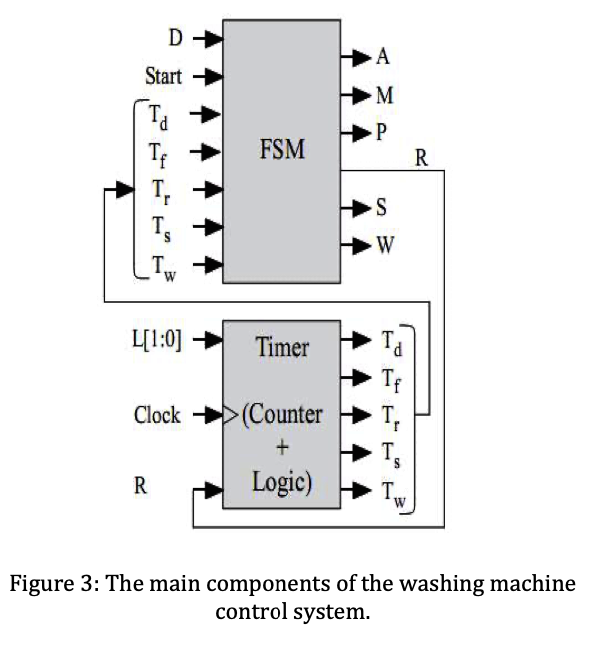
1. The wash machine has the following consecutive states: idle, fill, wash, drain, fill, rinse, drain, spin.
2. There is one control line to the washer water feed. Choice of hot or cold-water wash is done manually by the user for simplicity.
3. There are two drum rotation speeds: low speed for wash cycle and high speed for the spin cycle. Speed control is accomplished through an electrically controlled mechanism.
4. During the wash cycle, the drum direction of rotation is controlled through the agitator mechanism. Figure is the Icon for the washing machine controller indicating main input and output lines.



The below figure shows the block diagram of the automatic wash machine controller, in which the user selects the start button, the remaining process is continued on the time allocated to each state of the machine i.e. wash, fill, drain etc.

# WASH MACHINE CONTROLLER DETAIL

Figure2 shows the main components of the washing machine controller. The controller is composed of two blocks: a finite ‐ sate machine (FSM) block and a timer block. The FSM block receives some signals from the user, from the timer, and from other hardware parts such as the door sensor. FSM block output control the timer block and other hardware components of the washing machine.



It identifies the FSM input and output signals and their functionality. The timer block generates the correct time periods required for each cycle after it has been reset. The timer block is composed of an up‐counter and combinational logic to give the correct time signals once certain count values have been achieved. Of course the timer values will be determined by the clock frequency being used in the system. This, however, is beyond the scope of this dissertation.

# DESIGN FLOW

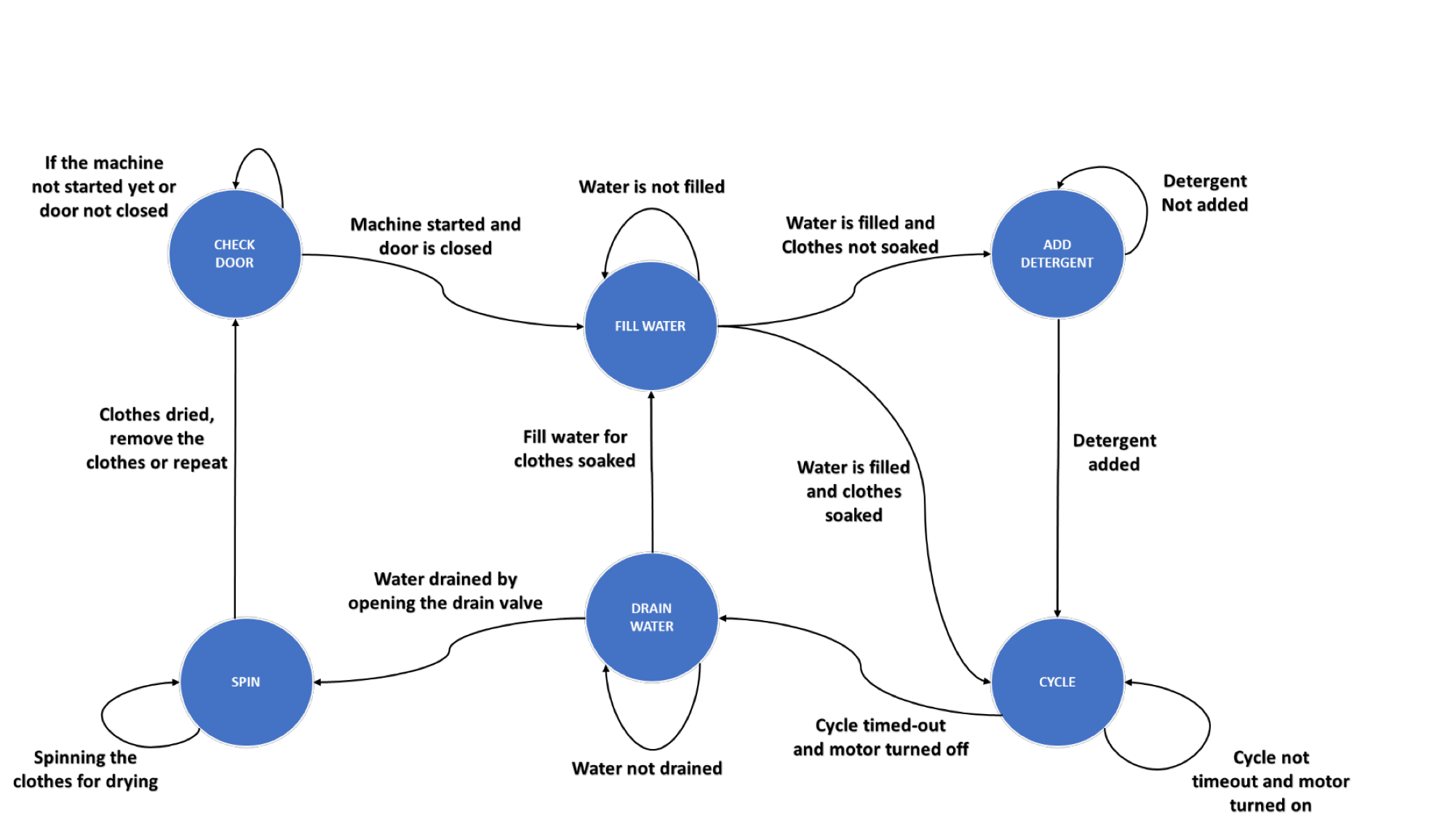
To design the washing machine the following are required to be done.

1. Design the Mealy state diagram for the washing machine whose specifications.

2. List the states of your state transition diagram

3. Design the timer but having the timing specifications.

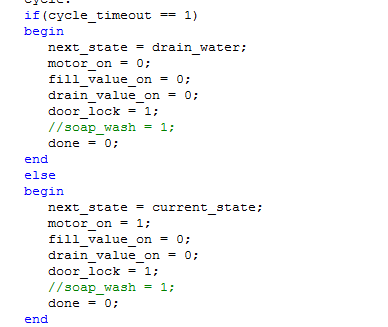
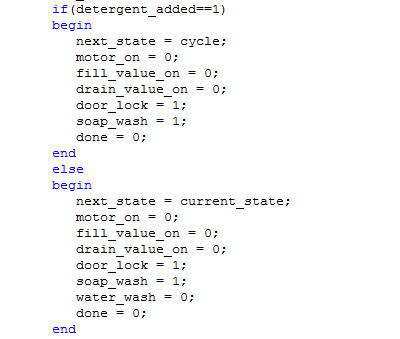
4. In new washing machines the door is locked as long as the machine is in operation. Draw the Mealy state diagram that satisfies this requirement.



# PROJECT REQUIREMENTS

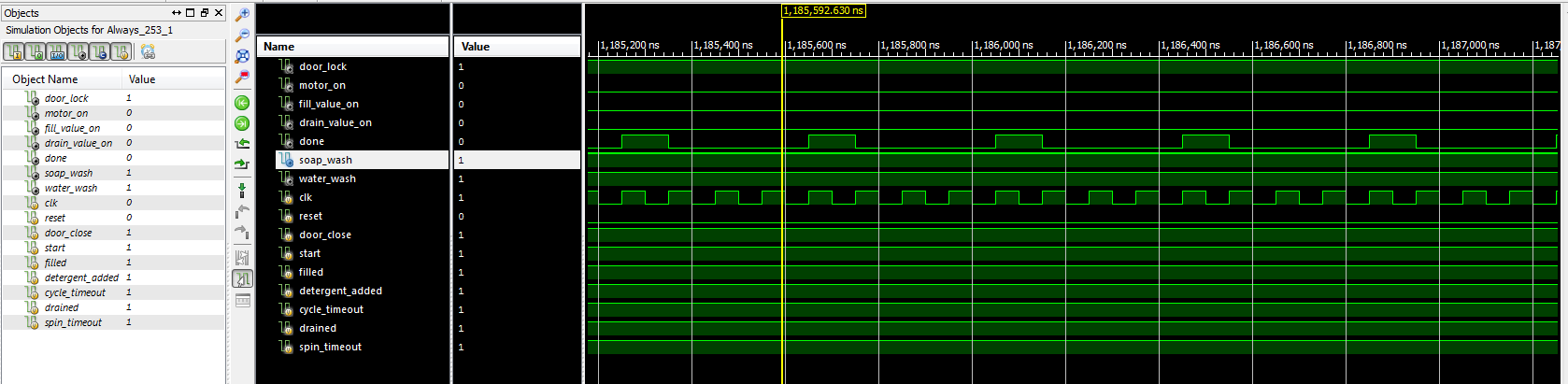
* In this project we are required to design, model, and simulate a washing machine controller, Use a two or a three‐process FSM Verilog coding style for the FSM block.
* Verilog code for the timer design.
* Write a test bench to verify the operation of the timer. Synthesize the controller on FPGA and study the performance parameters (delay, FPGA resources, power consumption, and equivalent gate count).

# PROGRAM

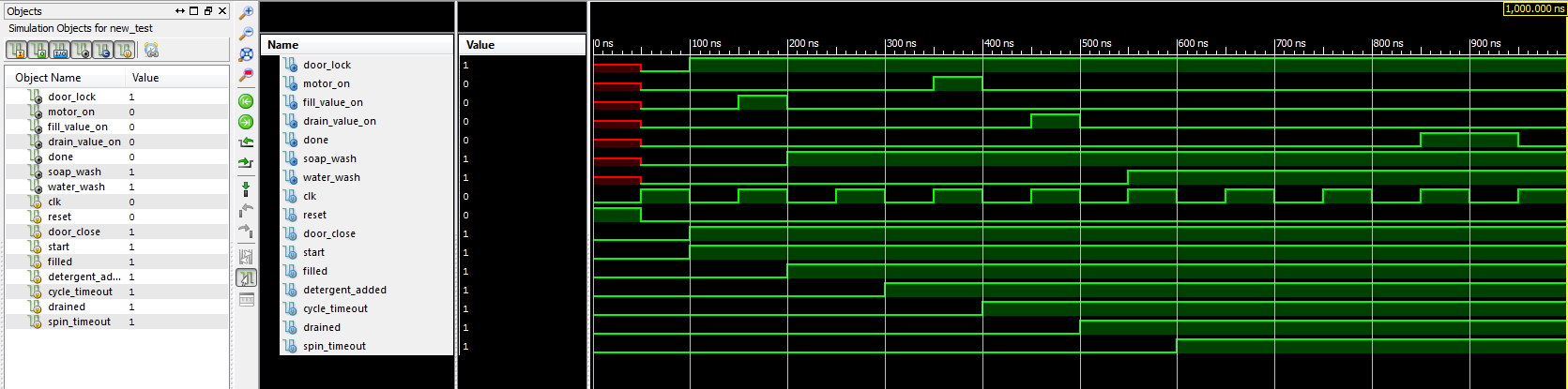


# Simulation of the Automatic Washing Machine

When reset signal comes, all of the signals are set to enter water state. As long as you no longer press start button, washing machine will automatically execute the process according to the predetermined process. The simulation results are as show.



Simulation of Automatic Washing machine controller



CONCLUSION

In this report we use Verilog HDL language to design automatic washing machine control system. We use this powerful language structure and concise code to describe the complex control logic. Through comprehend the corresponding hardware circuit and tools of Verilog HDL language to generate more than traditional logical design method which can adapt to the social development needs. We use hardware description language form digital system design which is not only flexible and convenient but also reduce the cost of development and the development cycle. This design method plays an increasingly important role in the future digital system design.

FUTURE SCOPE AND APPLICATIONS

* The automatic washing machine has been implemented on Verilog HDL using Xilinx ISE.
* The current project can be implemented on FPGA to demonstrate the code.
* The project is based on Finite State Machine (FSM). Various other projects based on FSM can be implemented using the current project code as the basis.
* More functionality may be included like different modes to wash the clothes based on the clothing material, temperature etc.

A FSM for washing machine control system was designed in Verilog HDL and implemented on Spartan 6 FPGA. The FSM designed has 6 states which perform different operations of a washing machine. The digital design of washing machine control system using Verilog HDL reduces the development cycle time.

In future, the number of states of the FSM can be increased for additional operations if required. Actuators like DC motor, stepper motor and solenoid valves can be interfaced with the FPGA to realize the real time operation and functioning of the washing machine control system.

REFERENCES

1. P. Usha, C H .Karuna, “An Efficient Implementation of Automatic Washing Machine Control System using Verilog”, IJSET, volume 2, issue 7, Sep-Oct 2014, pp 1575-1578.
2. Thomas & Moorby, the Hardware Verilog Description Language [M], Beijing tsinghua university press, 2001. 23‐36.
3. YangJimin YangJiBing, digital system design and Verilog HDL [M], Beijing: electronic industry press, 2003,   
   23(11):43‐45.
4. ”Design of Automatic Washing Machine Based on Verilog HDL” International Conference on Electronics and Optoelectronics, 29-31 July 2011, pp 38-40.
5. Wangguan,VerilogHDLanddigitalcircuitdesign[M],beijingmechanicalindustrypress,2005.
6. XiaYu wen, Verilog digital system design guide[M], beijing: aerospace university press, 2003. 2‐10.