

VL502: Analog IC Design, 2024-2025 Final Project

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1. Specifications

Design Specifications: Inorder to design our LDO we used (45nm HP) PDK. Since the gain of the Mpass is very low when we use min-length(45nm) we have simulated the results for 90nm and 135nm.

Table 1: Specifications of **Externally Compensated LDO**

Specification	Externally Compensated LDO
Input Voltage (V_{in})	1.4 V
Output Voltage (V_{out})	1 V
Power Supply Rejection Ratio (PSRR) at heavy load	60 dB
Minimum Load Current ($I_{load,min}$)	2 mA
Maximum Load Current ($I_{load,max}$)	10 mA
Load Capacitance (C_{load})	1 μ F
Quiescent Current ($I_{quiescent}$)	50 μ A
Transient Duration	100m

Table 2: Specifications of **Internally Compensated LDO**

Specification	Internally Compensated LDO
Input Voltage (V_{in})	1.4 V
Output Voltage (V_{out})	1 V
Power Supply Rejection Ratio (PSRR) at heavy load	60 dB
Minimum Load Current ($I_{load,min}$)	2 mA
Maximum Load Current ($I_{load,max}$)	10 mA
Load Capacitance (C_{load})	2 nF
Quiescent Current ($I_{quiescent}$)	50 μ A
Transient Duration	10 μ s

2. Purpose of an LDO

An LDO (Low-Dropout Regulator) is a type of linear voltage regulator used to maintain a stable output voltage from a varying input voltage with minimal voltage drop. It is particularly important in applications where a steady and reliable power supply is crucial for the proper operation of electronic devices.

- **Stable Voltage Output:**

Provides a consistent and regulated output voltage despite fluctuations in the input voltage, ensuring reliable operation of sensitive electronic circuits.

- **Noise Filtering:**

Reduces power supply noise, contributing to better performance in analog circuits and reducing interference in sensitive applications like RF modules and audio systems.

- **Simplicity and Cost-Effectiveness:**

Requires minimal external components, making it a simpler and often more cost-effective solution compared to switching regulators for low-power applications.

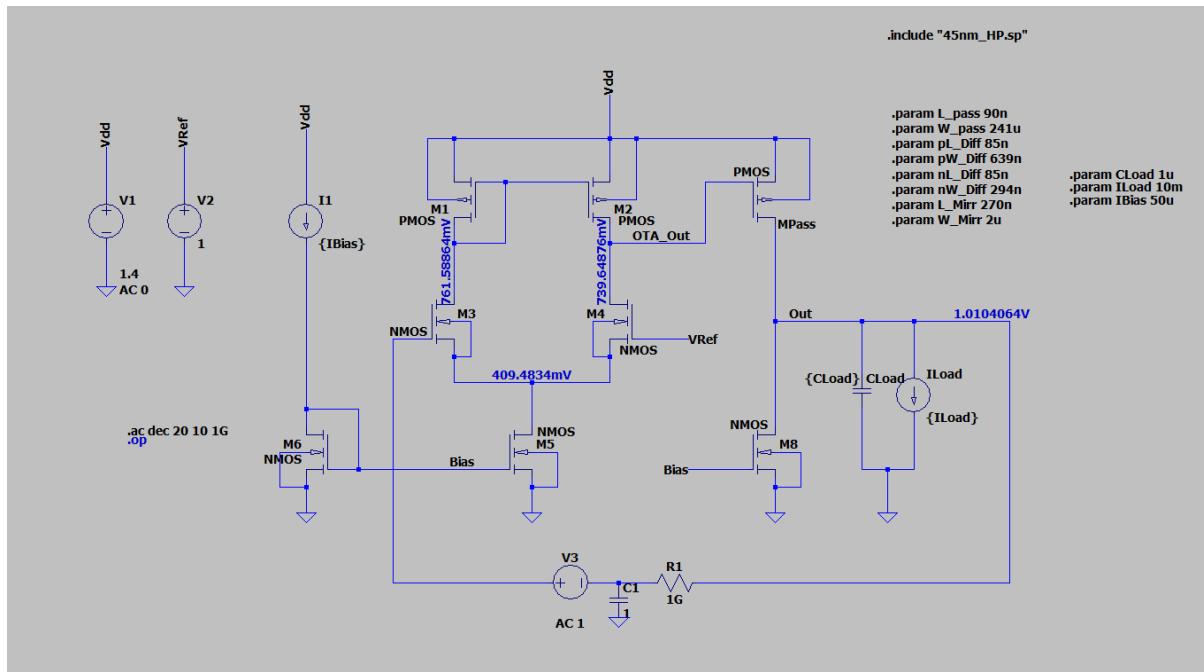


Figure 1: Our LDO schematic

3. Relevance of Techplots

Schematic: The following schematic shows how the techplots were obtained.

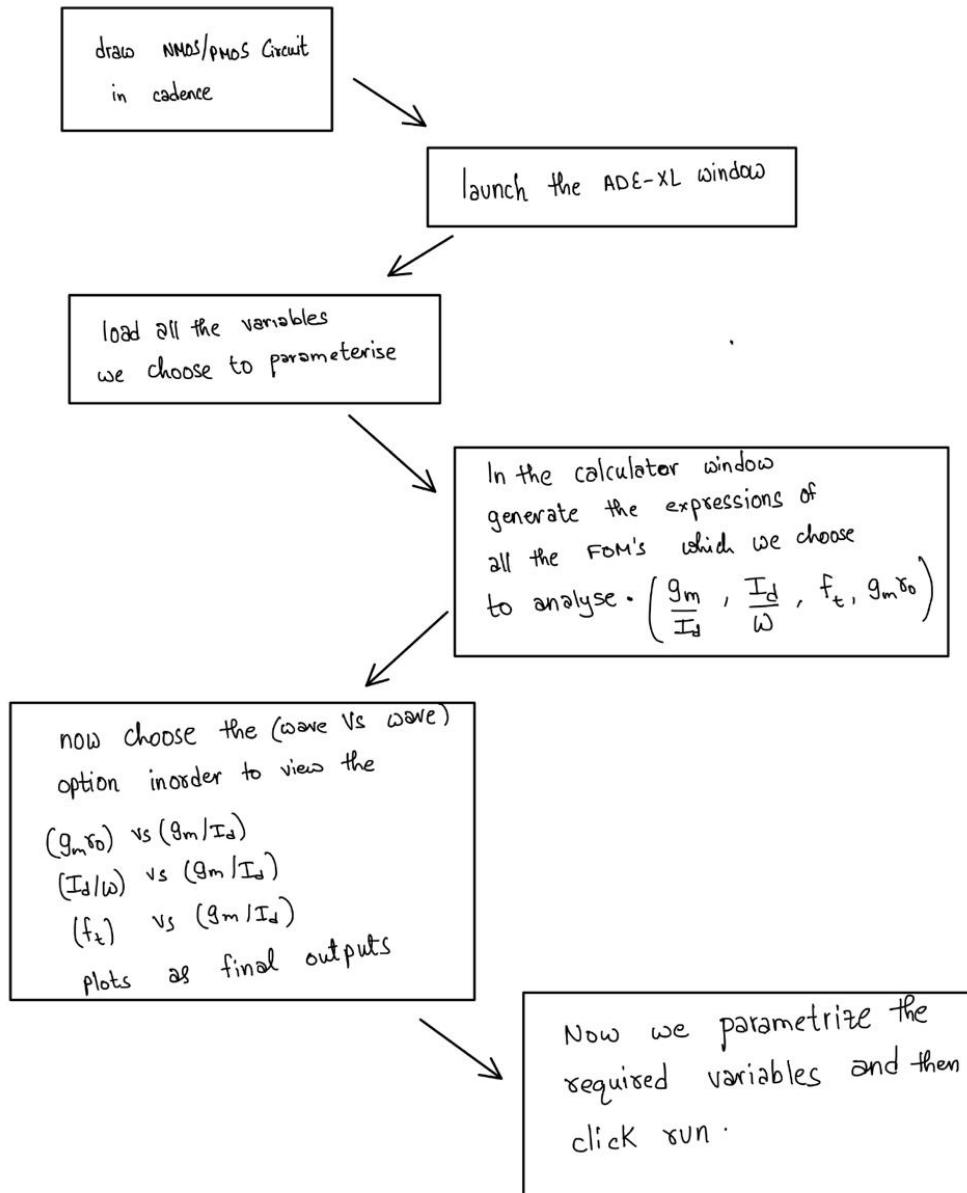


Figure 2: Schematic for generating techplots.

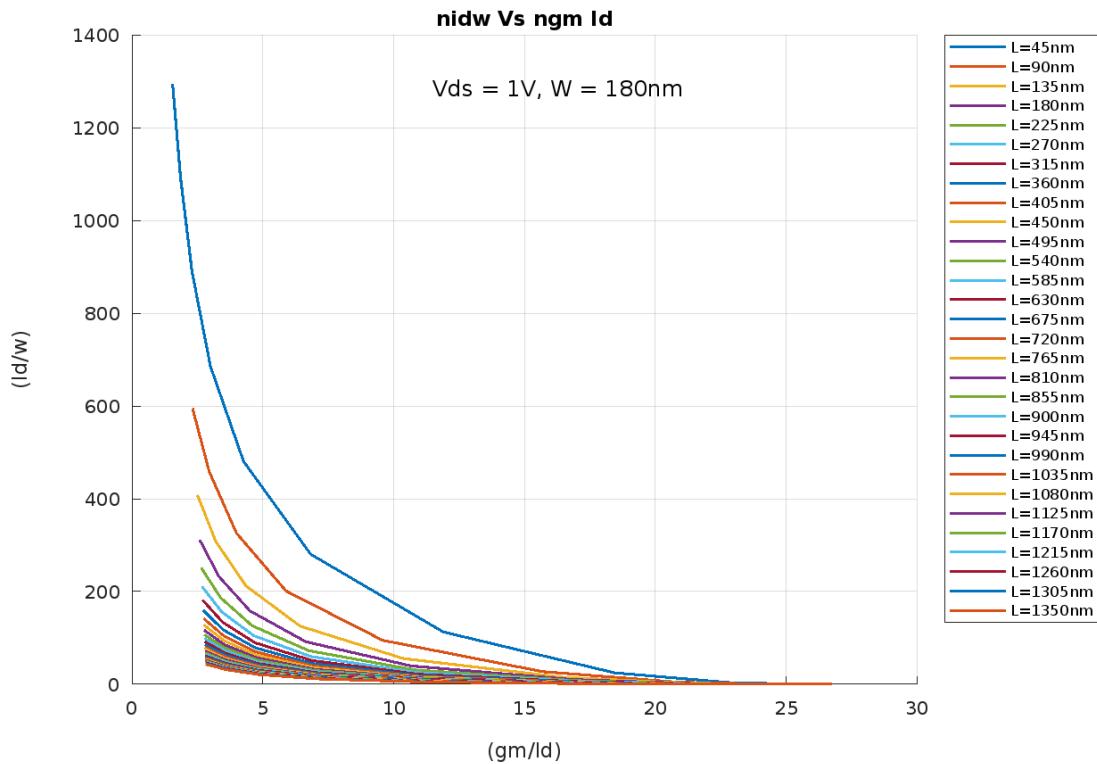
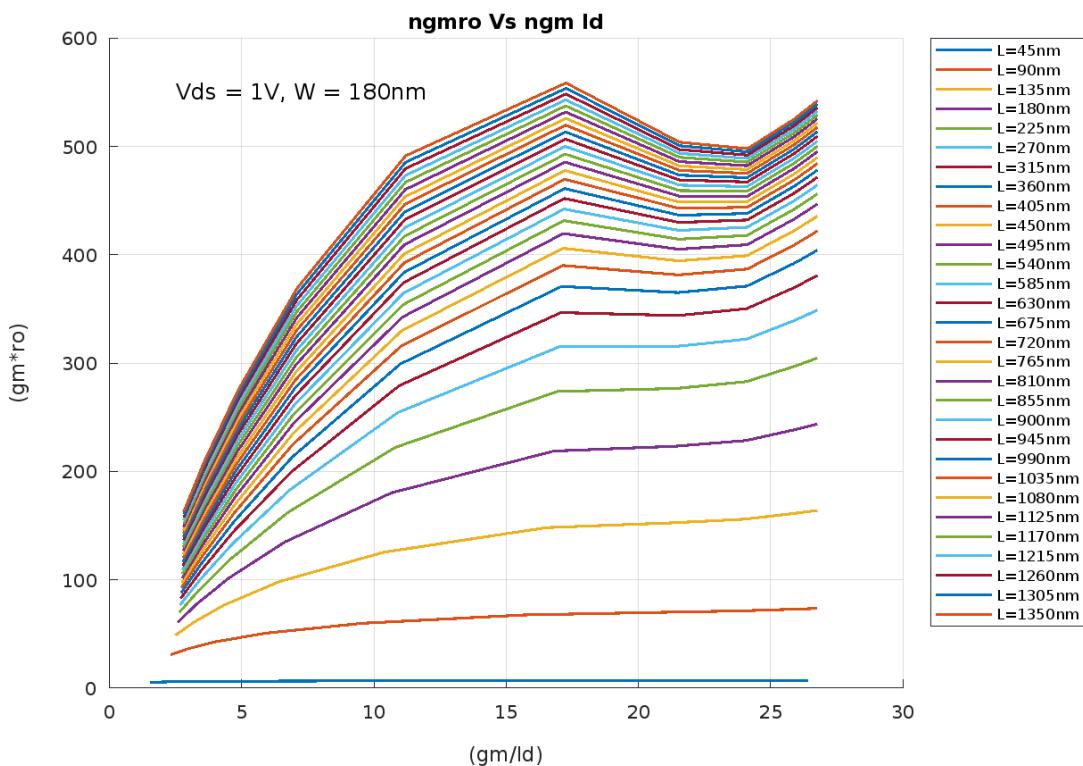
Figure 3: NMOS Techplots after Matlab postprocessing - Id/W 

Figure 4: NMOS Techplots after Matlab postprocessing - gmro

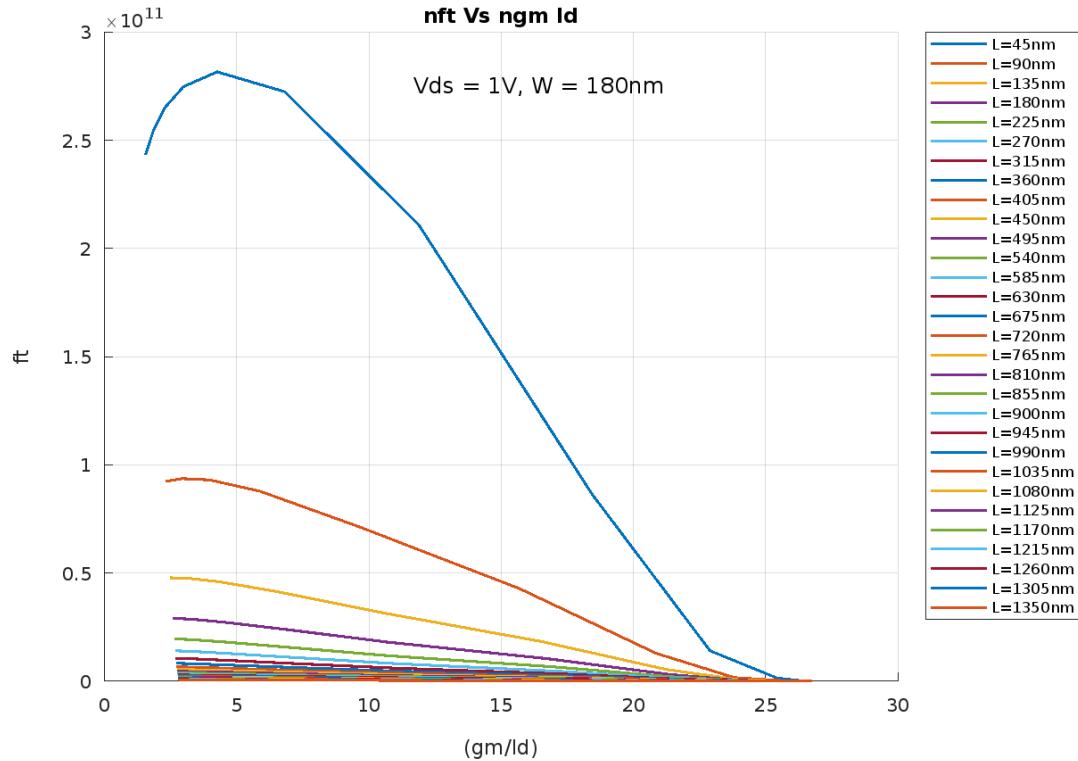


Figure 5: NMOS Techplots after Matlab postprocessing - fT

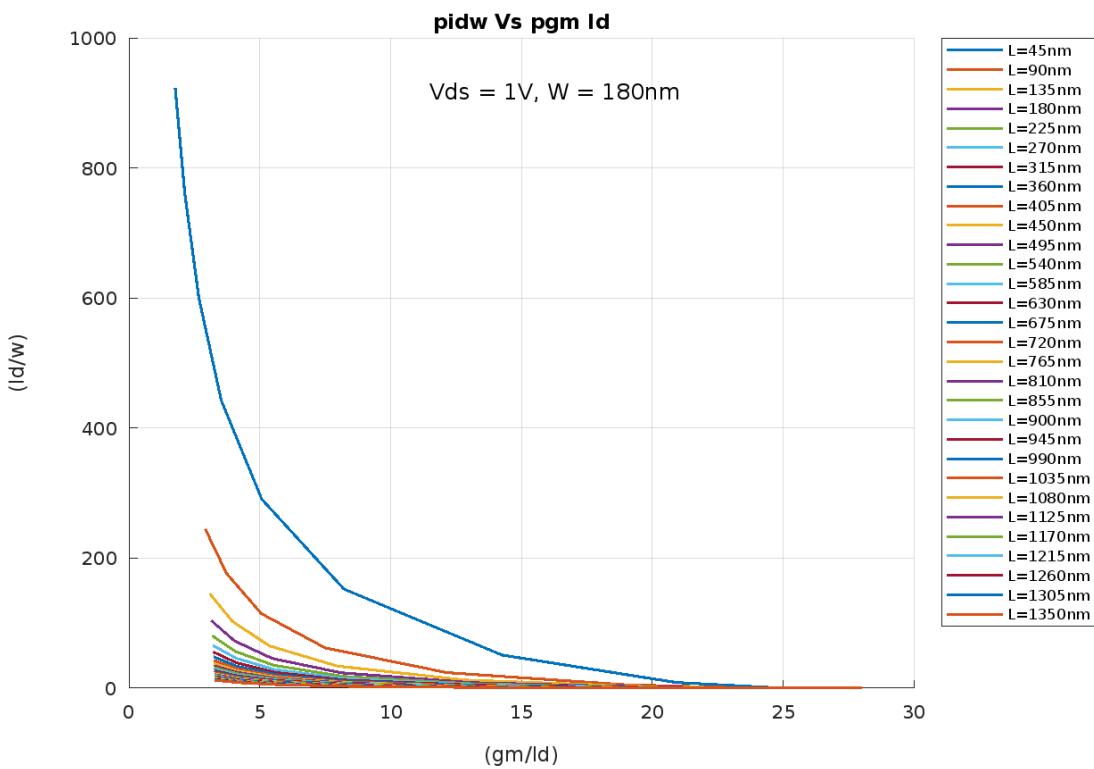


Figure 6: PMOS Techplots after Matlab postprocessing - Id/W

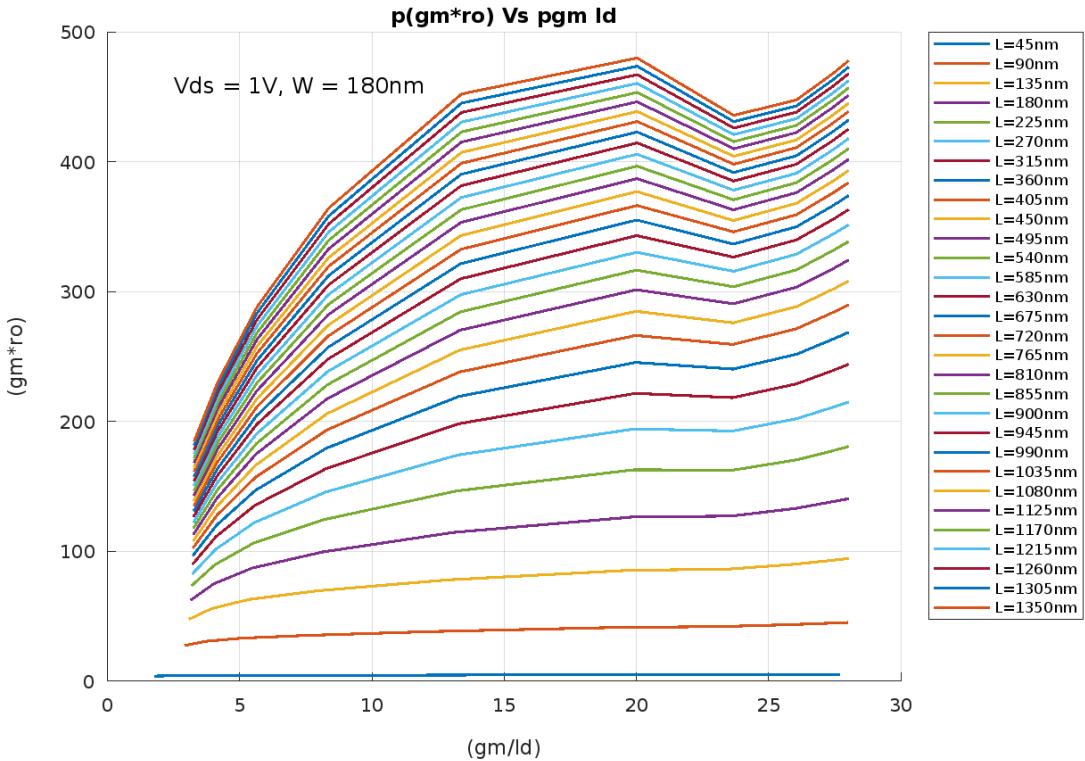


Figure 7: PMOS Techplots after Matlab postprocessing - gmro

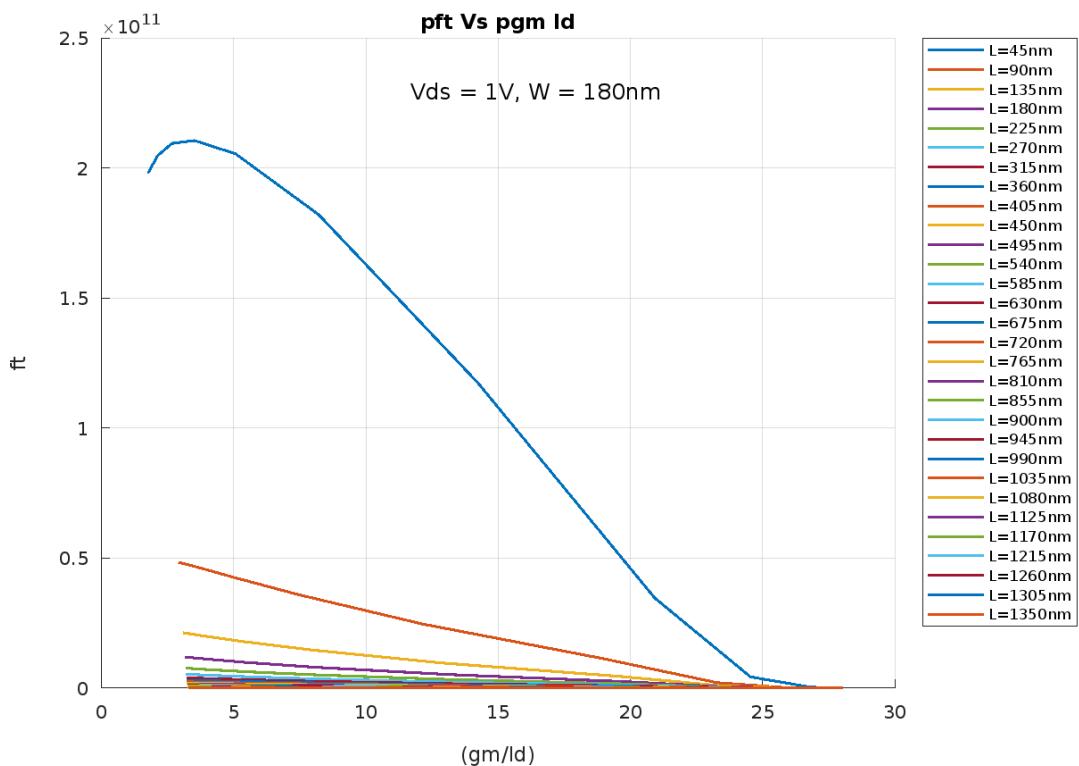


Figure 8: PMOS Techplots after Matlab postprocessing - fT

Table 3: Key Differences between 180 nm and (90nm and 135nm) of 45nmHP pdk

Parameter	180nm	135nm	90nm
gmro	33	73.125	36.8
id/w	8.83	24.86	41.38
ft(GHz)	6.5	12.6	29.8

Some of the key takeaways from the above table are as follows.

- If you observe f_T , It improves with shorter channel lengths, making circuits faster with scaling.
- Compared to 180 nm the FOMs of 135nm is x2 and that of 90nm is x5.
- All the transistors in the design are in saturation.

4. FET Sizes

90nm(Heavy Load): The following table shows the sizes of the passFET, differential amplifier, and mirror transistors. The Load current I_d is taken as 10mA.

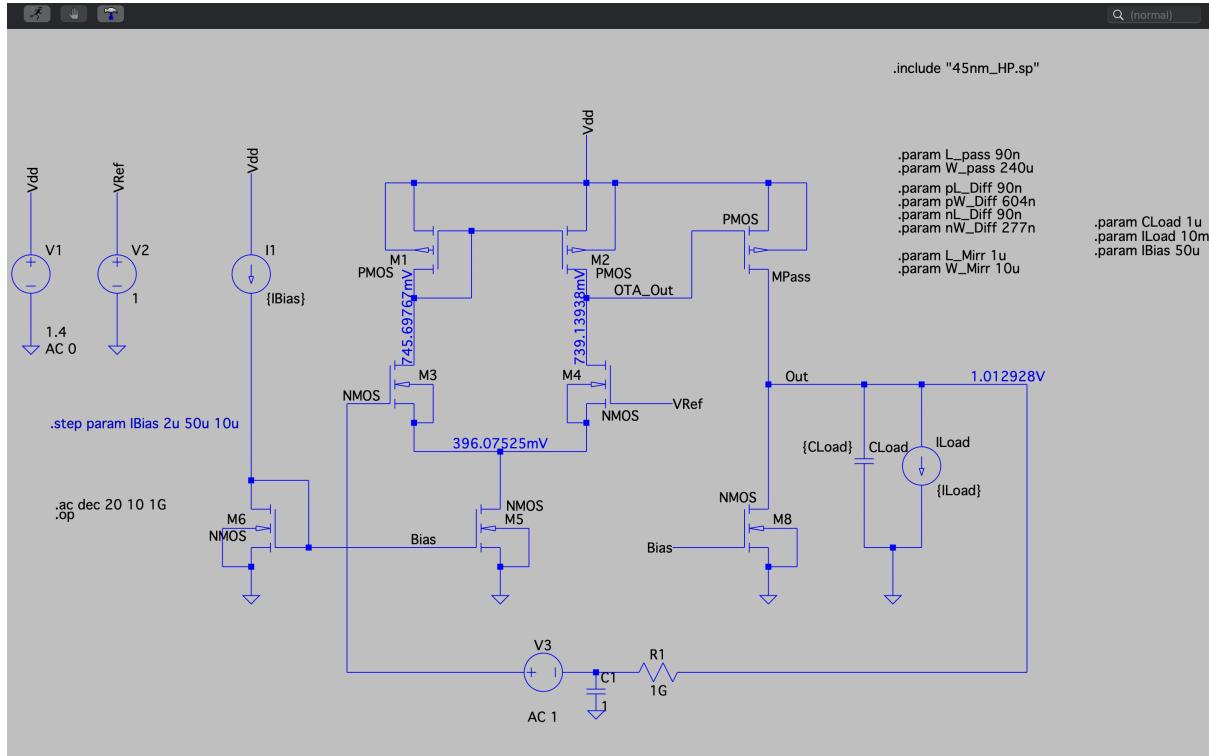


Figure 9: LDO design for 90nm Heavy Load.

Table 4: Hand Calculated FET Sizes for FOM's (gmro, id/w, gm/id and ft)

Transistor	gmro	id/w	gm/id	ft(GHz)
PassFET	36.8	41.28	10	29.8
DiffAmp Input	54.34	89.96	10	69.5
PMOS Load	54.34	41.38	10	29.8

If you observe table 4 you can see that loop gain of passfet is 36.8. So we can calculate the gain of load and diff-inp from the following method.

$$A_{loop} = A_{diff} \times A_{pass}$$

$$A_{loop} = 1000$$

$$A_{pass} = 36.8$$

for a differential amplifier we know that

$$A_{diff} = g_m (\tau_{op} \parallel \tau_{on}) = \frac{g_m \tau_0}{2}$$

$$A_{diff} = \frac{1000}{36.8} = 27.17$$

$$g_m \tau_0 = 54.34$$

So $g_m \tau_0$ of Diff-Amp and PMOS load is 54.34

Table 5: Hand Calculated FET Sizes (Length and Width)

Transistor	Length	Width	Area(μm^2)
PassFET	90n	241u	21.6
DiffAmp Input	90n	277n	0.0249
PMOS Load	90n	604n	0.0546
Mirror Transistors	1u	10u	10

```
Circuit: * /Users/karthikeyavadlamudi/Desktop/project_acmos/External_compensated/90nm/Heavy Load/90_LD0.asc
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m3      m4      m5      m6      m8
Model:    nmos    nmos    nmos    nmos    nmos
Id:   2.48e-05  2.49e-05  4.97e-05  5.00e-05  5.06e-05
Vgs:   6.03e-01  6.04e-01  5.76e-01  5.76e-01  5.76e-01
Vds:   3.50e-01  3.43e-01  3.96e-01  5.76e-01  1.01e+00
Vbs:   0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
Vth:   4.66e-01  4.66e-01  4.69e-01  4.69e-01  4.69e-01
Vdsat: 1.44e-01  1.45e-01  1.33e-01  1.33e-01  1.33e-01
Gm:   2.41e-04  2.41e-04  6.24e-04  6.28e-04  6.34e-04
Gds:   5.17e-06  5.28e-06  1.98e-06  1.54e-06  1.35e-06
Gmb:   5.56e-05  5.57e-05  1.44e-04  1.44e-04  1.46e-04
Cbd:   1.25e-16  1.26e-16  4.48e-15  4.30e-15  3.97e-15
Cbs:   2.22e-16  2.22e-16  8.00e-15  8.00e-15  8.00e-15

Name:      m1      m2      mpass
Model:    pmos    pmos    pmos
Id:   -2.48e-05 -2.48e-05 -1.01e-02
Vgs:   -6.54e-01 -6.54e-01 -6.61e-01
Vds:   -6.54e-01 -6.61e-01 -3.87e-01
Vbs:   0.00e+00  0.00e+00  0.00e+00
Vth:   -4.84e-01 -4.84e-01 -4.87e-01
Vdsat: -1.83e-01 -1.84e-01 -1.86e-01
Gm:   2.36e-04  2.36e-04  9.36e-02
Gds:   4.83e-06  4.82e-06  2.50e-03
Gmb:   5.00e-05  5.01e-05  1.99e-02
Cbd:   2.56e-16  2.55e-16  1.08e-13
Cbs:   4.83e-16  4.83e-16  1.92e-13
```

Figure 10: DC operating points for 90nm Heavy Load.

Table 6: Hand Calculated DC operating Points (g_m , r_o , $g_m r_o$ (from spicelog G_m/G_{ds}),and i_d)

Transistor	g_m	r_o	$g_m r_o$	i_d
PassFET	0.1	368	37.44	0.01
DiffAmp Input	0.000025	217391	46.61 — 45.64	0.00025
PMOS Load	0.000025	217391	48.86 — 48.96	0.00025

Table 7: Transistor Parameters and Operating Regions

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1(load)	PMOS	0.654	0.654	0.484	0.170	Saturation
M2(load)	PMOS	0.661	0.654	0.484	0.170	Saturation
MPass	PMOS	0.387	0.661	0.487	0.195	Saturation
M3(diffinp)	NMOS	0.35	0.604	0.466	0.138	Saturation
M4(diffinp)	NMOS	0.343	0.604	0.466	0.138	Saturation
M5	NMOS	0.396	0.576	0.469	0.107	Saturation
M6	NMOS	0.576	0.576	0.469	0.107	Saturation
M8	NMOS	1.01	0.576	0.469	0.107	Saturation

90nm(Low Load): The following table shows the sizes of the passFET, differential amplifier, and mirror transistors. The Load current Id is taken as 2mA.

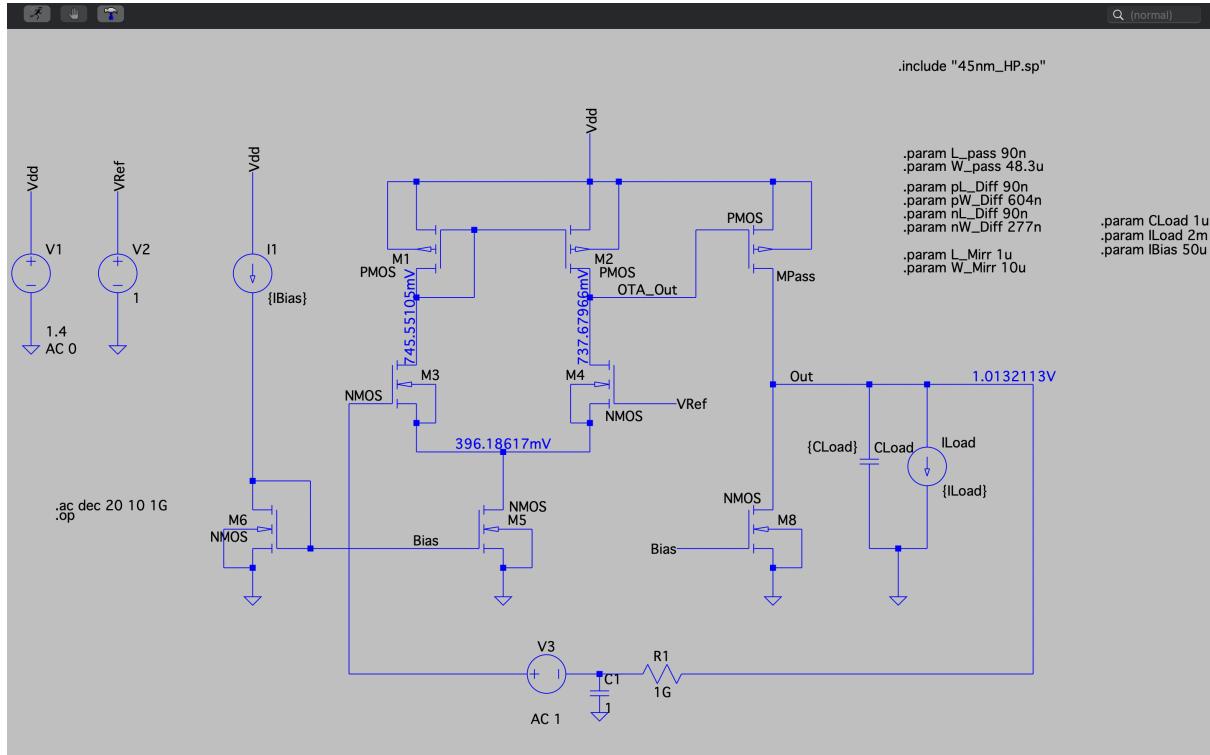


Figure 11: LDO design for 90nm Light Load.

Table 8: Hand Calculated FET Sizes for FOM's (gmro, id/w, gm/id and ft)

Transistor	gmro	id/w	gm/id	ft(GHz)
PassFET	36.8	41.28	10	29.8
DiffAmp Input	54.34	89.96	10	69.5
PMOS Load	54.34	41.38	10	29.8

If you observe table 8 you can see that loop gain of passfet is 36.8.

$$A_{loop} = A_{diff} \times A_{pass}$$

$$A_{loop} = 1000$$

$$A_{pass} = 36.8$$

for a differential amplifier we know that

$$A_{diff} = g_m (\tau_{op} \parallel \tau_{on}) = \frac{g_m \tau_0}{2}$$

$$A_{diff} = \frac{1000}{36.8} = 27.17$$

$$g_m \tau_0 = 54.34$$

So $g_m \tau_0$ of Diff-Amp and PMOS load is 54.34

Table 9: Hand Calculated FET Sizes (Length and Width)

Transistor	Length	Width	Area (μm^2)
PassFET	90n	48.3u	4.347
DiffAmp Input	90n	277n	0.0249
PMOS Load	90n	604n	0.0544
Mirror Transistors	1u	10u	10.0

```
Circuit: * /Users/karthikeyavadlamudi/Desktop/project_acmos/External_compensated/90nm/Light load/90_LDO_lowload.asc
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
--- BSIM4 MOSFETS ---
Name:      m3          m4          m5          m6          m8
Model:    nmos        nmos        nmos        nmos        nmos
Id:      2.48e-05   2.49e-05   4.97e-05   5.00e-05   5.06e-05
Vgs:     6.03e-01   6.04e-01   5.76e-01   5.76e-01   5.76e-01
Vds:     3.49e-01   3.41e-01   3.96e-01   5.76e-01   1.01e+00
Vbs:     0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00
Vth:     4.66e-01   4.66e-01   4.69e-01   4.69e-01   4.69e-01
Vdsat:   1.44e-01   1.45e-01   1.33e-01   1.33e-01   1.33e-01
Gm:      2.41e-04   2.41e-04   6.24e-04   6.28e-04   6.34e-04
Gds:     5.18e-06   5.30e-06   1.98e-06   1.54e-06   1.35e-06
Gmb:     5.56e-05   5.56e-05   1.44e-04   1.44e-04   1.46e-04
Cbd:     1.25e-16   1.26e-16   4.48e-15   4.30e-15   3.97e-15
Cbs:     2.22e-16   2.22e-16   8.00e-15   8.00e-15   8.00e-15

Name:      m1          m2          mpass
Model:    pmos        pmos        pmos
Id:      -2.48e-05  -2.48e-05  -2.05e-03
Vgs:     -6.54e-01  -6.54e-01  -6.62e-01
Vds:     -6.54e-01  -6.62e-01  -3.87e-01
Vbs:     0.00e+00   0.00e+00   0.00e+00
Vth:     -4.84e-01  -4.84e-01  -4.87e-01
Vdsat:   -1.84e-01  -1.84e-01  -1.87e-01
Gm:      2.36e-04   2.36e-04   1.90e-02
Gds:     4.83e-06   4.82e-06   5.09e-04
Gmb:     5.01e-05   5.01e-05   4.04e-03
Cbd:     2.56e-16   2.55e-16   2.17e-14
Cbs:     4.83e-16   4.83e-16   3.86e-14
```

Figure 12: DC operating points for 90nm Light Load.

Table 10: Hand Calculated DC operating Points (g_m , r_o , $g_m r_o$, i_d)

Transistor	g_m	r_o	$g_m r_o$	i_d
PassFET	0.02	1840	37.3	0.002
DiffAmp Input	0.000025	217391	46.52 — 45.47	0.00025
PMOS Load	0.000025	217391	48.86 — 48.96	0.00025

Table 11: Transistor Parameters and Operating Regions

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1 (load)	PMOS	0.654	0.654	0.484	0.170	Saturation
M2 (load)	PMOS	0.662	0.654	0.484	0.170	Saturation
MPass	PMOS	0.387	0.662	0.487	0.175	Saturation
M3 (diff-inp)	NMOS	0.349	0.603	0.466	0.137	Saturation
M4 (diff-inp)	NMOS	0.341	0.604	0.466	0.138	Saturation
M5	NMOS	0.396	0.576	0.469	0.107	Saturation
M6	NMOS	0.576	0.576	0.469	0.107	Saturation
M8	NMOS	1.010	0.576	0.469	0.107	Saturation

The final deduction from 90nm Heavy load and Light load is that only the parameters of PassFET are changing.

Light Load uses Less Area compared to Heavy Load.

135nm(Heavy Load): The following table shows the sizes of the passFET, differential amplifier, and mirror transistors. The Load current Id is taken as 10mA.

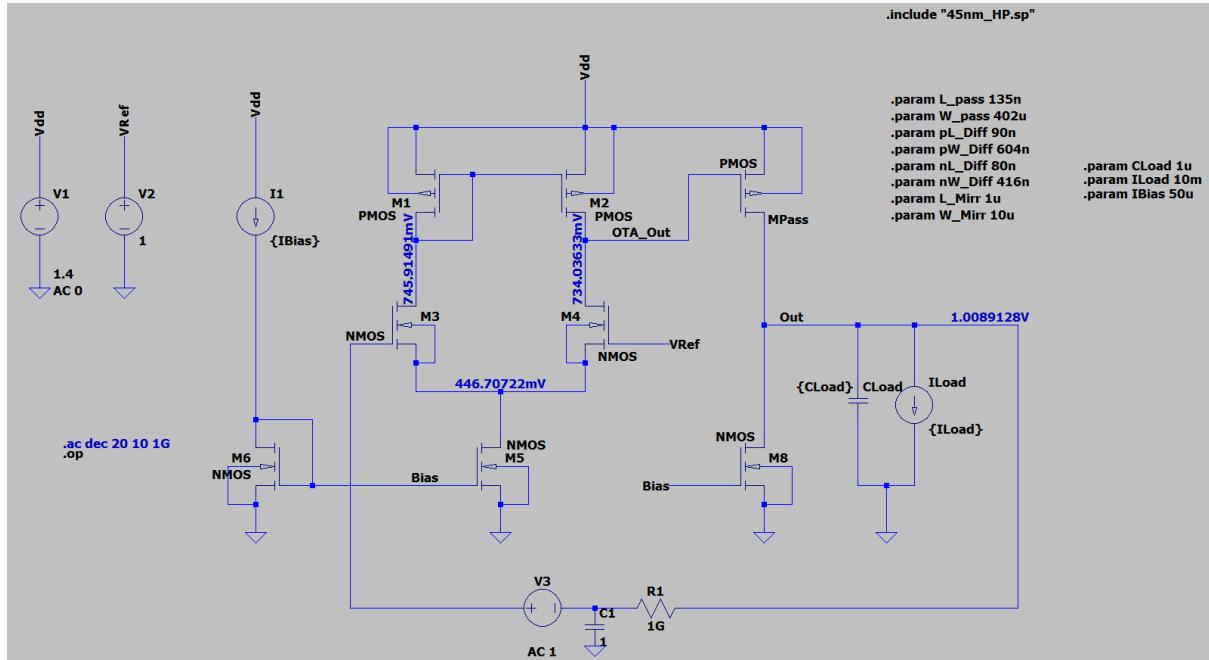


Figure 13: LDO design for 135nm Heavy Load.

Table 12: FET Sizes for FOM's (gmro, id/w, gm/id and ft)

Transistor	gmro	id/w	gm/id	ft(GHz)
PassFET	73.125	24.86	10	12.6
DiffAmp Input	27.35	60	10	32.8
PMOS Load	27.35	41.38	10	12.6

If you observe table 12 you can see that loop gain of passfet is 73.125.

$$A_{\text{loop}} = A_{\text{diff}} \times A_{\text{pass}}$$

$$A_{\text{loop}} = 1000$$

$$A_{\text{pass}} = 73.125$$

for a differential amplifier we know that

$$A_{\text{diff}} = g_m (\tau_{\text{op}} \parallel \tau_{\text{on}}) = \frac{g_m \tau_0}{2}$$

$$A_{\text{diff}} = \frac{1000}{73.125} = 13.675$$

$$g_m \tau_0 = 27.35$$

So $g_m \tau_0$ of Diff-Amp and PMOS load is 27.35

Table 13: Hand Calculated FET Sizes (Length and Width)

Transistor	Length	Width	Area(μm^2)
PassFET	135n	402u	54.27
DiffAmp Input	80n	416n	0.03328
PMOS Load	90n	604n	0.05436
mirror transistors	1u	10u	10

```

LTspice 24.0.12 for Windows
Circuit: * C:\Users\rohit\Desktop\project_acmos\project_acmos\External_compensated\135nm\Heavy Load\135_LDO.asc
Start Time: Tue Dec 3 23:12:59 2024
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:     m3      m4      m5      m6      m8
Model:   nmos    nmos    nmos    nmos    nmos
Id:      2.47e-05 2.51e-05 4.98e-05 5.00e-05 5.06e-05
Vgs:      5.52e-01 5.53e-01 5.76e-01 5.76e-01 5.76e-01
Vds:      2.99e-01 2.87e-01 4.47e-01 5.76e-01 1.01e+00
Vbs:      0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00
Vth:      4.65e-01 4.65e-01 4.69e-01 4.69e-01 4.69e-01
Vdsat:    1.12e-01 1.12e-01 1.33e-01 1.33e-01 1.33e-01
Gm:       3.07e-04 3.09e-04 6.26e-04 6.28e-04 6.34e-04
Gds:       7.61e-06 7.92e-06 1.77e-06 1.54e-06 1.35e-06
Gmb:       6.94e-05 6.99e-05 1.44e-04 1.44e-04 1.46e-04
Cbd:      1.91e-16 1.91e-16 4.43e-15 4.30e-15 3.97e-15
Cbs:      3.33e-16 3.33e-16 8.00e-15 8.00e-15 8.00e-15

Name:     m1      m2      mpass
Model:   pmos    pmos    pmos
Id:      -2.47e-05 -2.48e-05 -1.01e-02
Vgs:      -6.54e-01 -6.54e-01 -6.66e-01
Vds:      -6.54e-01 -6.66e-01 -3.91e-01
Vbs:      0.00e+00 0.00e+00 0.00e+00
Vth:      -4.84e-01 -4.84e-01 -4.90e-01
Vdsat:    -1.83e-01 -1.83e-01 -1.89e-01
Gm:       2.35e-04 2.36e-04 9.48e-02
Gds:       4.82e-06 4.81e-06 1.38e-03
Gmb:       5.00e-05 5.01e-05 2.01e-02
Cbd:      2.56e-16 2.55e-16 1.80e-13
Cbs:      4.83e-16 4.83e-16 3.22e-13

```

Figure 14: DC operating points for 135nm Heavy Load.

Table 14: Hand Calculated DC operating Points (g_m , r_o , $g_m r_o$ (from spicelog G_m/G_{ds}), and i_d)

Transistor	g_m	r_o	$g_m r_o$	i_d
PassFET	0.1	731	68.11	0.01
DiffAmp Input	0.000025	109401	40.34 — 39.01	0.00025
PMOS Load	0.000025	109401	48.75 — 49.06	0.00025

Table 15: Transistor Parameters and Operating Regions

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1 (load)	PMOS	0.648	0.648	0.484	0.164	Saturation
M2 (load)	PMOS	0.653	0.648	0.484	0.164	Saturation
MPass	PMOS	0.391	0.666	0.490	0.176	Saturation
M3 (diffinp)	NMOS	0.299	0.552	0.465	0.087	Saturation
M4 (diffinp)	NMOS	0.299	0.552	0.465	0.087	Saturation
M5	NMOS	0.447	0.576	0.469	0.107	Saturation
M6	NMOS	0.576	0.576	0.469	0.107	Saturation
M8	NMOS	1.01	0.576	0.469	0.107	Saturation

135nm(Low Load): The following table shows the sizes of the passFET, differential amplifier, and mirror transistors. The Load current Id is taken as 2mA.

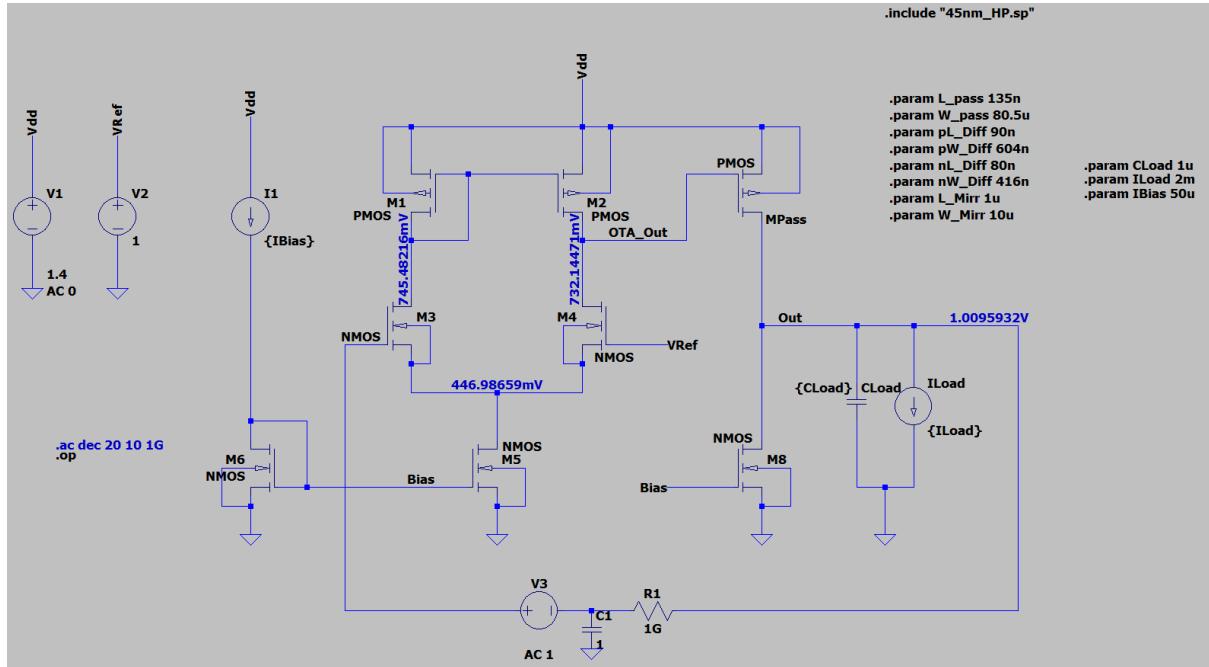


Figure 15: LDO design for 135nm Light Load.

Table 16: FET Sizes for FOM's (gmro, id/w, gm/id and ft)

Transistor	gmro	id/w	gm/id	ft(GHz)
PassFET	73.125	24.86	10	12.6
DiffAmp Input	27.35	60	10	32.8
PMOS Load	27.35	41.38	10	12.6

If you observe table 16 you can see that loop gain of passfet is 73.125.

$$A_{\text{loop}} = A_{\text{diff}} \times A_{\text{pass}}$$

$$A_{\text{loop}} = 1000$$

$$A_{\text{pass}} = 73.125$$

for a differential amplifier we know that

$$A_{\text{diff}} = g_m (\tau_{\text{op}} \parallel \tau_{\text{on}}) = \frac{g_m \tau_0}{2}$$

$$A_{\text{diff}} = \frac{1000}{73.125} = 13.675$$

$$g_m \tau_0 = 27.35$$

So $g_m \tau_0$ of Diff-Amp and PMOS load is 27.35

Table 17: Hand Calculated FET Sizes (Length and Width)

Transistor	Length	Width	Area(μm^2)
PassFET	135n	402u	54.27
DiffAmp Input	80n	416n	0.03328
PMOS Load	90n	604n	0.05436
mirror transistors	1u	10u	10

```

SPICE Output Log: C:\Users\rohit\Desktop\project_acmos\project_acmos\External_compensated\135nm\Light Load\135_LDO copy.log
LTspice 24.0.12 for Windows
Circuit: * C:\Users\rohit\Desktop\project_acmos\project_acmos\External_compensated\135nm\Light Load\135_LDO copy.asc
Start Time: Wed Dec 4 00:46:25 2024
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:   m3      m4      m5      m6      m8
Model: nmos    nmos    nmos    nmos    nmos
Id:    2.48e-05 2.49e-05 4.98e-05 5.00e-05 5.06e-05
Vgs:   5.52e-01 5.53e-01 5.76e-01 5.76e-01 5.76e-01
Vds:   2.98e-01 2.85e-01 4.47e-01 5.76e-01 1.01e+00
Vbs:   0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00
Vth:   4.65e-01 4.65e-01 4.69e-01 4.69e-01 4.69e-01
Vdsat: 1.12e-01 1.12e-01 1.33e-01 1.33e-01 1.33e-01
Gm:    3.08e-04 3.09e-04 6.26e-04 6.28e-04 6.34e-04
Gds:   7.65e-06 7.94e-06 1.77e-06 1.54e-06 1.35e-06
Gmb:   6.96e-05 6.97e-05 1.44e-04 1.44e-04 1.46e-04
Cbd:   1.91e-16 1.91e-16 4.43e-15 4.30e-15 3.97e-15
Cbs:   3.33e-16 3.33e-16 8.00e-15 8.00e-15 8.00e-15

Name:   m1      m2      mpass
Model: pmos   pmos   pmos
Id:    -2.48e-05 -2.49e-05 -2.05e-03
Vgs:   -6.55e-01 -6.55e-01 -6.68e-01
Vds:   -6.55e-01 -6.68e-01 -3.90e-01
Vbs:   0.00e+00 0.00e+00 0.00e+00
Vth:   -4.84e-01 -4.84e-01 -4.90e-01
Vdsat: -1.84e-01 -1.84e-01 -1.90e-01
Gm:    2.36e-04 2.36e-04 1.92e-02
Gds:   4.83e-06 4.82e-06 2.82e-04
Gmb:   5.01e-05 5.02e-05 4.07e-03
Cbd:   2.56e-16 2.55e-16 3.61e-14
Cbs:   4.83e-16 4.83e-16 6.44e-14

```

Figure 16: DC operating points for 135nm Light Load.

Table 18: FET Sizes and Parameters (Length, Width, gm, ro, id)

Transistor	g_m	r_o	$g_m r_o$	i_d
PassFET	0.02	3660	68.08	0.002
DiffAmp Input	0.000025	109401	40.26 — 38.91	0.00025
PMOS Load	0.000025	109401	48.86 — 48.96	0.00025

Table 19: Transistor Parameters and Operating Regions

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1(load)	PMOS	0.655	0.655	0.484	0.171	Saturation
M2(load)	PMOS	0.661	0.661	0.484	0.177	Saturation
MPass	PMOS	0.391	0.668	0.490	0.178	Saturation
M3(diffinp)	NMOS	0.298	0.552	0.466	0.086	Saturation
M4(diffinp)	NMOS	0.298	0.552	0.466	0.086	Saturation
M5	NMOS	0.447	0.576	0.469	0.107	Saturation
M6	NMOS	0.576	0.576	0.469	0.107	Saturation
M8	NMOS	1.01	0.576	0.469	0.107	Saturation

The final deduction from 135nm Heavy load and Light load is that only the parameters of PassFET are changing.

Light Load uses Less Area compared to Heavy Load.

5. Stability Analysis

90nm:

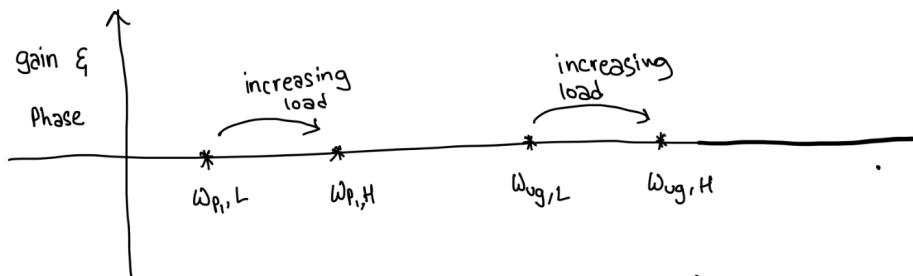
- w_{p1} would be located at a position where there is a 3dB drop from the peak
 $w_{p1} = 1/(r_{o_{pass}} * C_{Load})$
- w_{p2} can be found at the position where phase margin is 45 degrees or 135 deg drop from the initial phase.
 $w_{p2} = 1/(r_{o_{diff}} * C_{g_{load}})$
- w_{ugb} would be located at the place where the gain is 0.
 $w_{ugb} = (g_{m_{pass}} * A_{diff})/C_{load}$
- Phase margin is $180^\circ - \text{phase at } w_{ugb}$.
- General take from the plots: w_{ugb} is less than w_{p2} .

Table 20: Simulation Key Metrics under Heavy and Light Load Conditions for 90nm

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	57.97	58.57
Unity Gain Bandwidth(KHz)	324	70
Phase Margin (degrees)	84.3	89.82
Pole 1 (Hz)	409	82.8
Pole 2 (Hz)	3.09MHz	14.5MHz

Table 21: Hand Calculated Key Metrics under Heavy and Light Load Conditions for 90nm

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	60	60
Unity Gain Bandwidth	2.72 MHz	543 KHz
Pole 1 (Hz)	411	86.5



worst phase margin when
Heavy load.

$$\phi_{HL} = 84.3$$

$$\phi_{LL} = 89.82$$

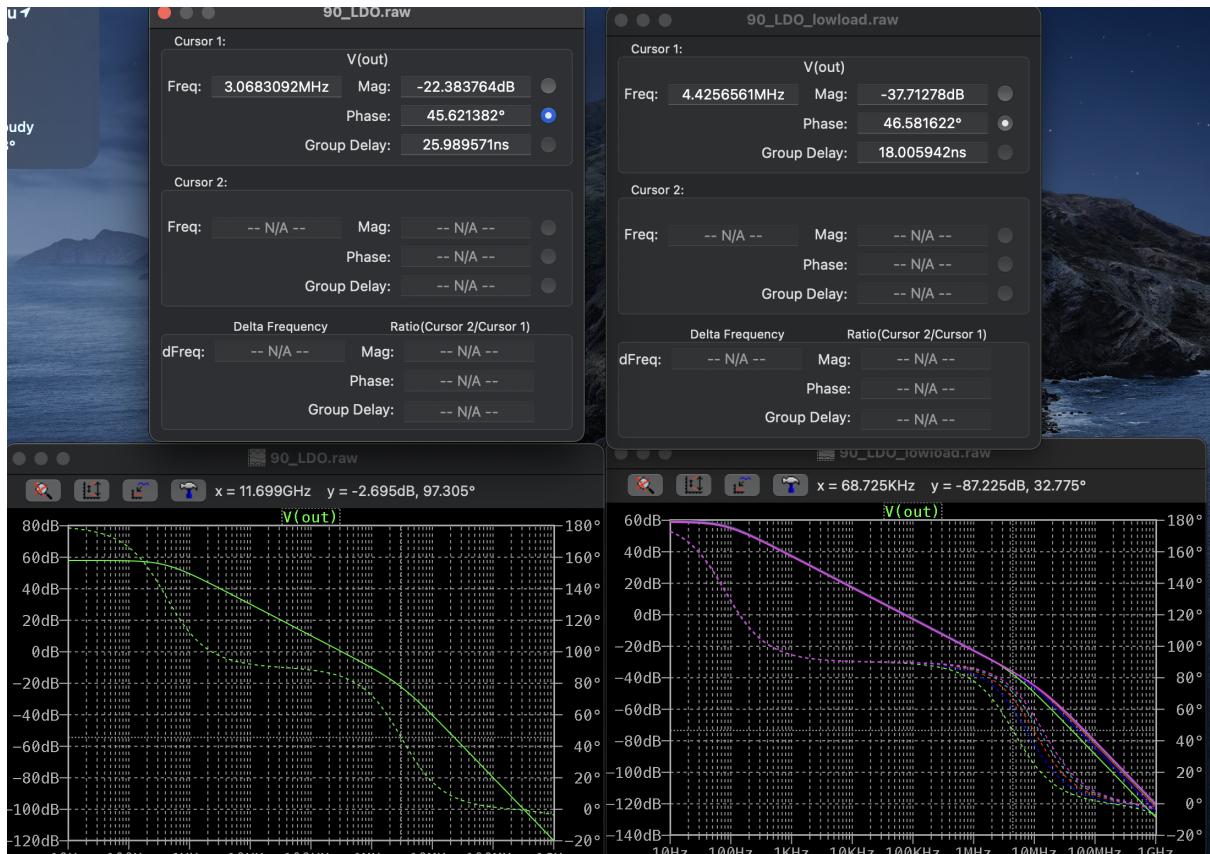


Figure 17: Stability analysis plot.

If you look at the equation of ω_p we are supposed to get the same value for light load and heavy load but since the gm/id is fixed we won't have the freedom to control the value of r_{odiff} , hence the variation in the values of ω_p values. In order to rectify that we can parameterize the value of I_{bias} in order to get the same ω_p .

135nm:

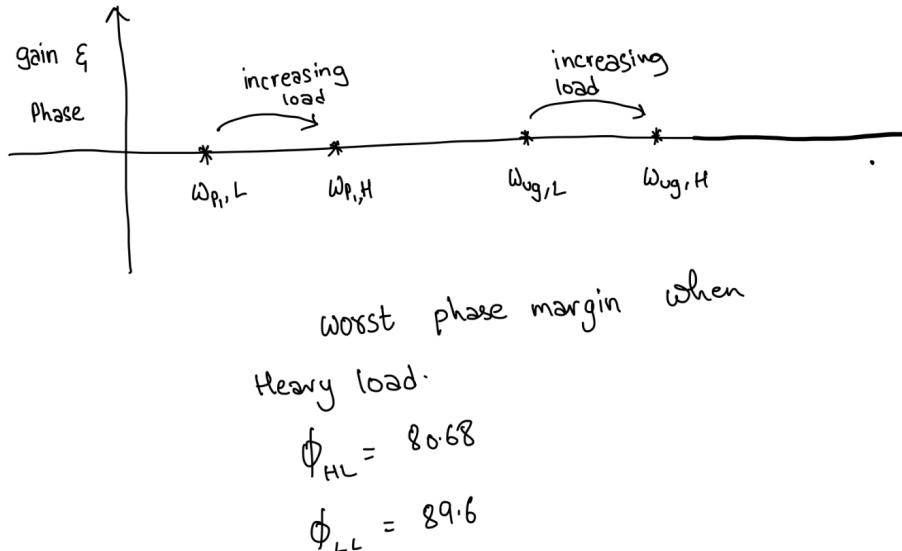
- w_{p1} would be located at a position where there is a 3dB drop from the peak
 $w_{p1} = 1/(r_{o_{pass}} * C_{Load})$
- w_{p2} can be found at the position where phase margin is 45 degrees or 135 deg drop from the initial phase.
 $w_{p2} = 1/(r_{o_{diff}} * C_{g_{gload}})$
- w_{ugb} would be located at the place where the gain is 0.
 $w_{ugb} = (g_{m_{pass}} * A_{diff})/C_{load}$
- Phase margin is $180^\circ - \text{phase at } w_{ugb}$.
- General take from the plots: w_{ugb} is less than w_{p2} .

Table 22: Simulation Key Metrics under Heavy and Light Load Conditions for 135nm

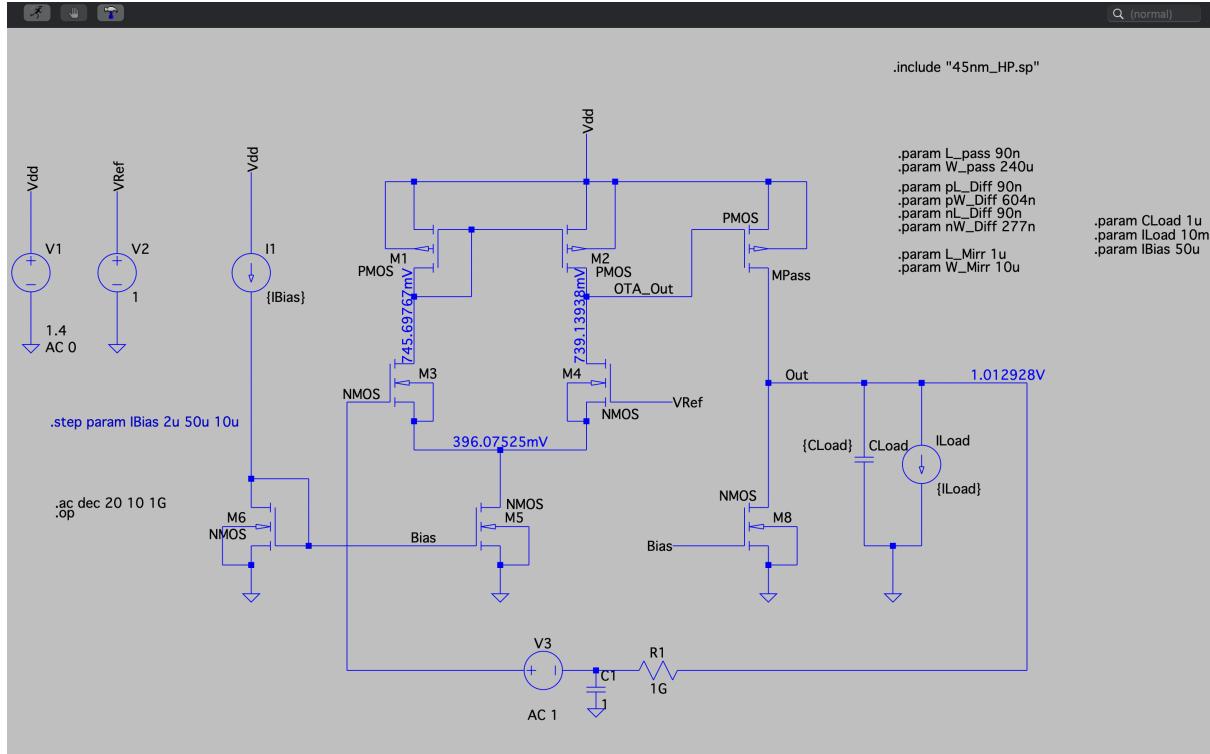
Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	62.149	63.48
Unity Gain Bandwidth (Hz)	303.3 KHz	70.47 KHz
Phase Margin (degrees)	80.68	89.6
Pole 1 (Hz)	259.7	71
Pole 2 (Hz)	1.8 MHz	7.8 MHz

Table 23: Hand Calculated Key Metrics under Heavy and Light Load Conditions for 135nm

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	60	60
Unity Gain Bandwidth (Hz)	1.37 MHz	273 KHz
Pole 1 (Hz)	218	43.5

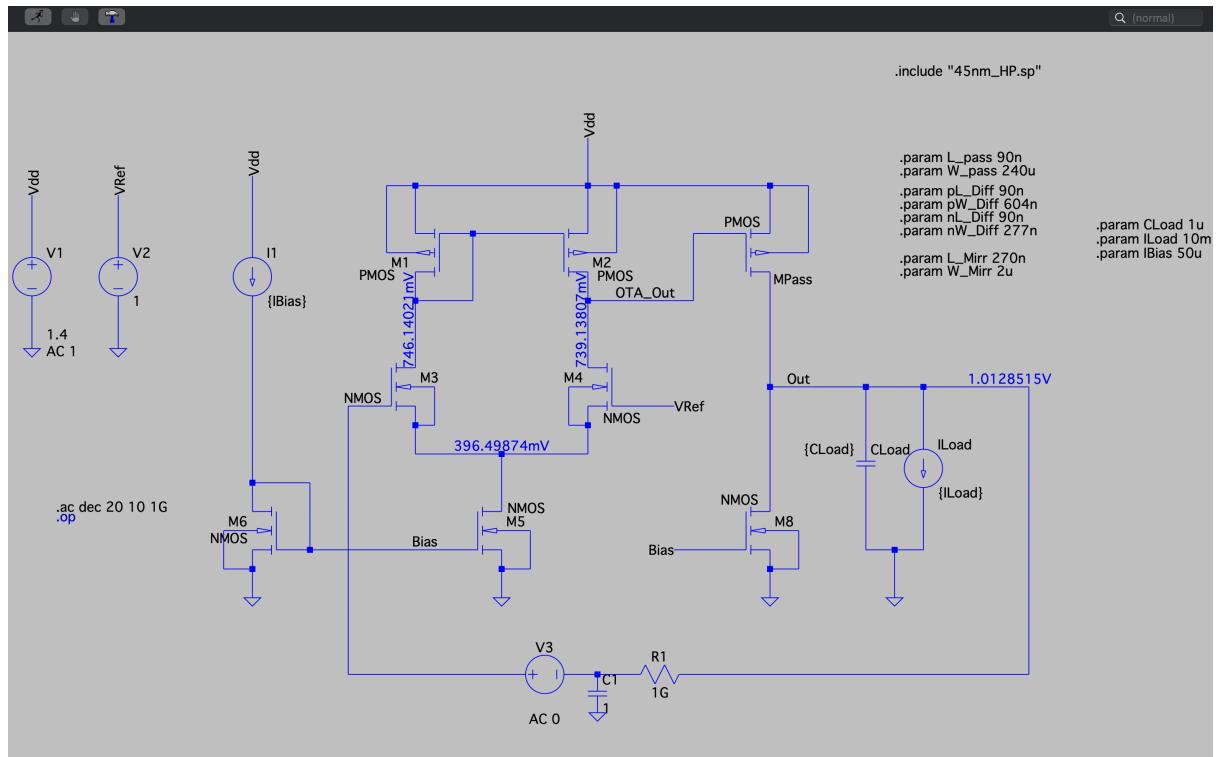


6. PSRR Explanation



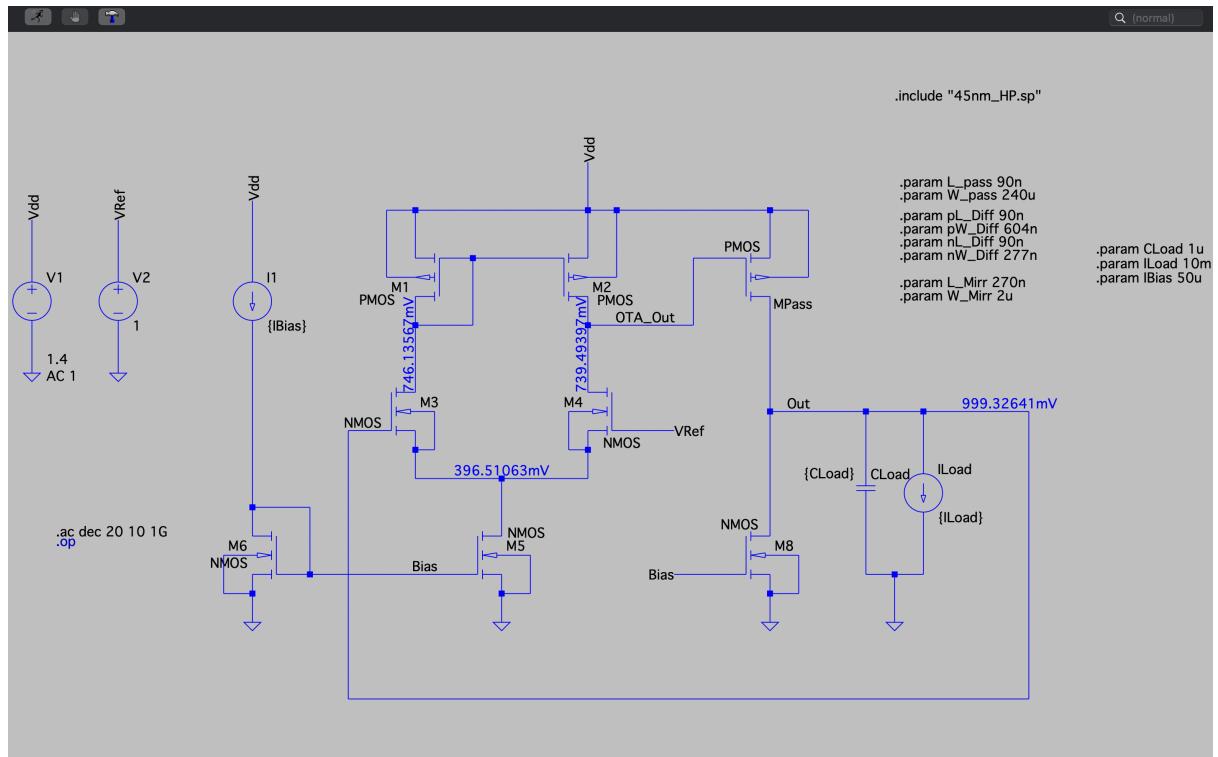
Loop Gain: In this setup, I'm using an RC circuit in the feedback loop of the Low Dropout Regulator (LDO) to separate the DC and AC signals. The RC network allows me to bias the gate of the NMOS transistor in the differential amplifier with a DC voltage, while preventing DC current from flowing to ground. The capacitor blocks DC components but lets AC signals pass, so I can focus on the AC response for loop gain calculation. The resistor has a very high value, ensuring that the current into the gate of the NMOS transistor is negligible, which results in minimal voltage drop across it.

To calculate the loop gain, I apply an AC signal with a 1V amplitude at the output of the LDO. The RC circuit isolates the AC signals from the DC biasing, letting me measure how the system responds to small AC fluctuations. The loop gain is calculated by finding the ratio of the AC output to the AC input, which helps me understand the LDO's frequency response and stability. This method ensures that I can calculate the loop gain accurately while keeping the necessary biasing conditions for the NMOS differential amplifier.



Open Loop PSRR: To calculate the open-loop Power Supply Rejection Ratio (PSRR) of the Low Dropout Regulator (LDO), an AC signal is applied to the source of the pass transistor (passfet) and the PMOS in the differential amplifier. This AC signal represents noise from the supply voltage (VDD). The goal is to observe how much of this AC noise is rejected by the circuit, ideally leaving a clean DC output. In the case of the differential amplifier, the intention is to allow the maximum amount of AC noise to pass through, so that the output transconductance (OTA) responds with the full noise, which will then be ideally rejected by the LDO, leaving a noise-free DC output.

The RC circuit in the setup is used to bias the circuit appropriately while blocking DC components, allowing for accurate AC measurement. Since the circuit is in an open-loop configuration (no feedback), there is no mechanism to suppress the AC noise from the supply effectively. This results in a poor PSRR, meaning the noise from the power supply will not be filtered out efficiently, and the output will reflect a significant amount of the noise. The open-loop PSRR, therefore, indicates how much of the supply noise gets transferred to the output when there's no feedback to aid in noise rejection.



Close Loop PSRR: In this setup, we've applied an AC source to the VDD terminal to introduce noise into the circuit. The key objective here is to observe the negative feedback mechanism, which helps cancel out the AC noise at the output. Using small signal analysis, the circuit is designed to adjust dynamically and reject any noise coming from the power supply, ensuring that the output voltage remains stable and free from unwanted fluctuations. The feedback loop from the output to the input of the differential amplifier (diffamp) plays a crucial role in this process, enabling the circuit to suppress the noise and maintain a clean DC output.

For the closed-loop PSRR, we're aiming for a high rejection ratio, ideally 60dB, as per the specifications. This high PSRR value indicates that the circuit is effectively filtering out the noise from the supply and preventing it from affecting the output. By using the feedback path, the circuit adapts to any disturbances from the supply voltage and ensures that the output voltage stays unaffected. Achieving the desired PSRR value confirms that the circuit sizing and feedback mechanism are working properly, providing the expected noise rejection and stable performance.

7. PSRR Simulation Results

90nm Heavy Load: Provide PSRR simulation results at heavy and light load conditions. Include mathematical expressions if derived.

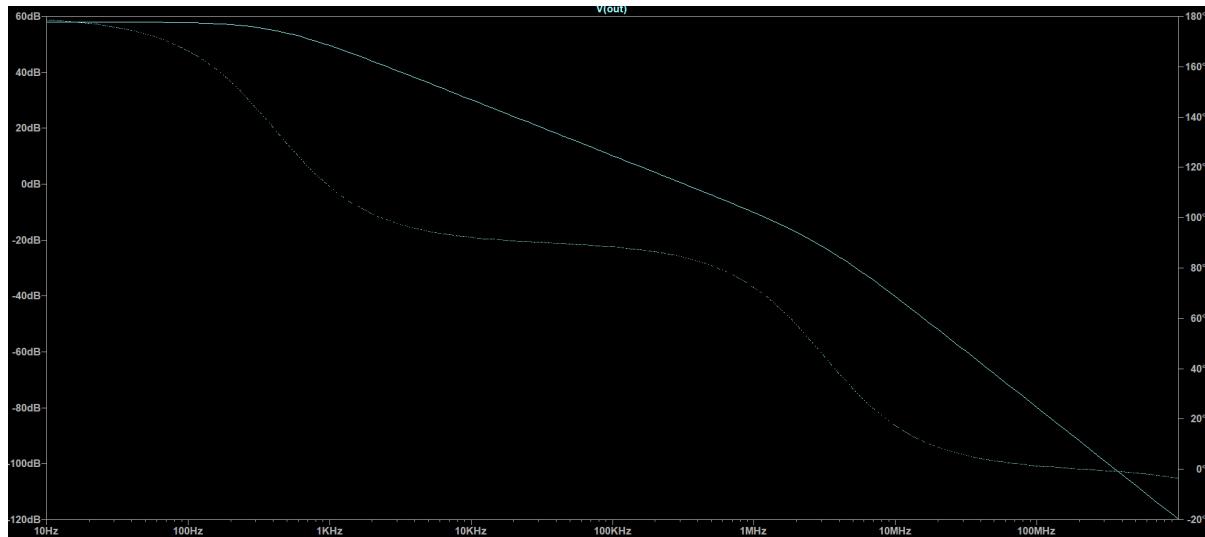


Figure 18: Loop Gain simulation results - heavy load.

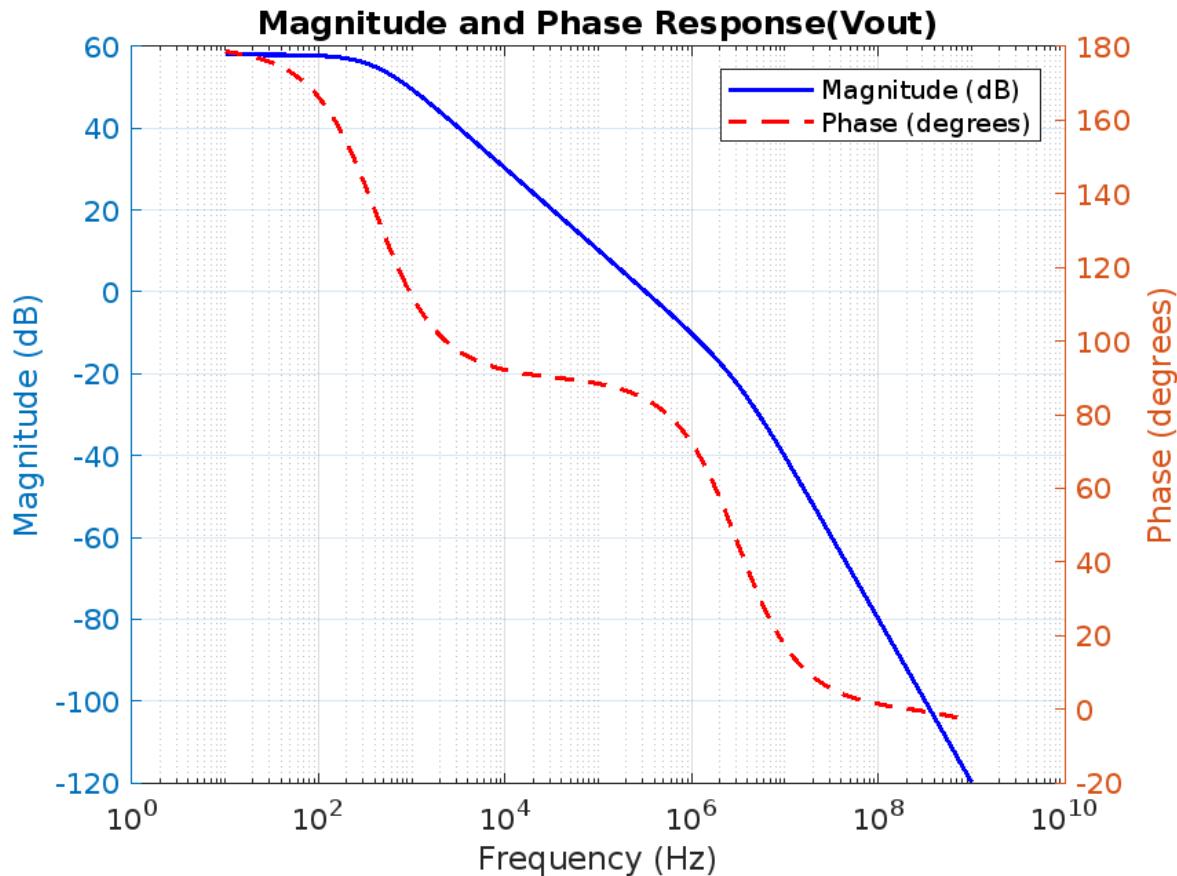


Figure 19: (Matlab)Loop Gain simulation results - heavy load.

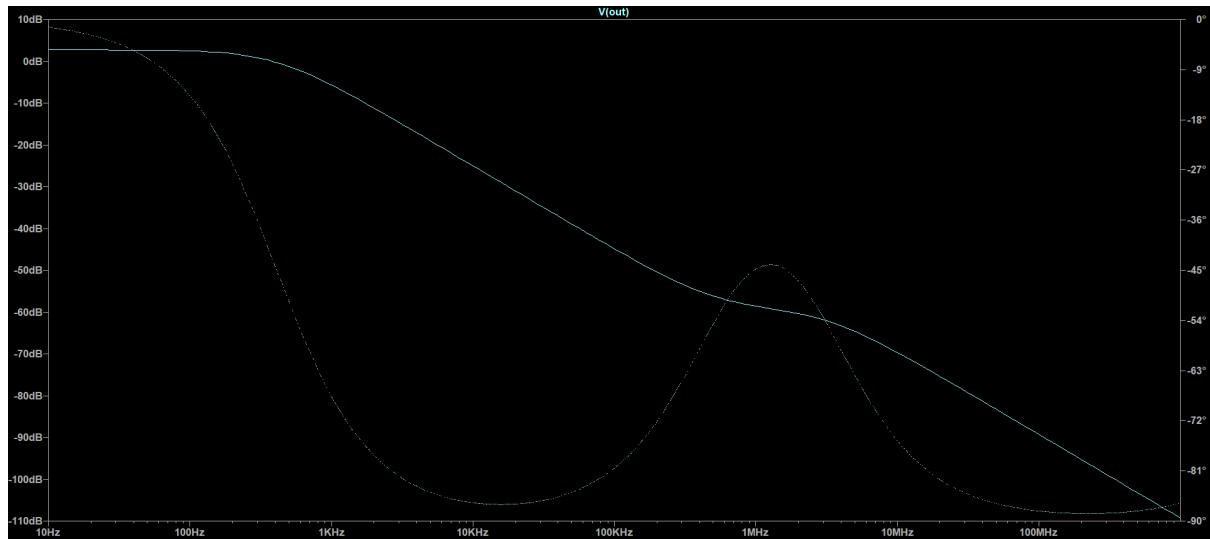


Figure 20: PSRR Openloop simulation results - heavy load.

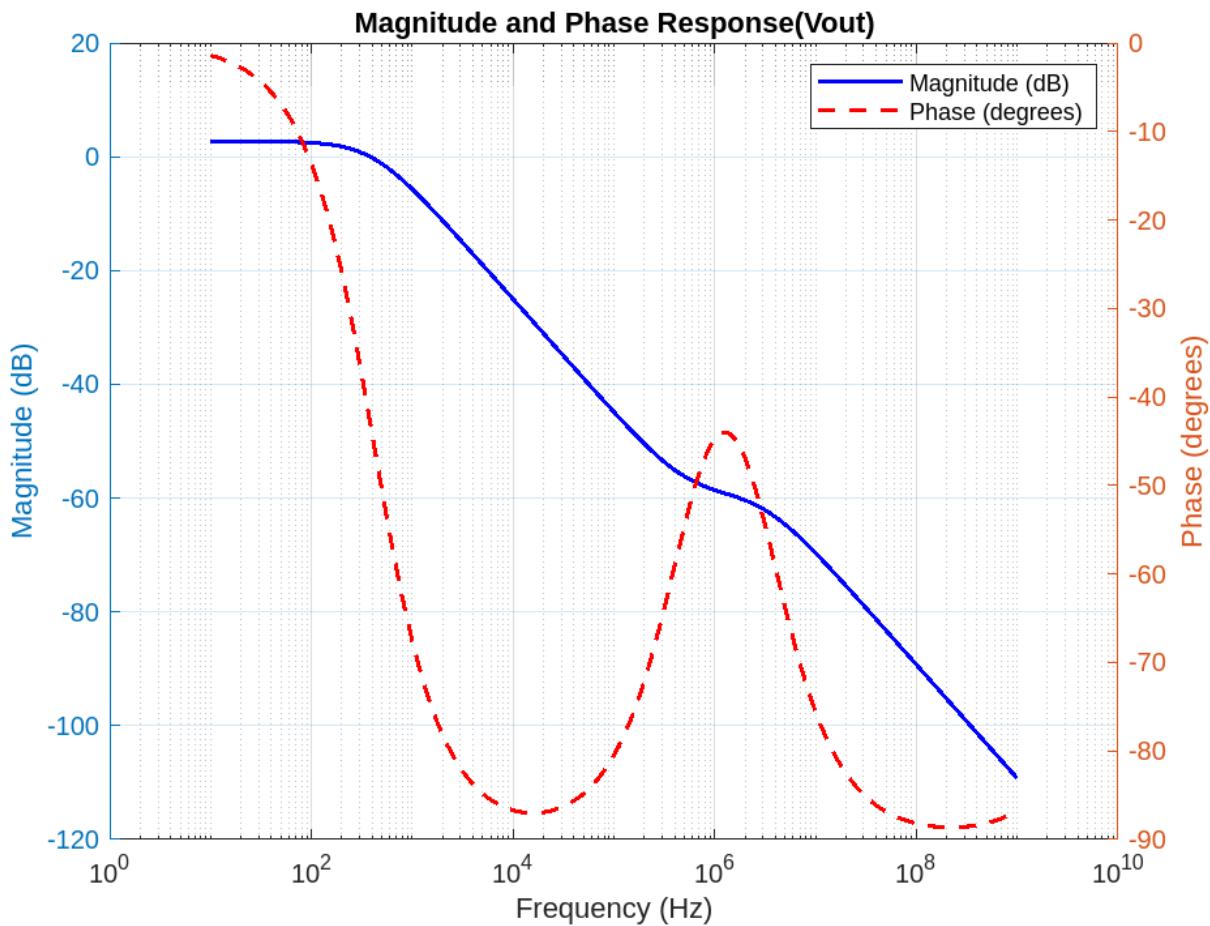


Figure 21: (Matlab)PSRR Openloop simulation results - heavy load.

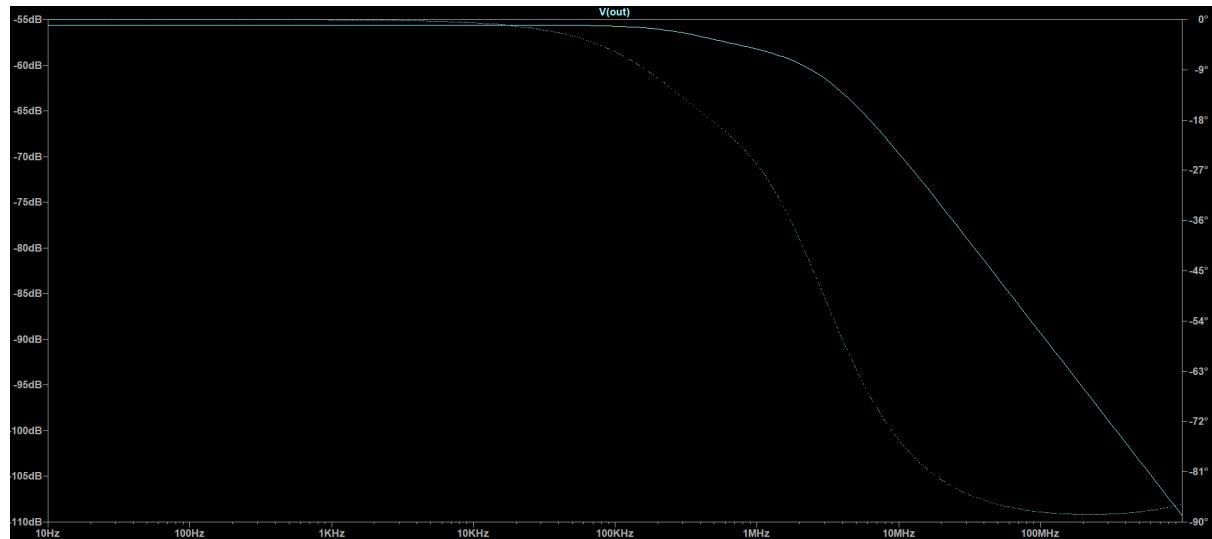


Figure 22: PSRR Closeloop simulation results - heavy load.

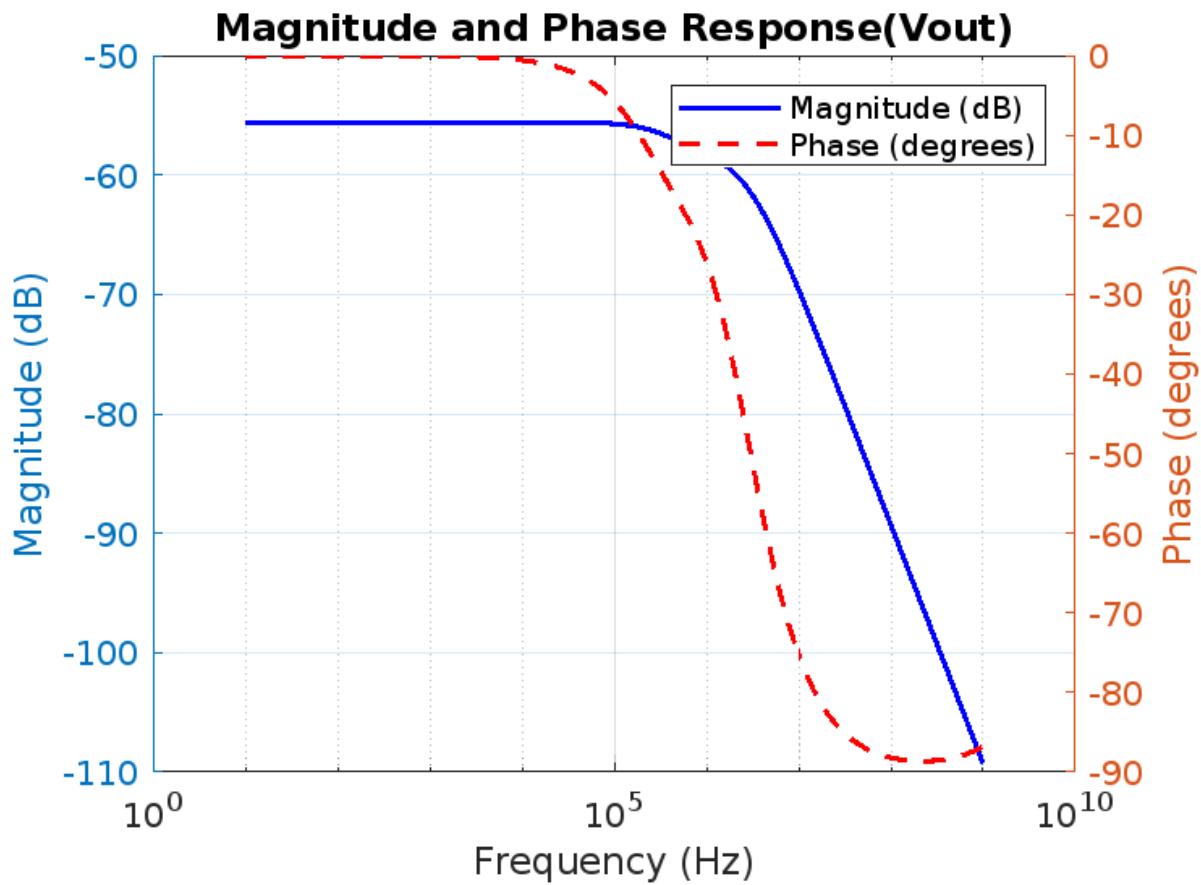


Figure 23: (Matlab)PSRR Closeloop simulation results - heavy load.

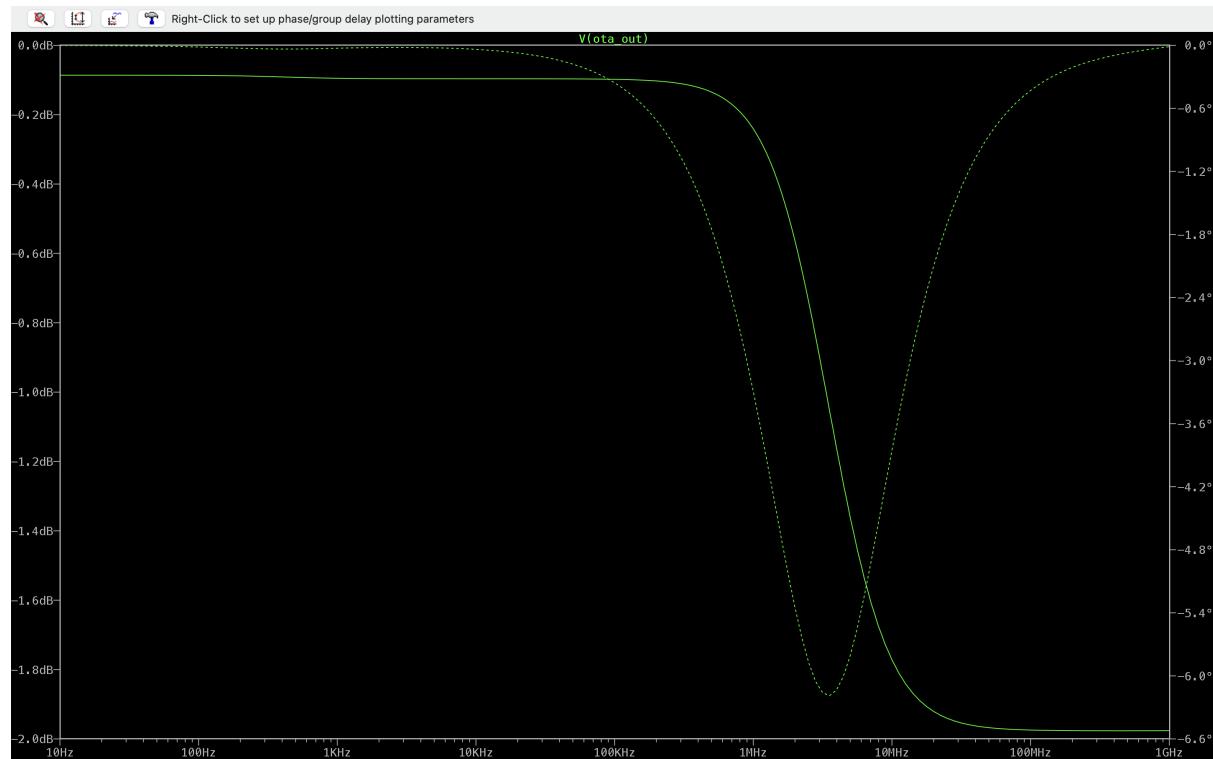


Figure 24: PSRR Openloop OTA simulation results - heavy load.

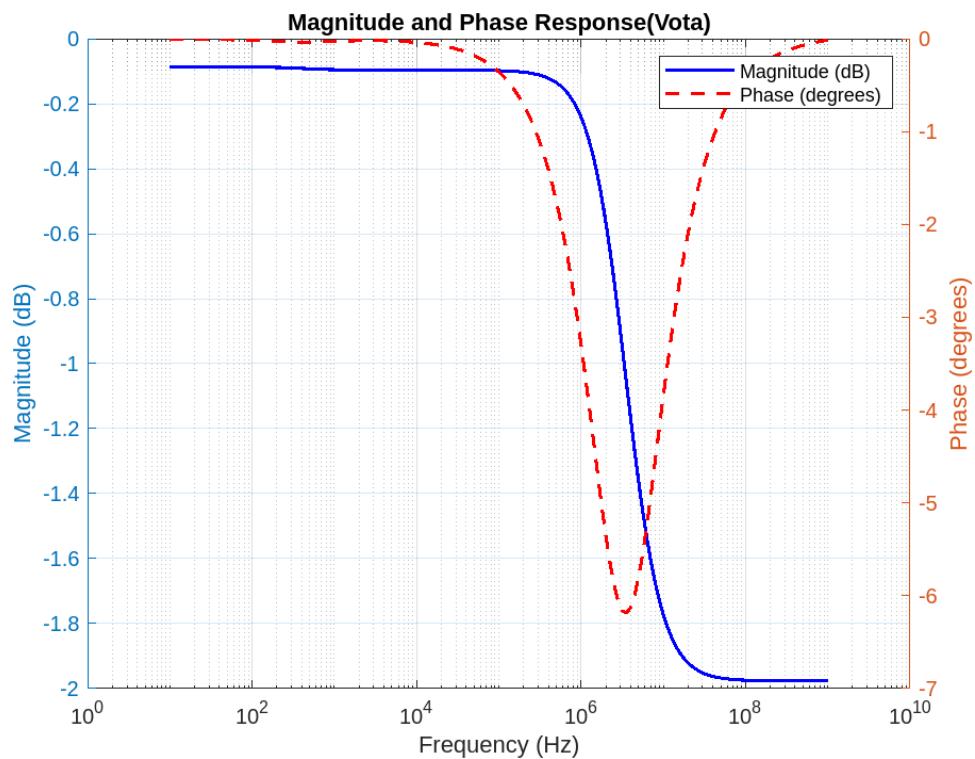


Figure 25: (Matlab)PSRR Openloop OTA simulation results - heavy load.

$$PSRR_{CL} = \frac{PSRR_{OL}}{1 + A_{loop}}$$

$$A_{loop} = 57.97$$

$$PSRR_{OL} = 2.72$$

so from the above values
 $PSRR_{CL}$ should be $2.72 - 57.97 = -55.25$
and from simulation we get -55.25

90nm Light Load: Provide PSRR simulation results at heavy and light load conditions. Include mathematical expressions if derived.

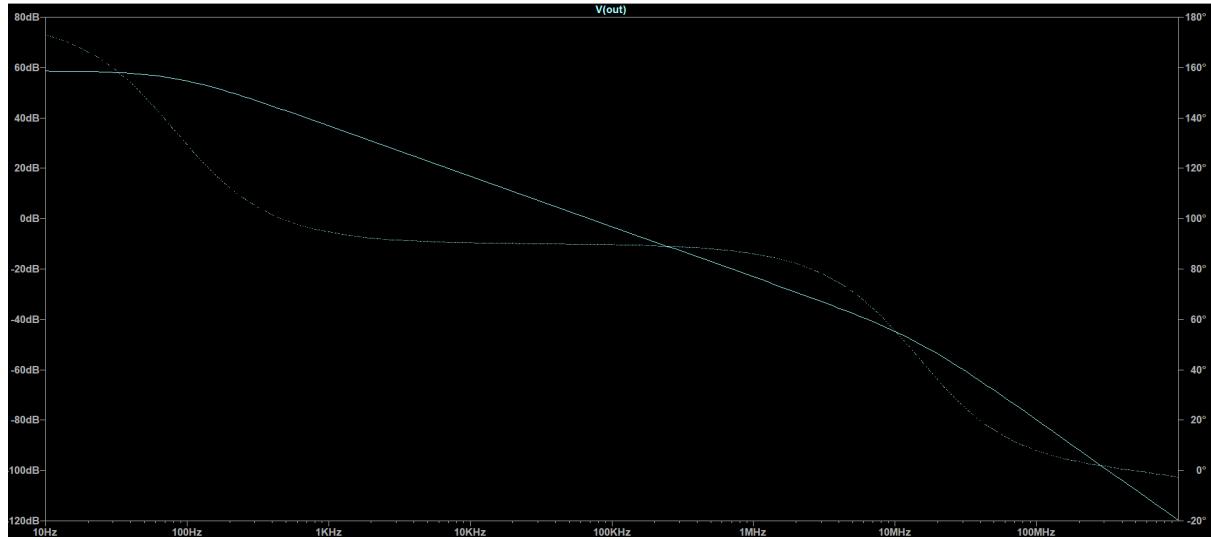


Figure 26: Loop Gain simulation results - heavy load.

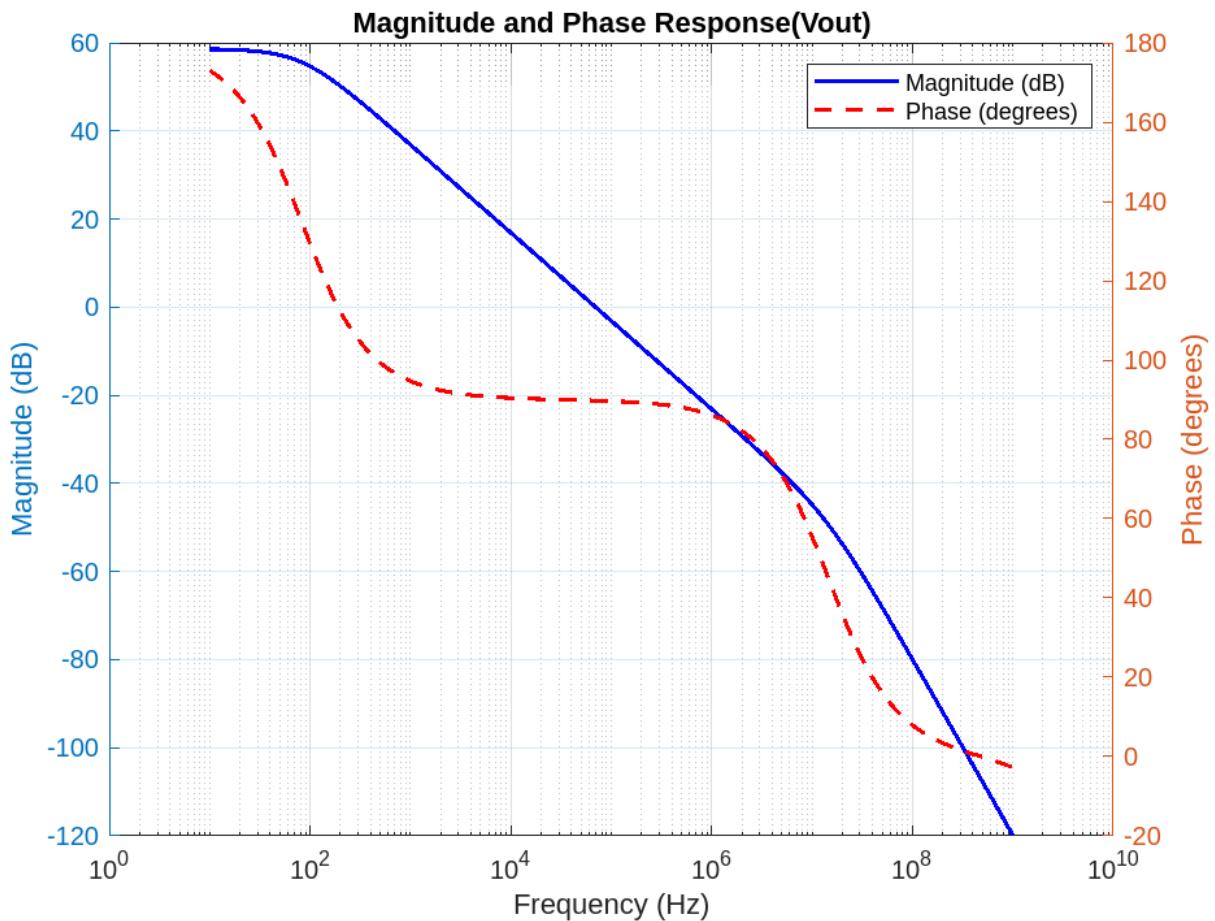


Figure 27: (Matlab)Loop Gain simulation results - heavy load.

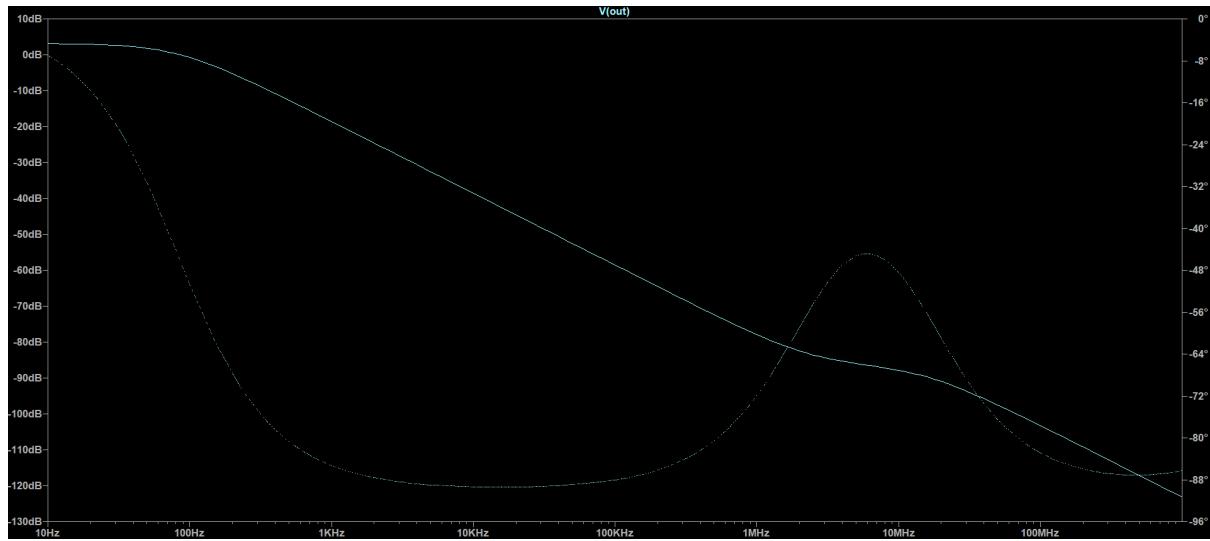


Figure 28: PSRR Openloop simulation results - heavy load.

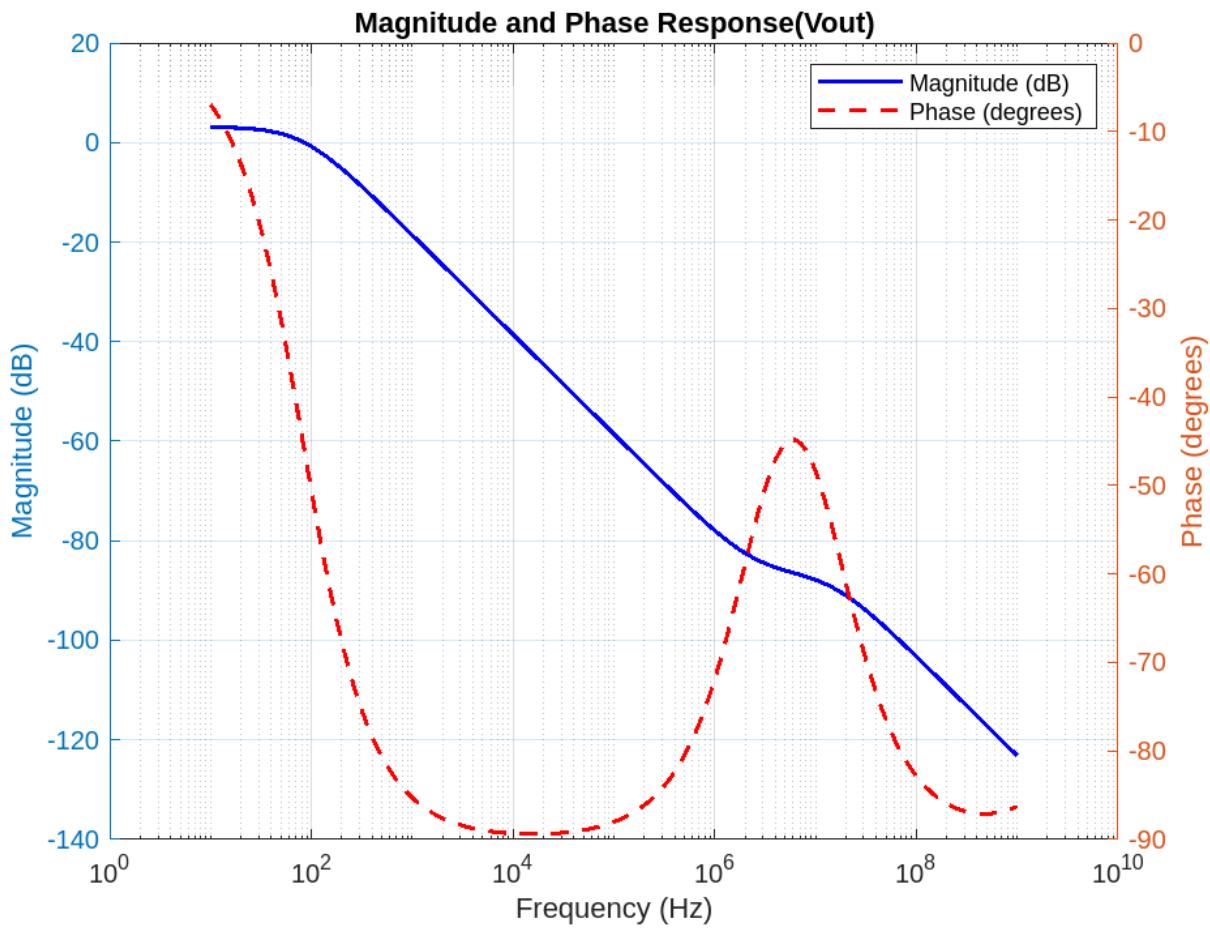


Figure 29: (Matlab)PSRR Openloop simulation results - heavy load.

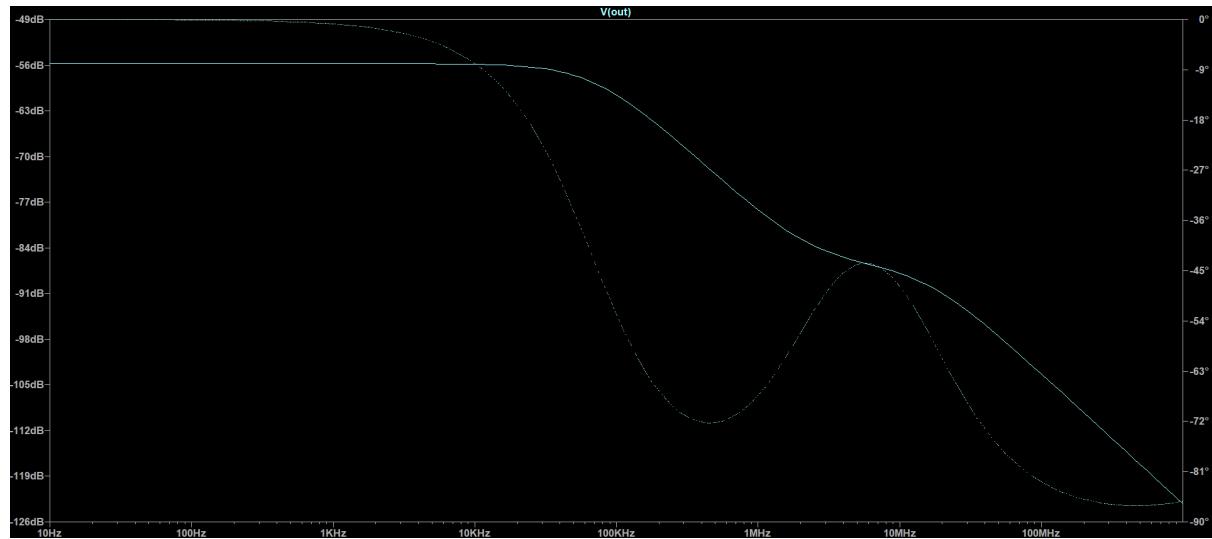


Figure 30: PSRR Closeloop simulation results - heavy load.

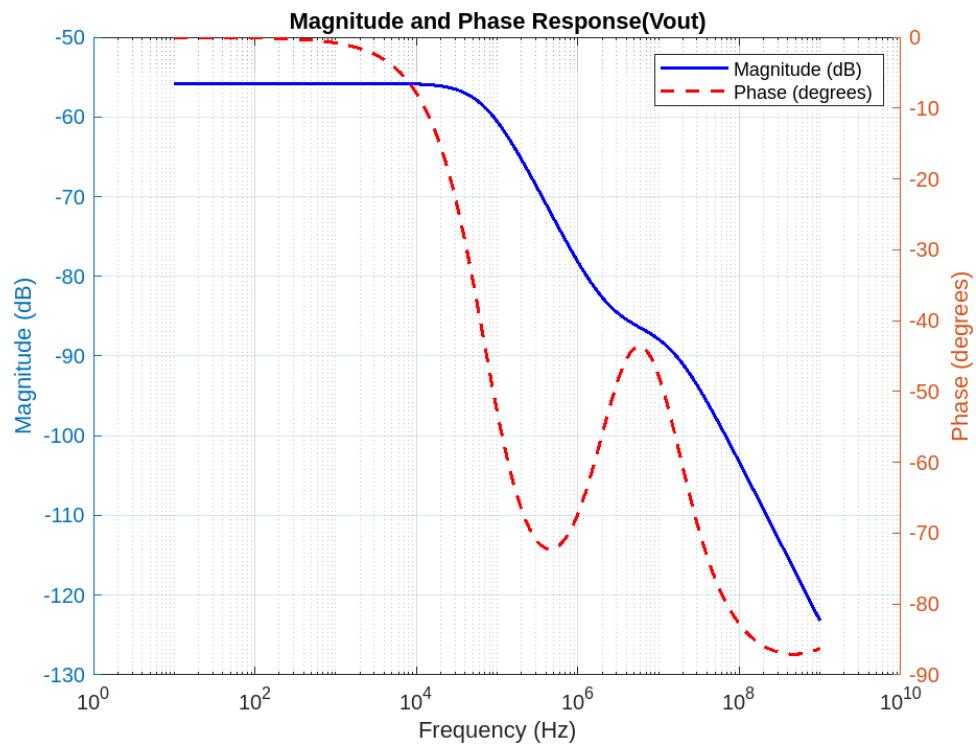


Figure 31: (Matlab)PSRR Closeloop simulation results - heavy load.

$$PSRR_{CL} = \frac{PSRR_{OL}}{1 + A_{loop}}$$

$$A_{loop} = 58.56$$

$$PSRR_{OL} = 3.10$$

so from the above values
 $PSRR_{CL}$ should be $3.10 - 58.56 = -55.46$
and from simulation we get -55.46

135nm Heavy Load: Provide PSRR simulation results at heavy and light load conditions. Include mathematical expressions if derived.

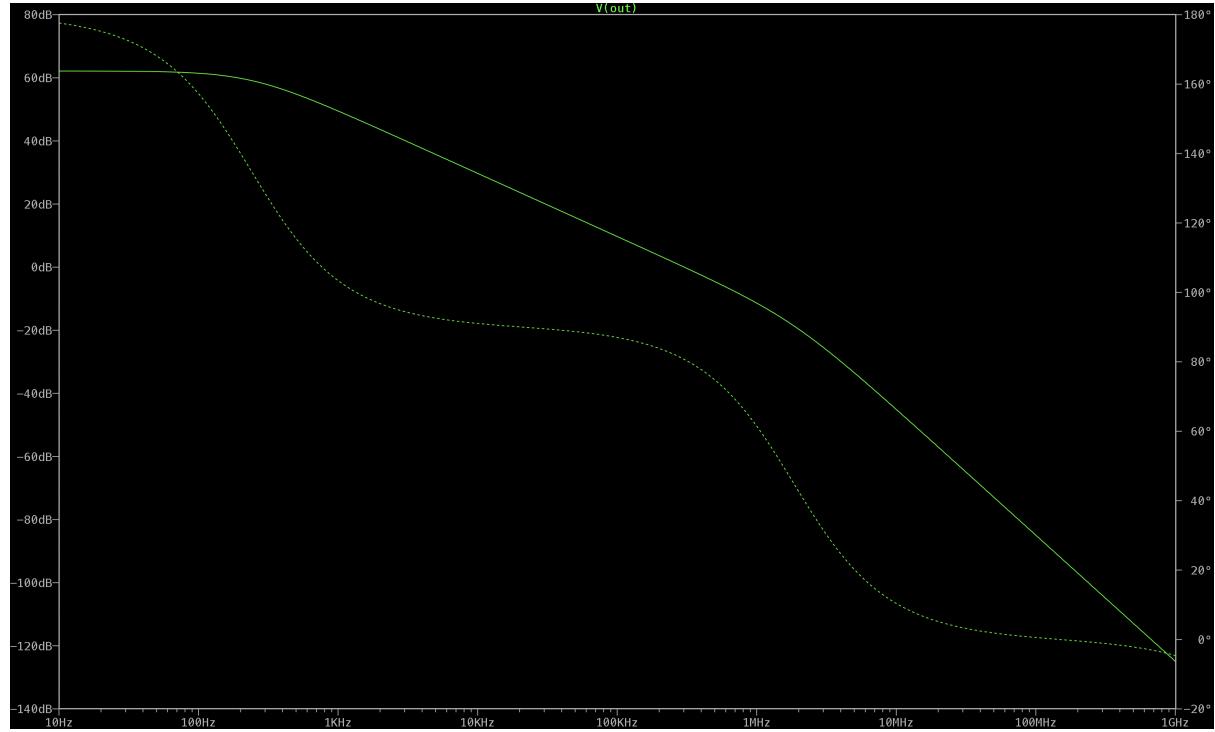


Figure 32: Loop Gain simulation results - heavy load.

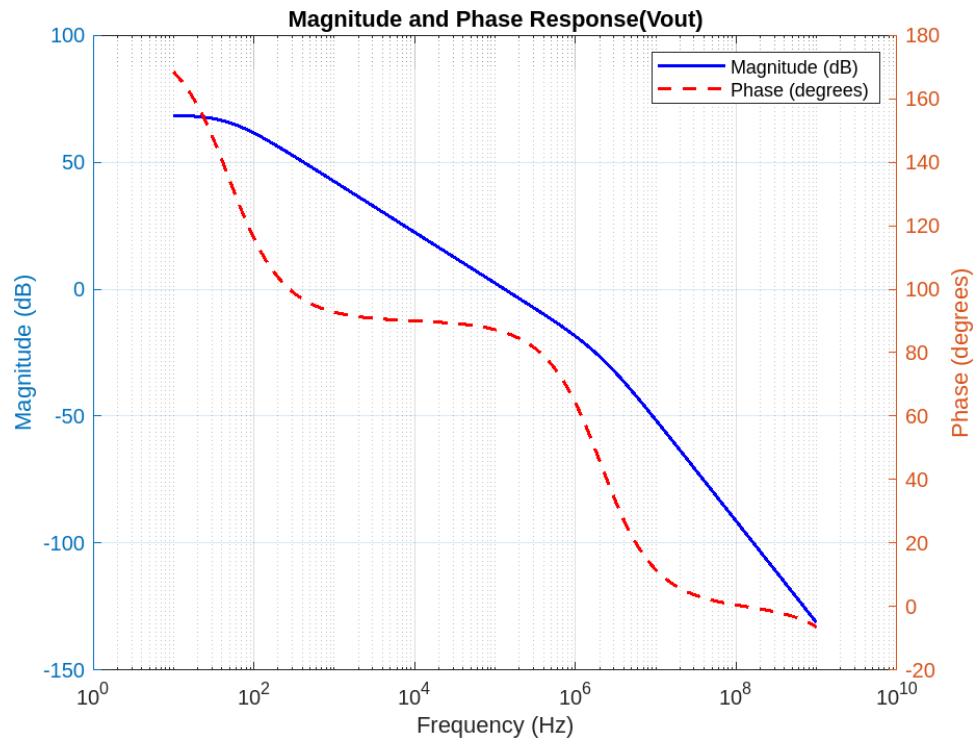


Figure 33: (Matlab)Loop Gain simulation results - heavy load.

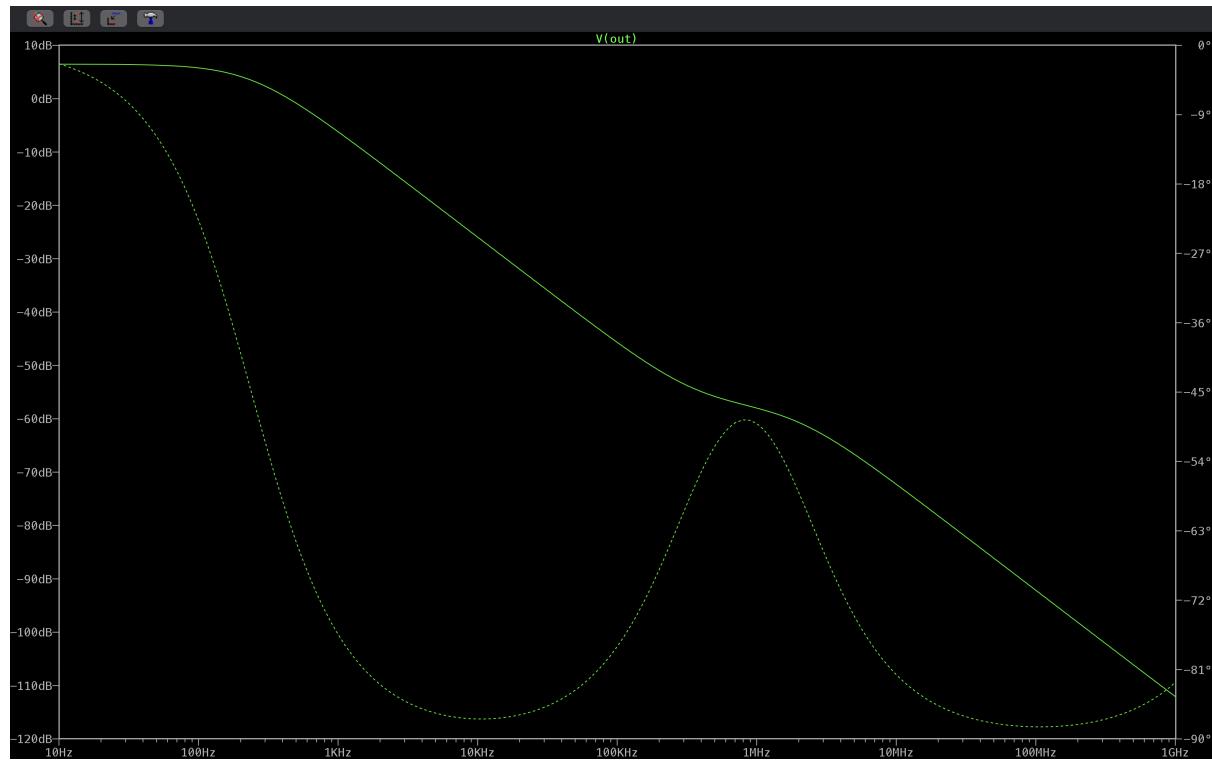


Figure 34: PSRR Openloop simulation results - heavy load.

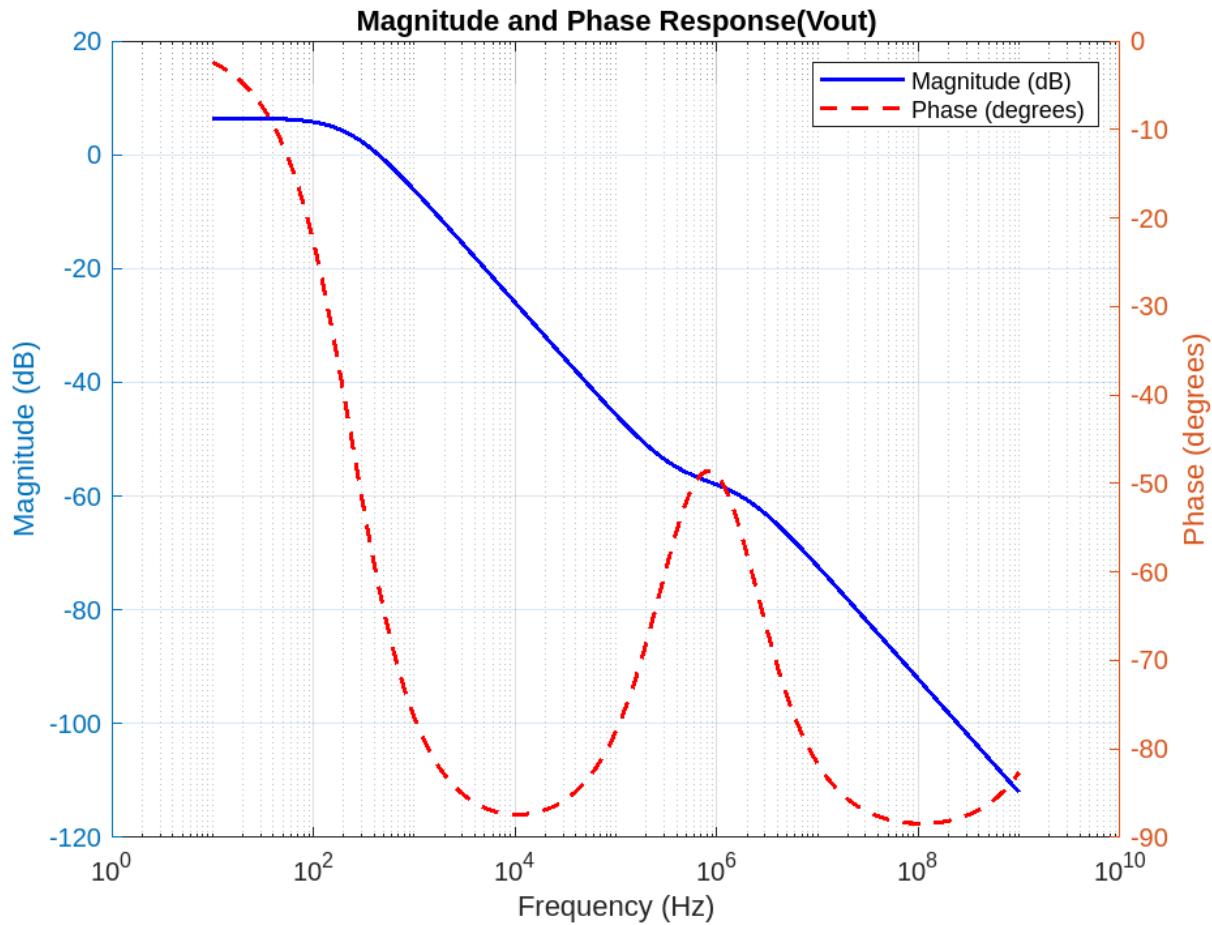


Figure 35: (Matlab)PSRR Openloop simulation results - heavy load.

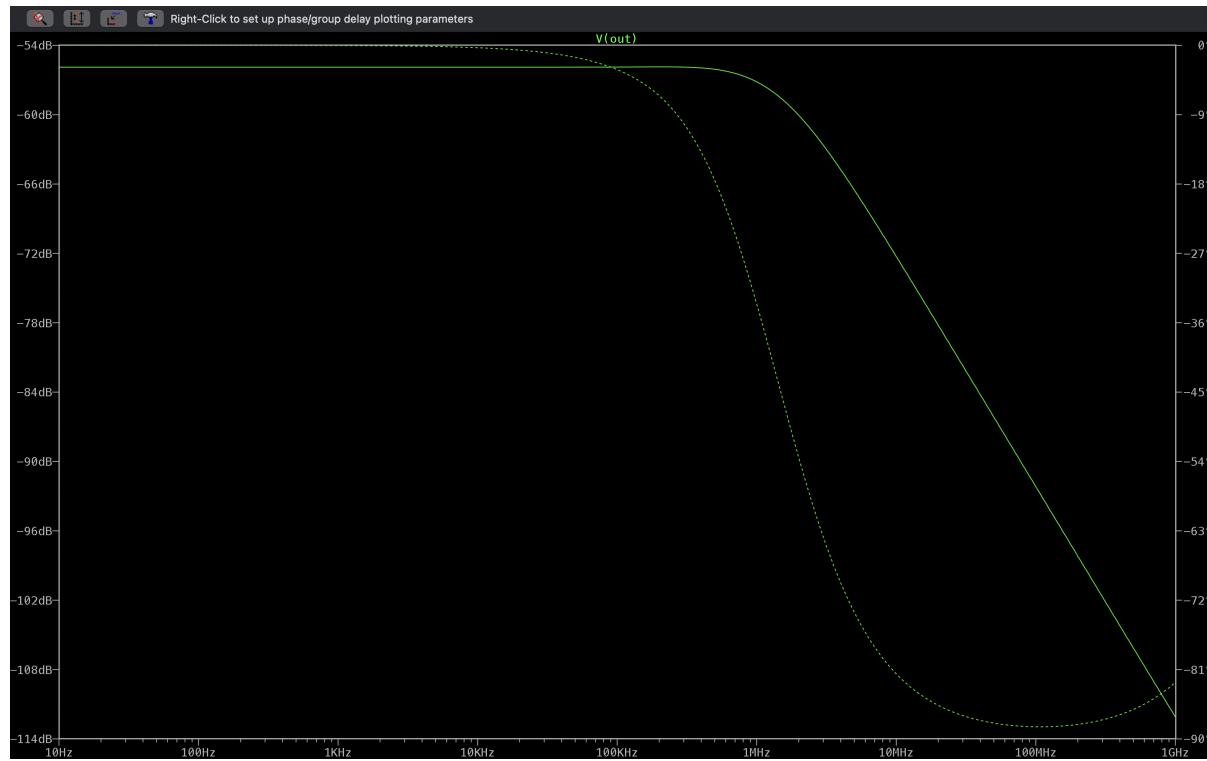


Figure 36: PSRR Closeloop simulation results - heavy load.

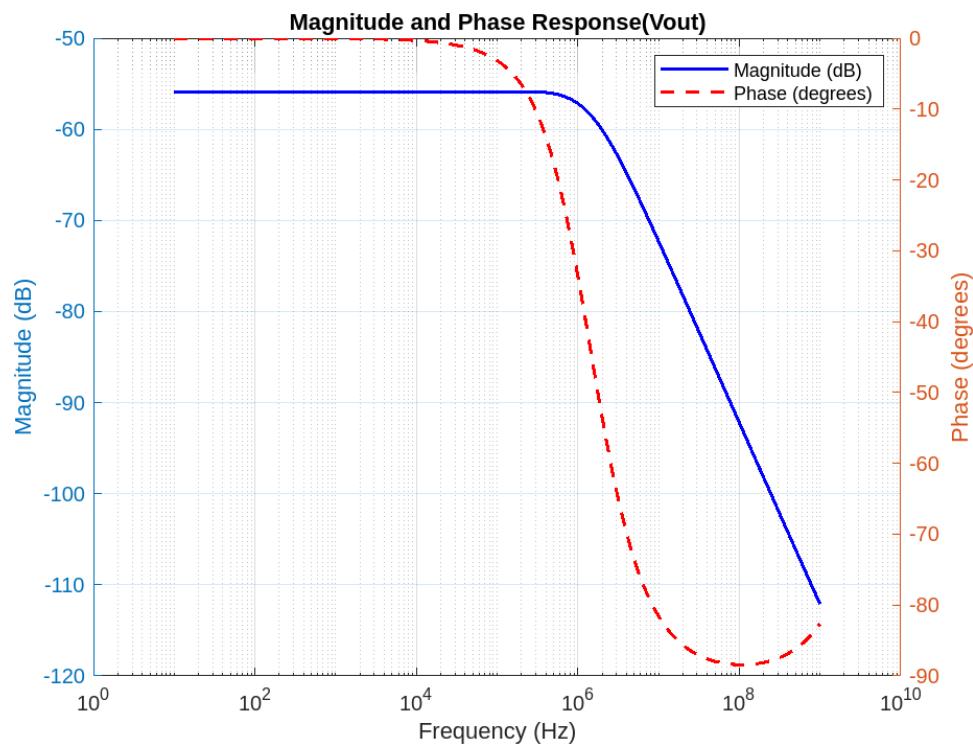


Figure 37: (Matlab)PSRR Closeloop simulation results - heavy load.

$$PSRR_{CL} = \frac{PSRR_{OL}}{1 + A_{loop}}$$

$$A_{loop} = 62.149$$

$$PSRR_{OL} = 6.46$$

So from the above values

$$PSRR_{CL} \text{ should be } 6.46 - 62.149 = \underline{-55.689}$$

and from simulation we get -55.893

135nm Light Load: Provide PSRR simulation results at heavy and light load conditions. Include mathematical expressions if derived.

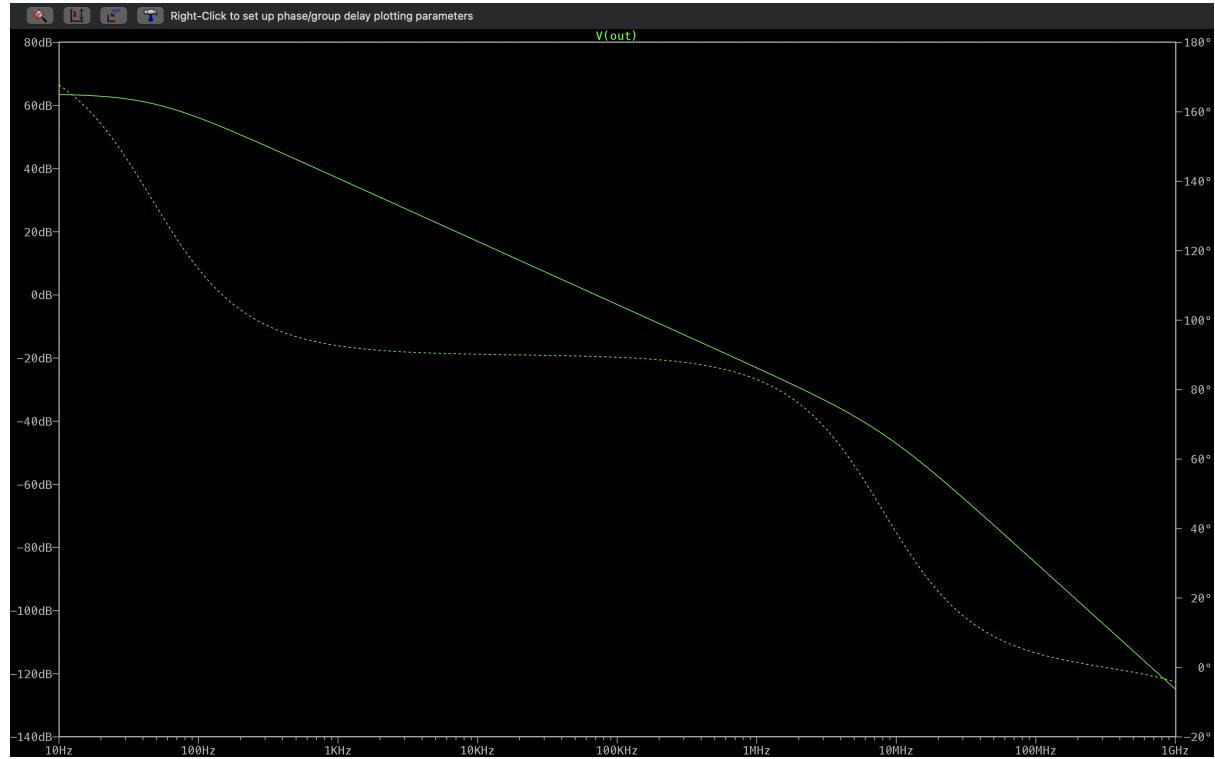


Figure 38: Loop Gain simulation results - light load.

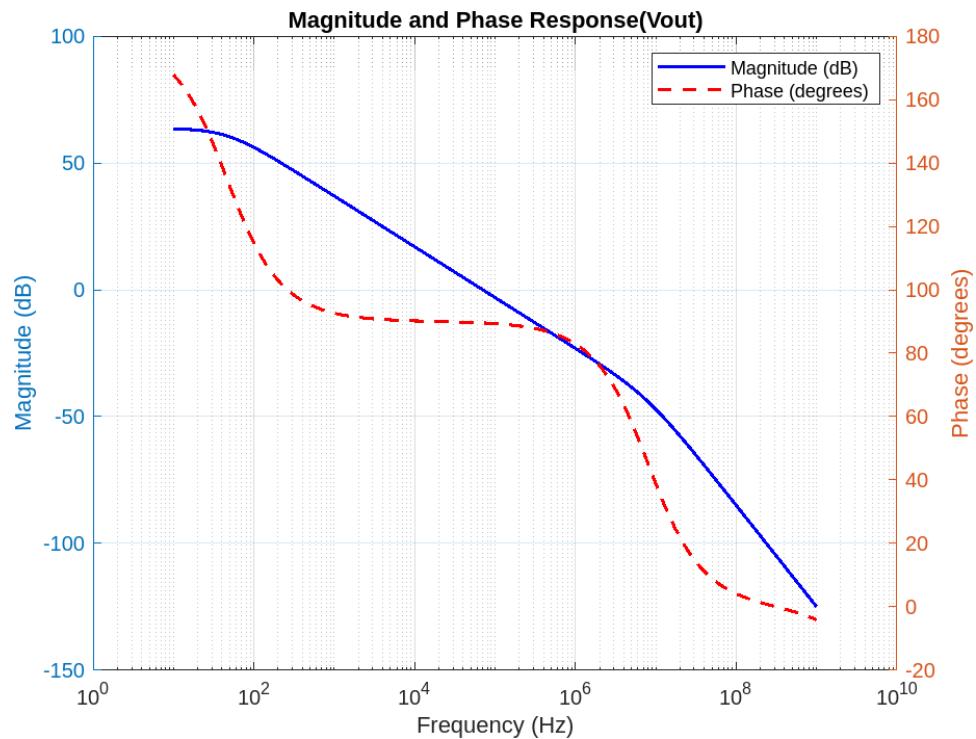


Figure 39: (Matlab)Loop Gain simulation results - light load.

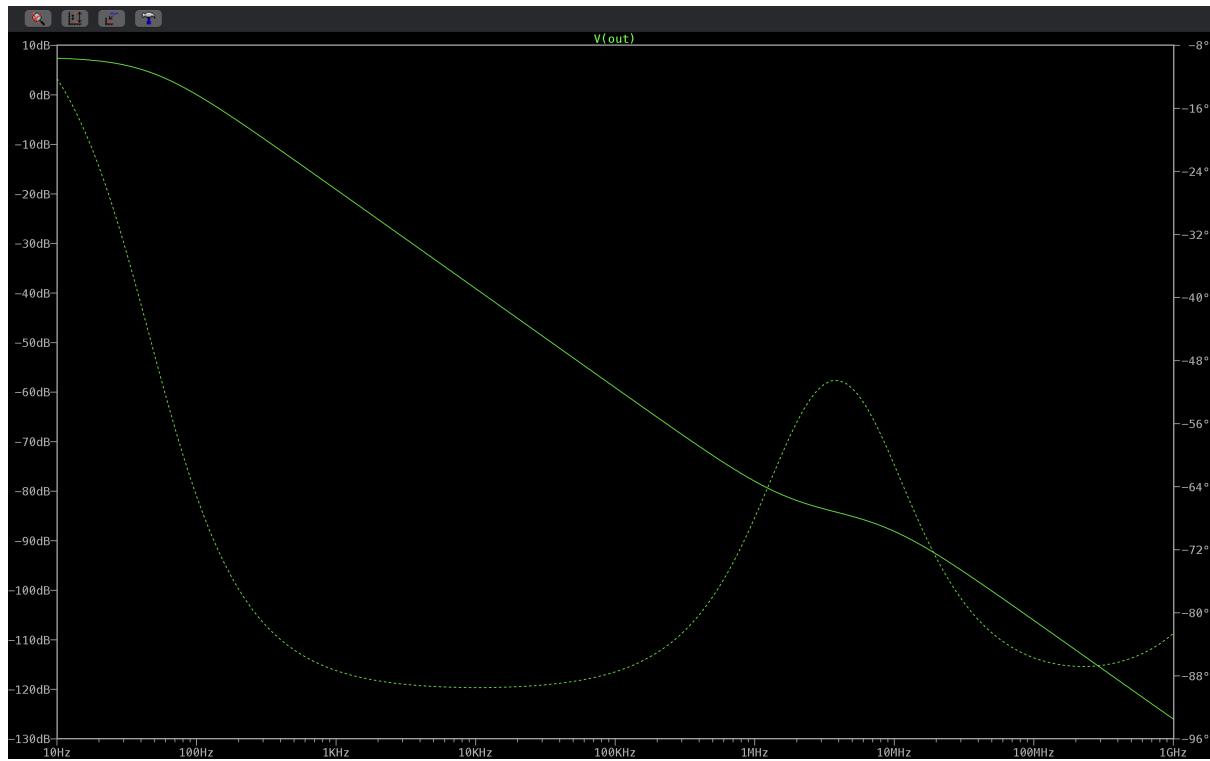


Figure 40: PSRR Openloop simulation results - light load.

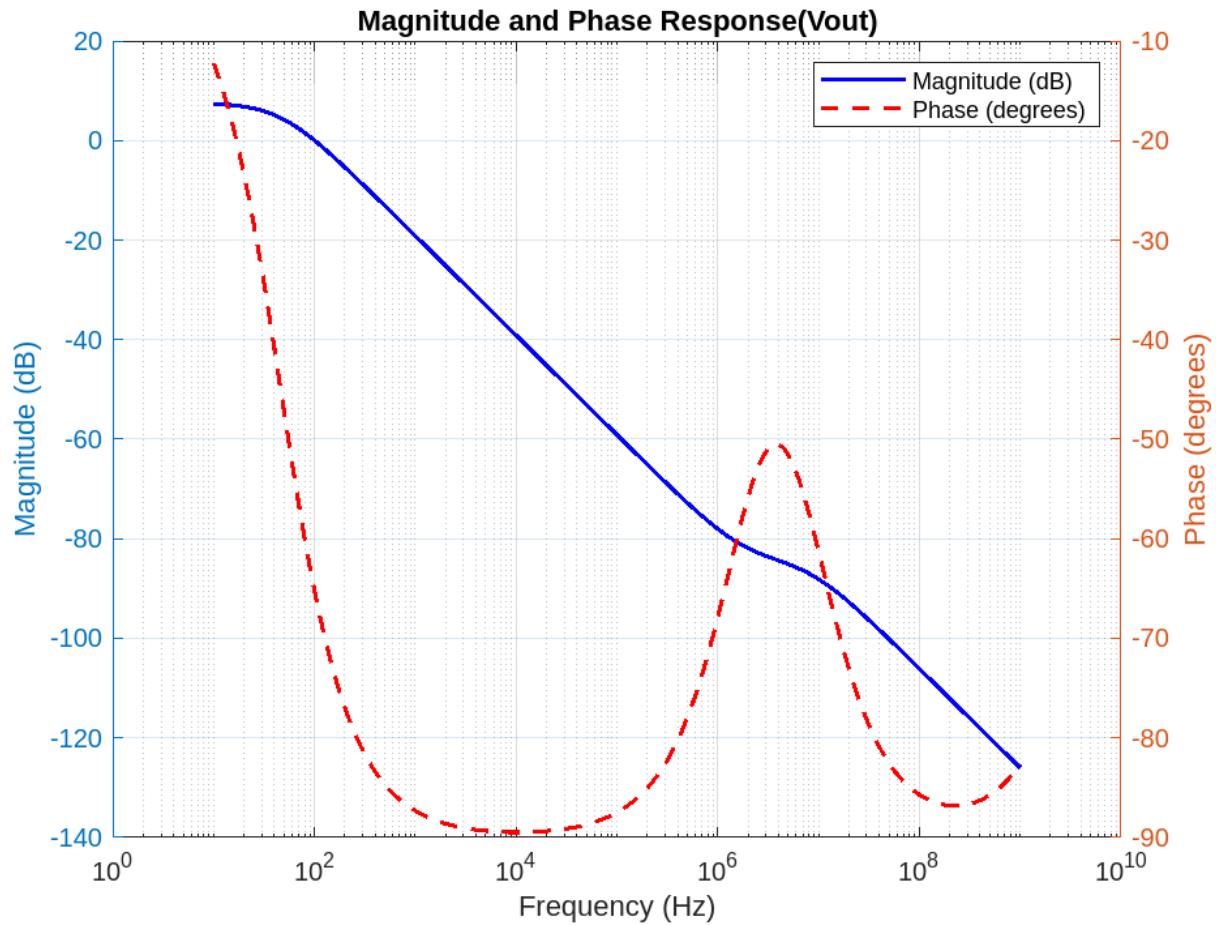


Figure 41: (Matlab)PSRR Openloop simulation results - light load.

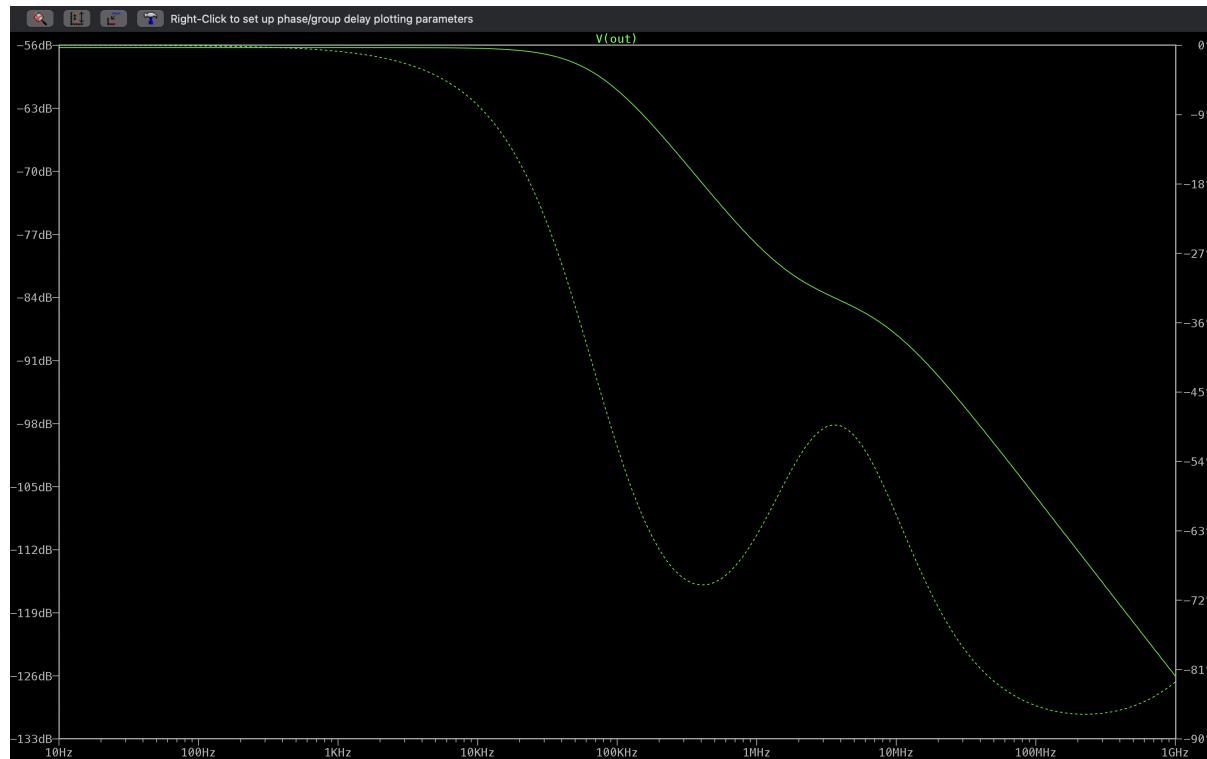


Figure 42: PSRR Closeloop simulation results - light load.

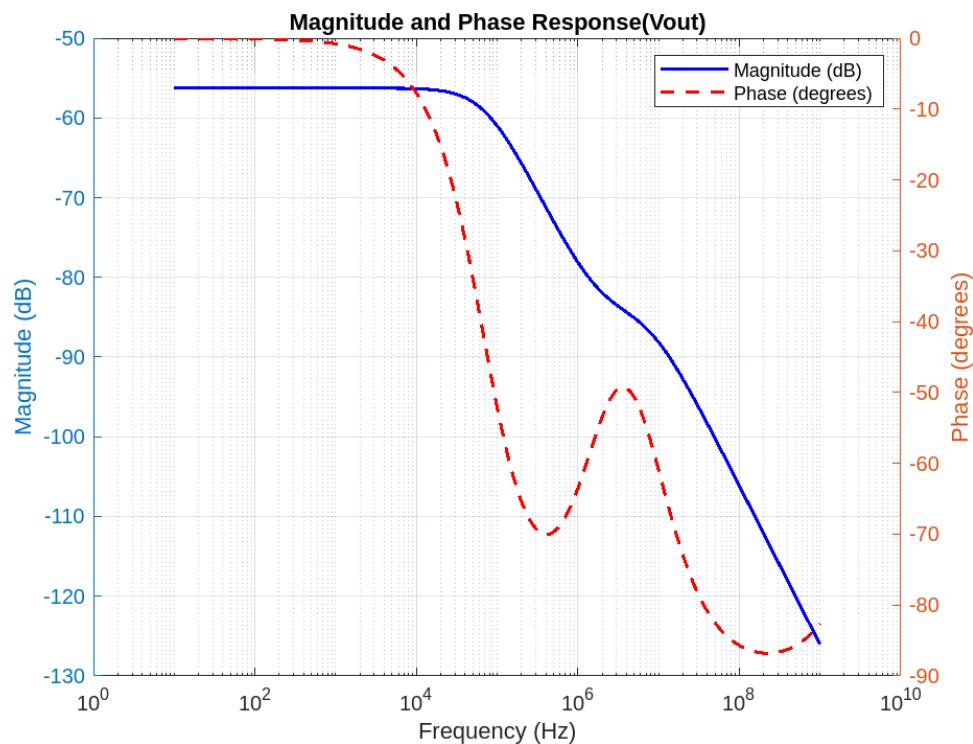


Figure 43: (Matlab)PSRR Closeloop simulation results - light load.

$$PSRR_{CL} = \frac{PSRR_{OL}}{1 + A_{loop}}$$

$$A_{loop} = 63.48$$

$$PSRR_{OL} = 7.39$$

So from the above values
 $PSRR_{CL}$ should be $7.39 - 63.48 = \underline{-56.09}$
 and from simulation we get $\underline{-56.24}$

8. Transient Simulation Results

90nm: I have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a duty cycle of 50 . From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

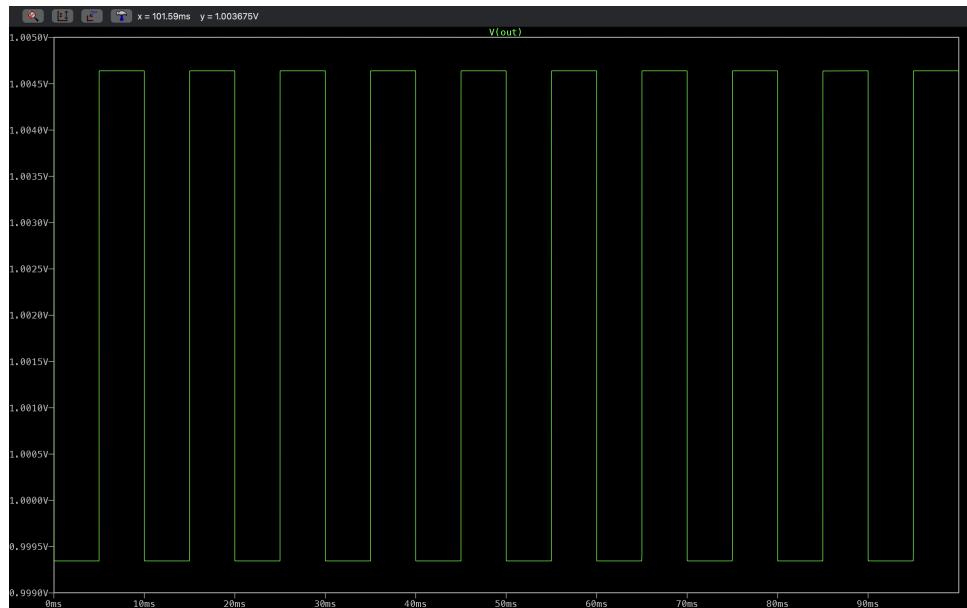


Figure 44: Transient simulation results for 90nm.

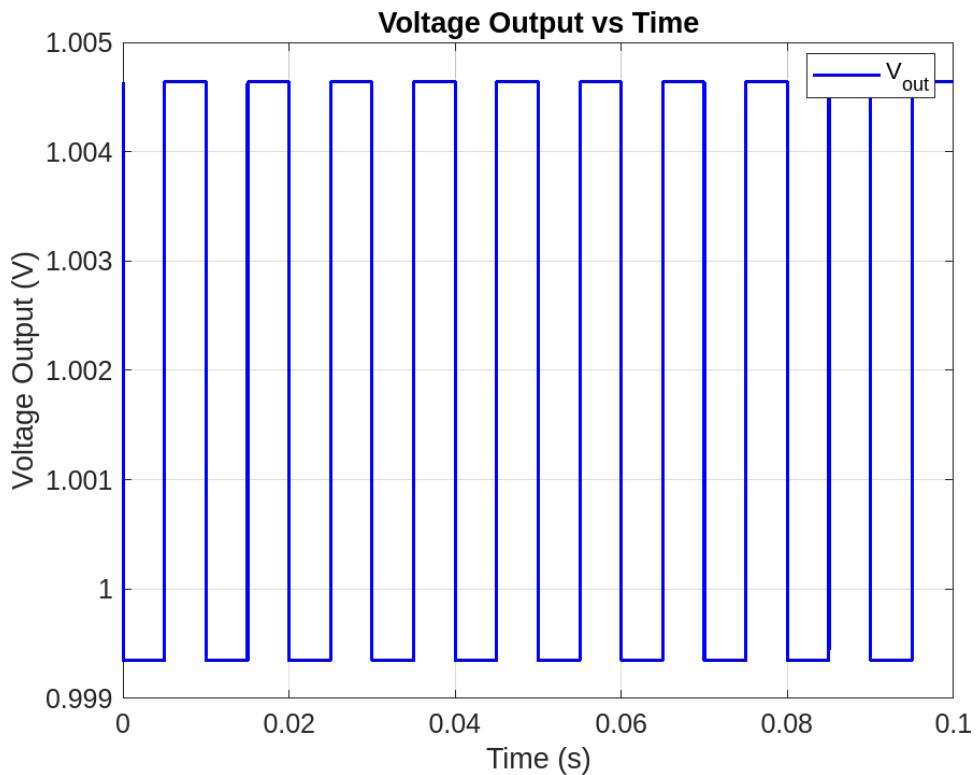


Figure 45: (Matlab)Transient simulation results for 90nm.

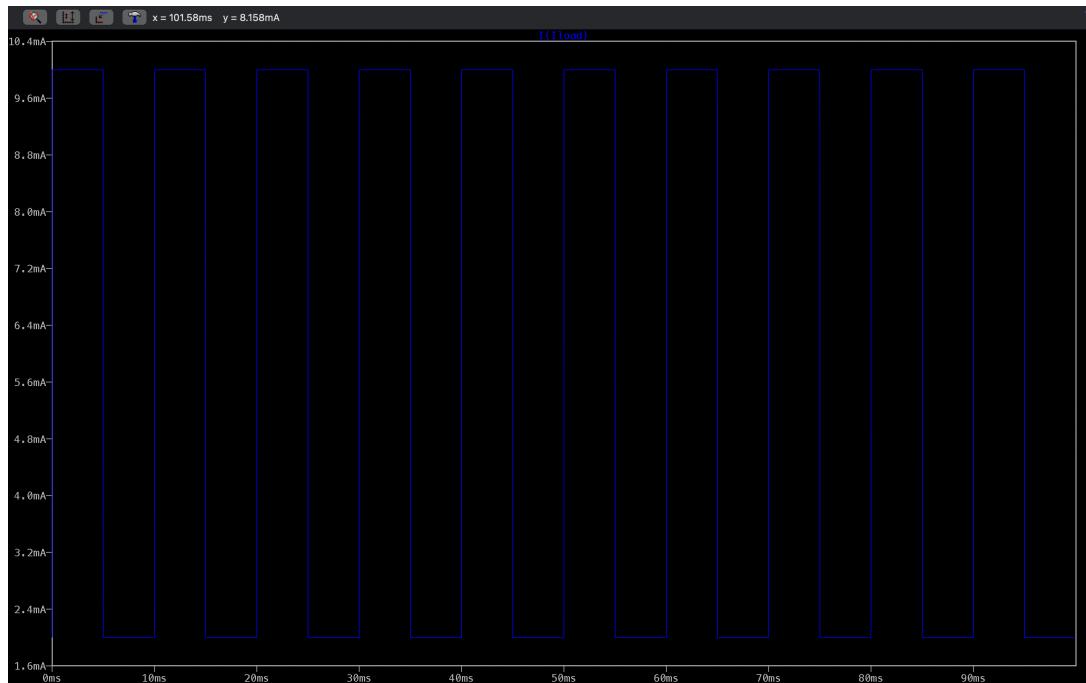


Figure 46: Transient simulation results for 90nm.

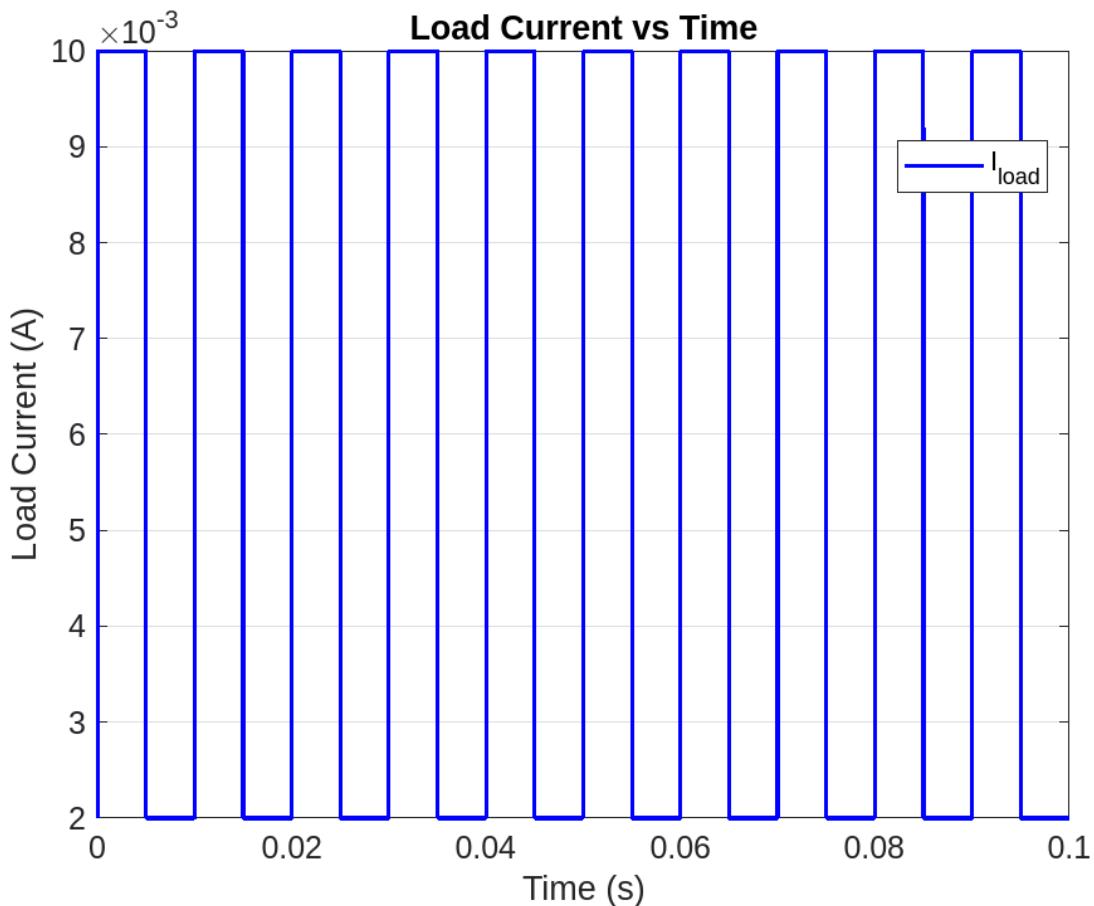


Figure 47: (Matlab) Transient simulation results for 90nm.

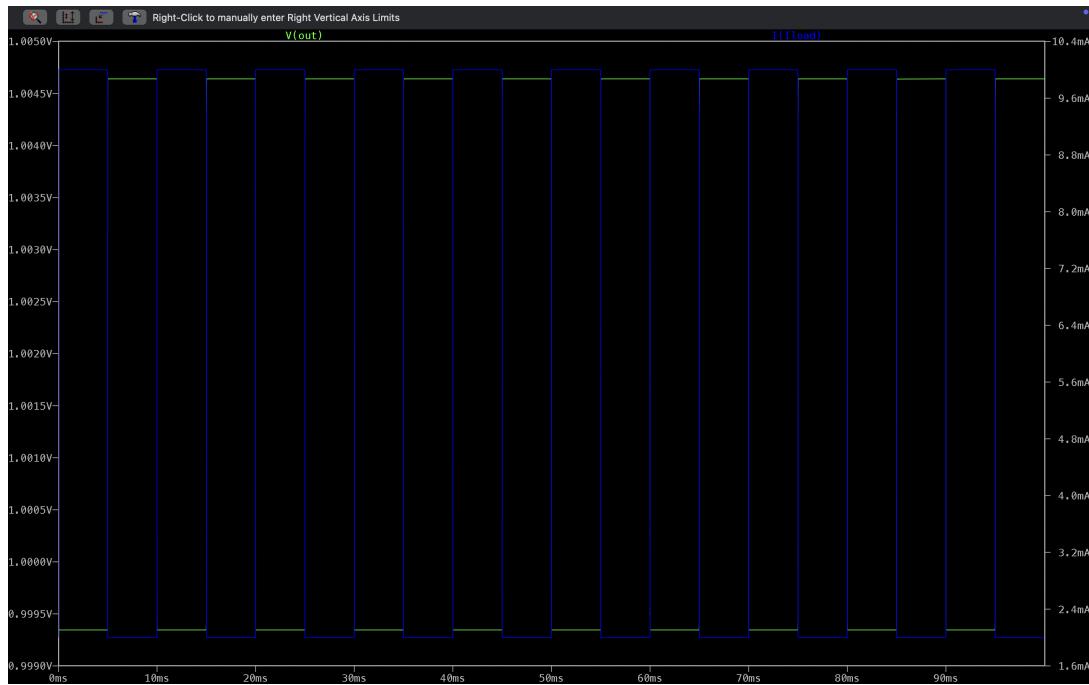


Figure 48: Transient simulation results for 90nm .

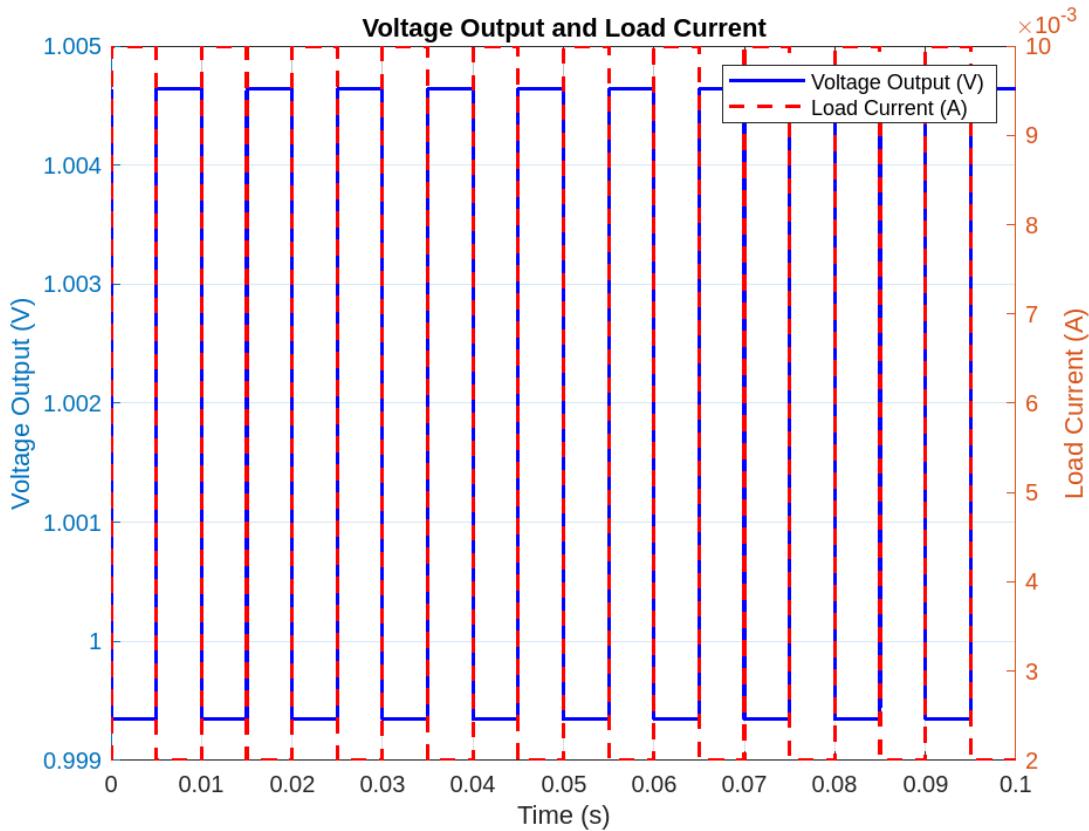


Figure 49: (Matlab)Transient simulation results for 90nm .

135nm: I have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a duty cycle of 50 . From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

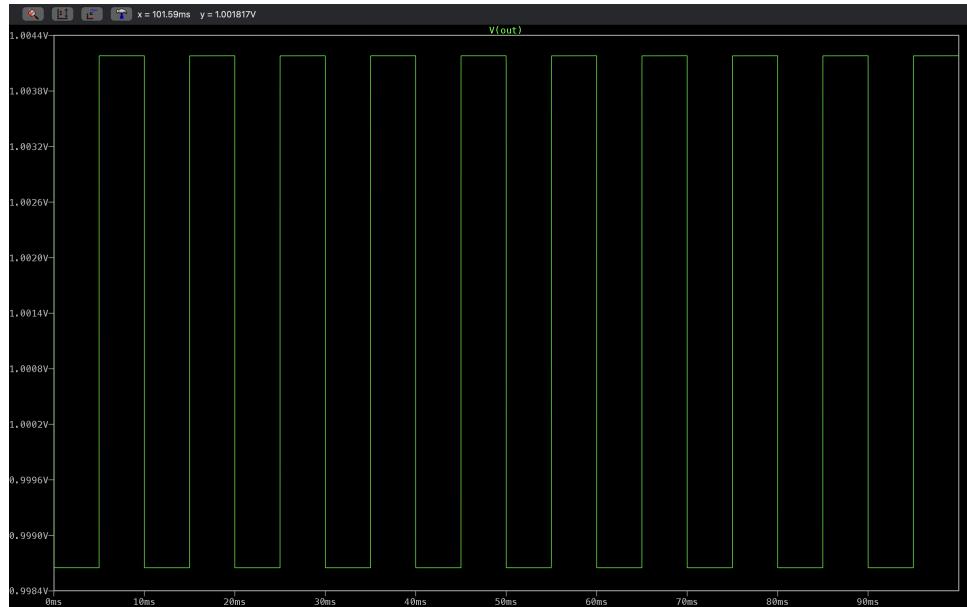


Figure 50: Transient simulation results.

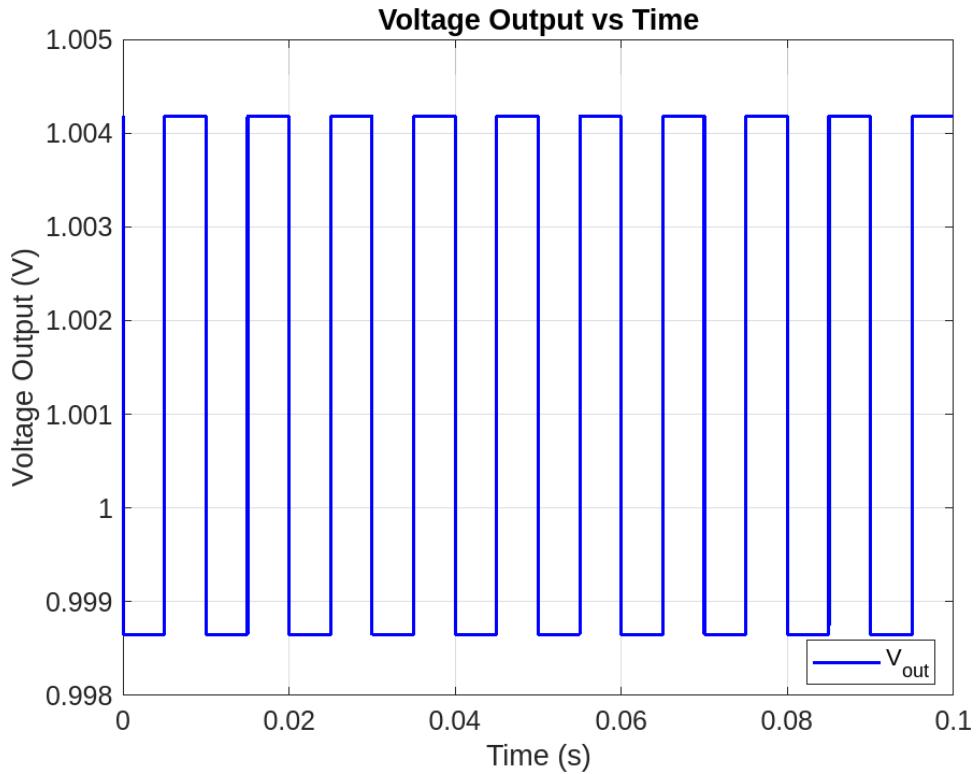


Figure 51: (Matlab)Transient simulation results.

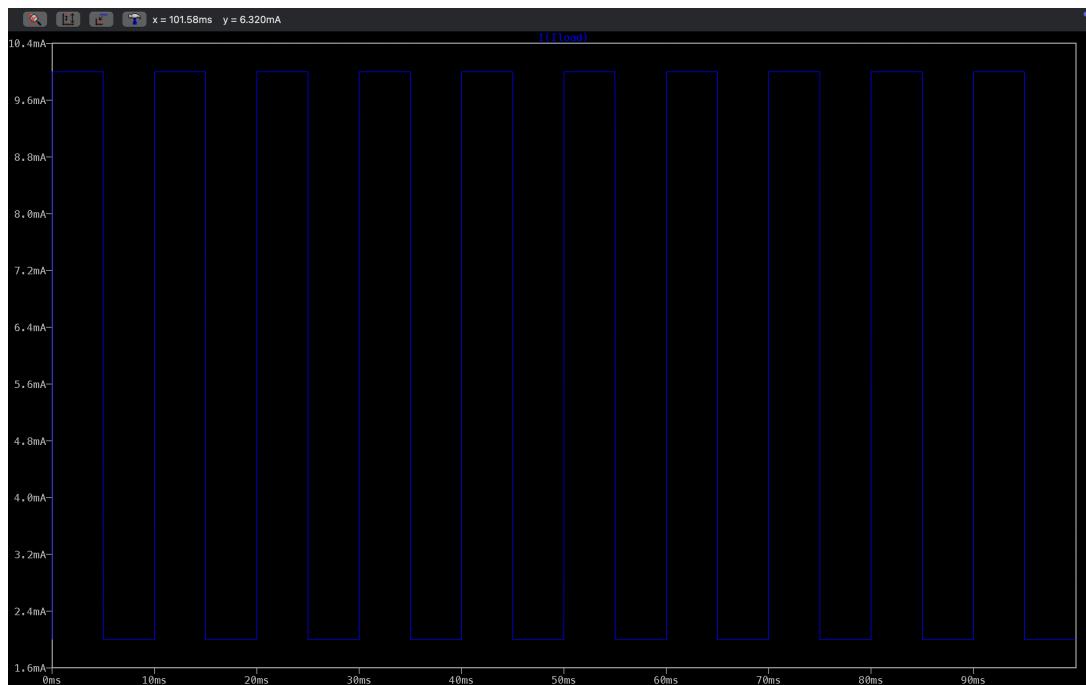


Figure 52: Transient simulation results.

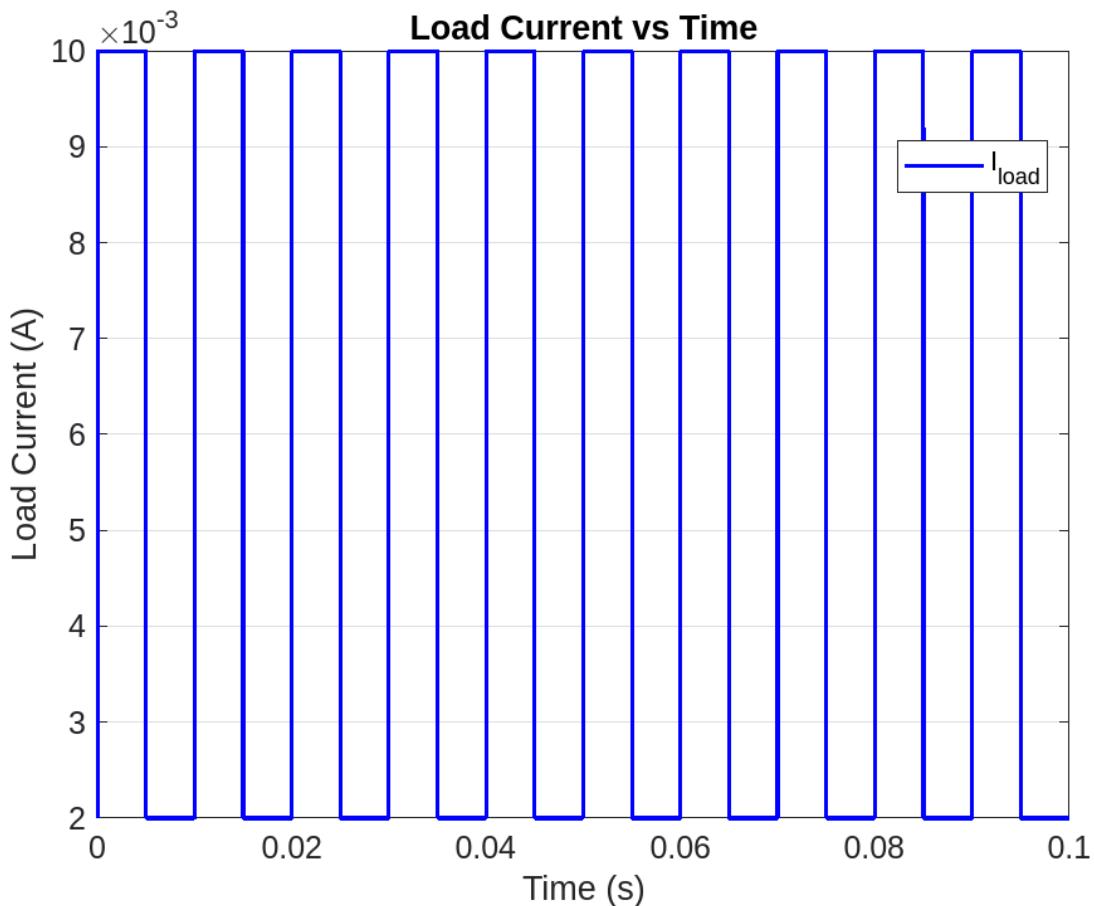


Figure 53: (Matlab) Transient simulation results.

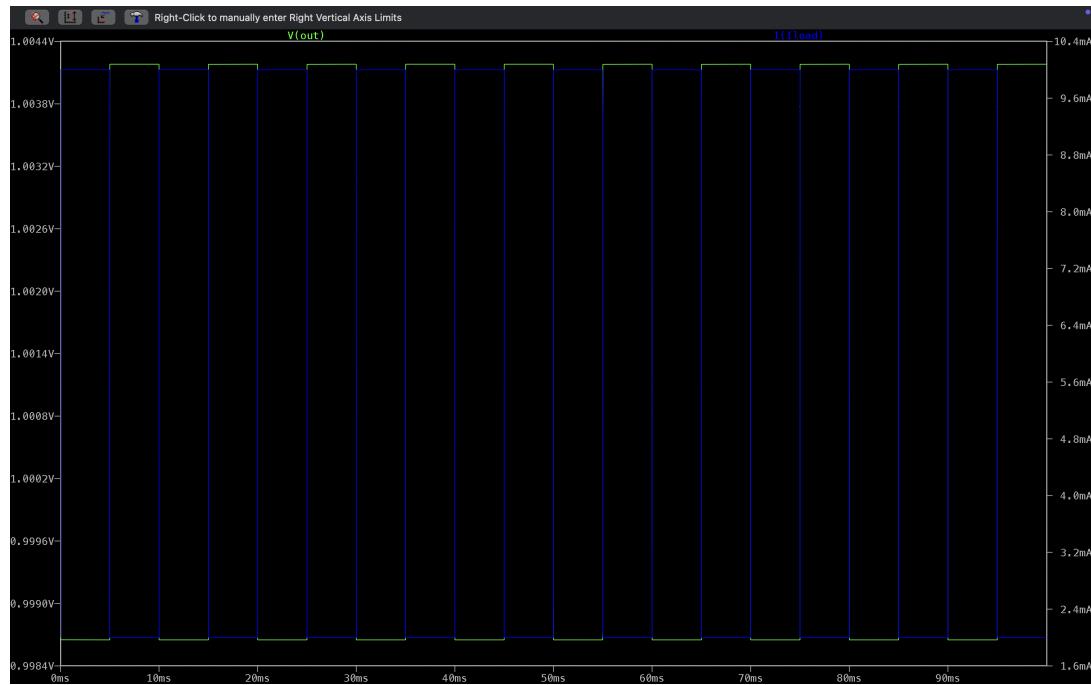


Figure 54: Transient simulation results.

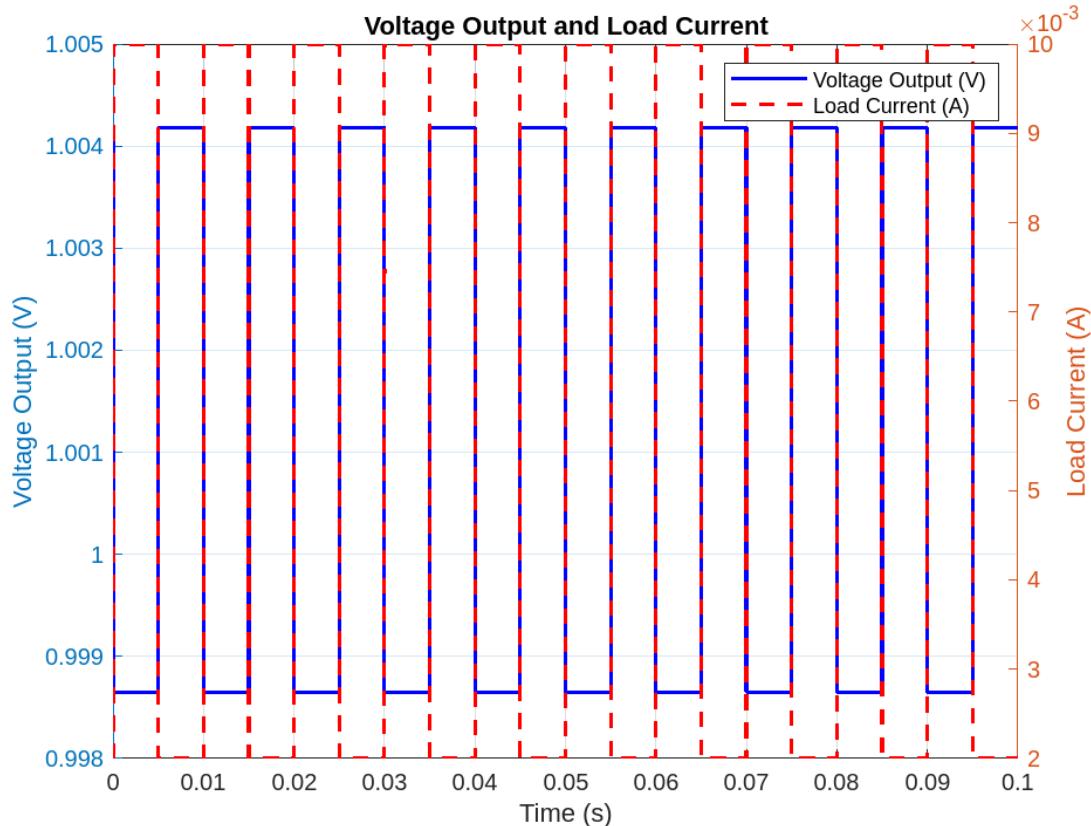


Figure 55: (Matlab) Transient simulation results.

9. Simulation vs. Hand Calculations

90nm: Compare simulation results with hand calculations using techplots. Highlight agreements and discrepancies in a table.

Table 24: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
Heavy Load Loop Gain (dB)	57.97	60	3.38
Light Load Loop Gain (dB)	58.57	60	2.38
Heavy Load PSRR (dB)	-55.25	-60	7.91
Light Load PSRR (dB)	-55.46	-60	7.56
Heavy Load gmro	37.44	36.8	1.73
Light Load gmro	37.3	36.8	1.35
Heavy Load Pole 1 (Hz)	409	411	0.48
Light Load Pole 1 (Hz)	82.8	86.5	4.27

135nm: Compare simulation results with hand calculations using techplots. Highlight agreements and discrepancies in a table.

Table 25: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
Heavy Load Loop Gain (dB)	62.149	60	3.58
Light Load Loop Gain (dB)	63.48	60	5.80
Heavy Load PSRR (dB)	-55.893	-60	6.84
Light Load PSRR (dB)	-56.24	-60	6.26
Heavy Load gmro	68.11	73.125	6.85
Light Load gmro	68.08	73.125	6.89
Heavy Load Pole 1 (Hz)	259.7	218	19.12
Light Load Pole 1 (Hz)	71	43.5	63.21

10. Internal Compensated

Loop gain:

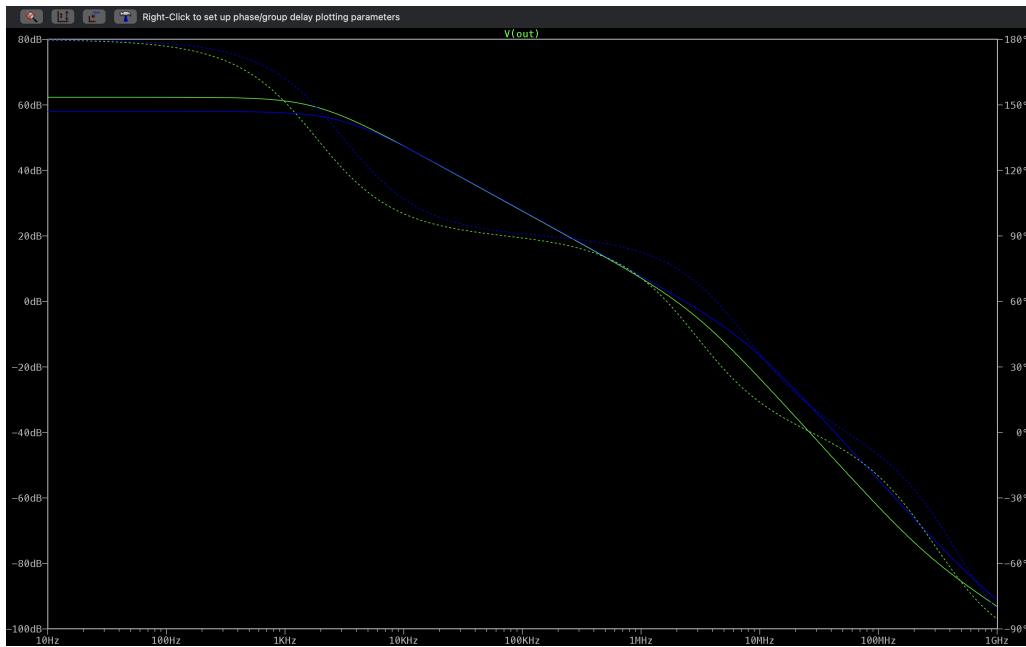


Figure 56: Transient simulation results.

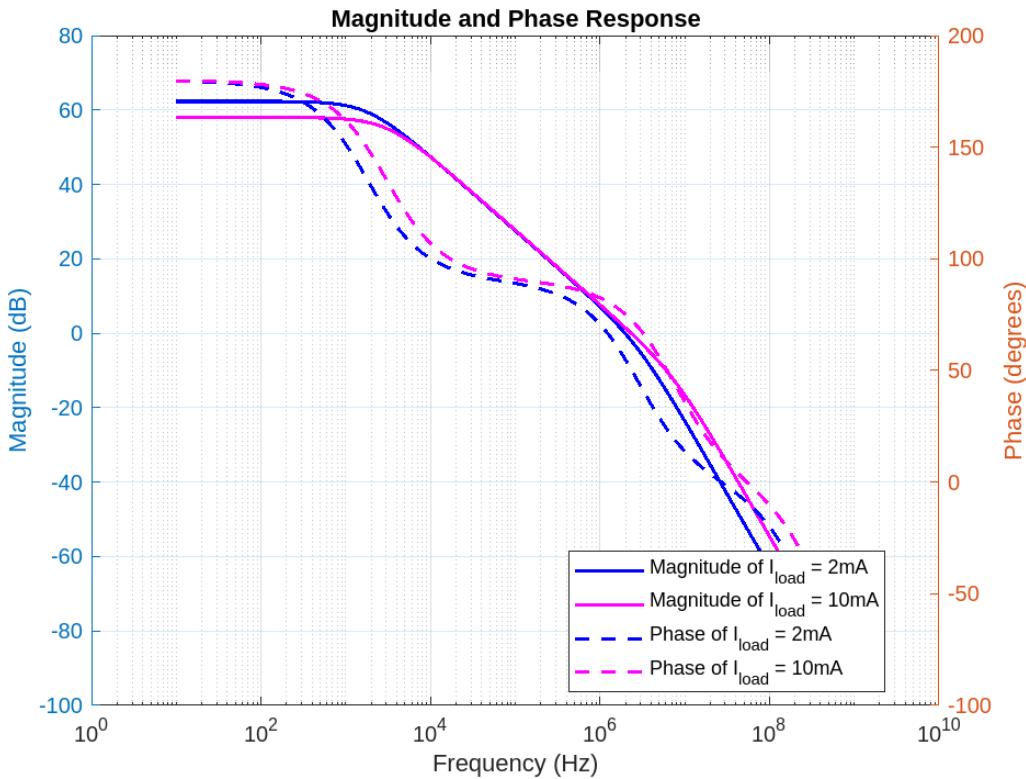


Figure 57: (Matlab) Transient simulation results.

Openloop PSRR :

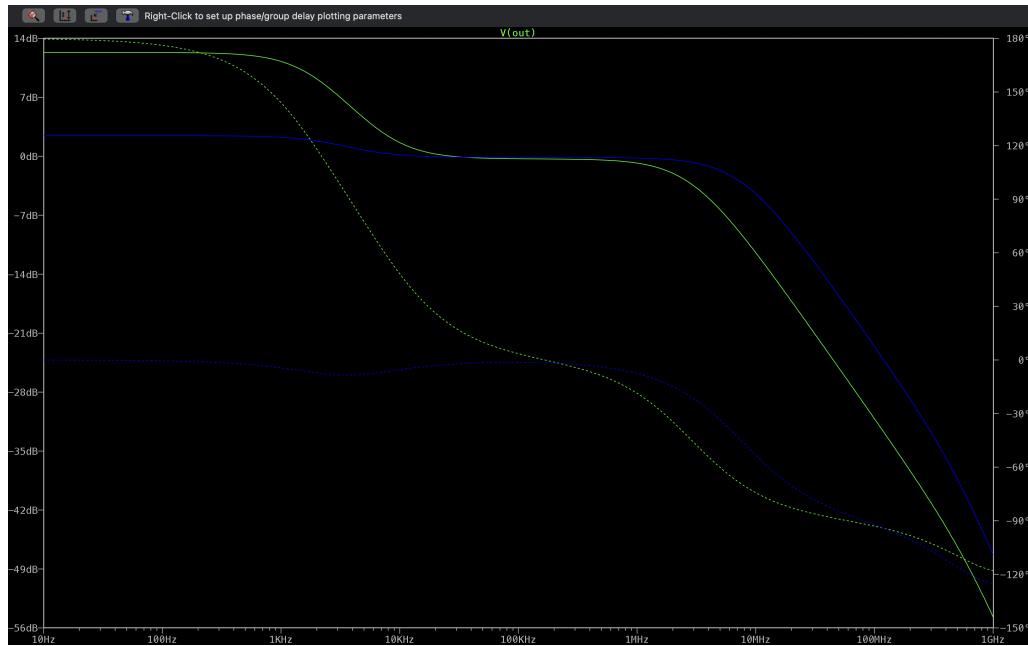


Figure 58: Transient simulation results.

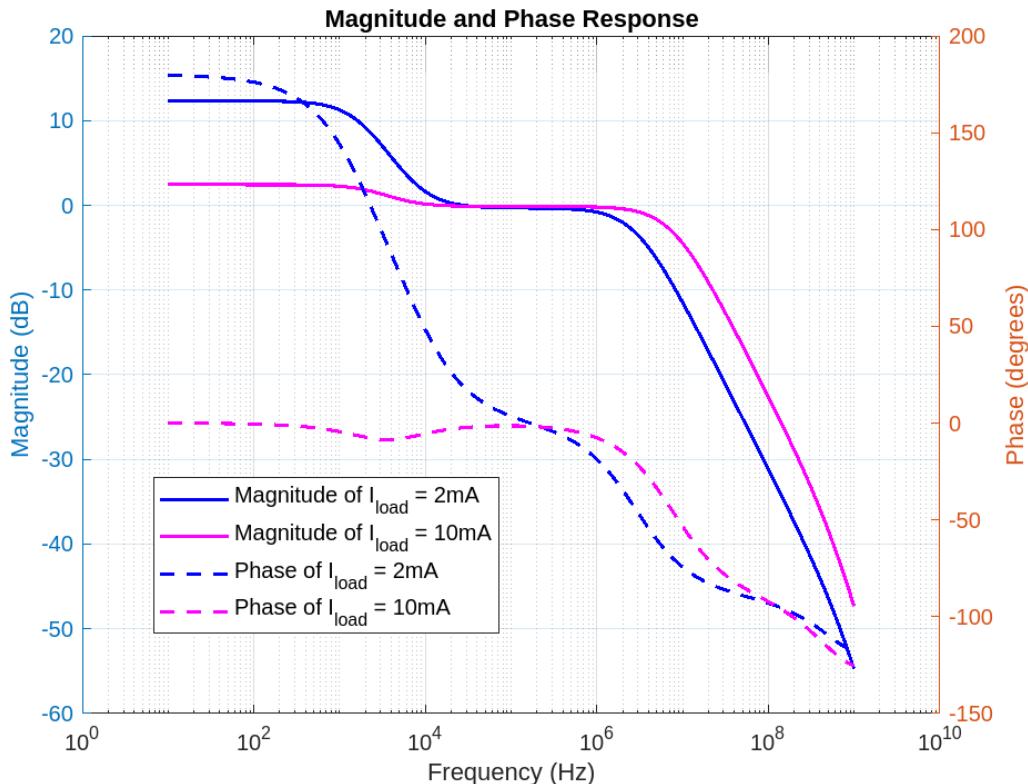


Figure 59: (Matlab) Transient simulation results.

Closeloop PSRR :

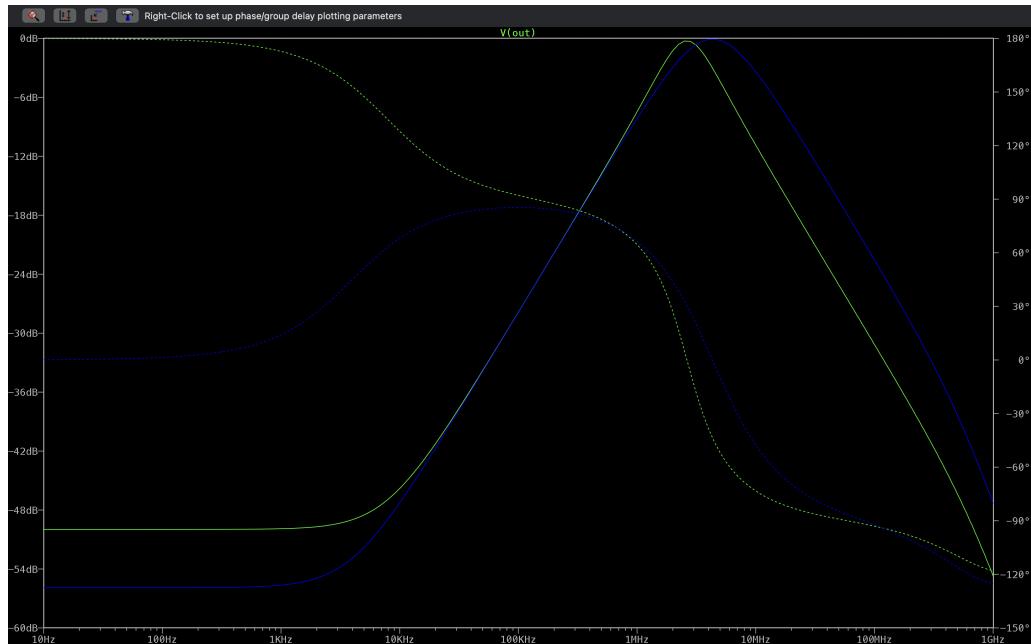


Figure 60: Transient simulation results.

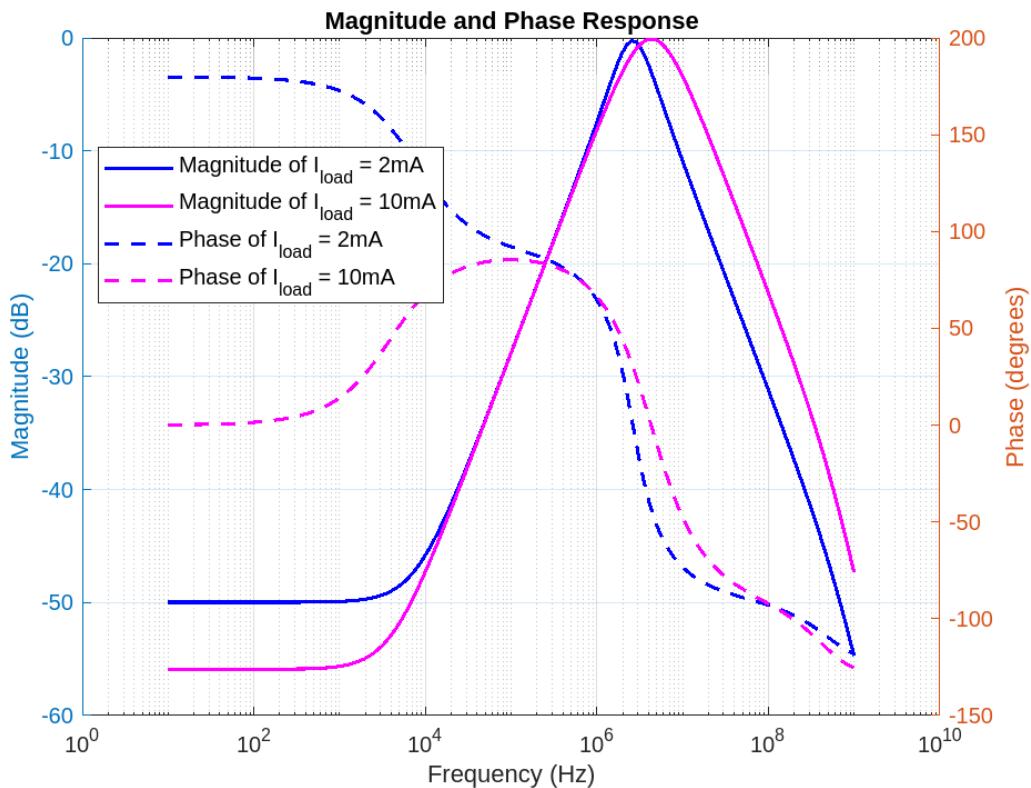


Figure 61: (Matlab) Transient simulation results.

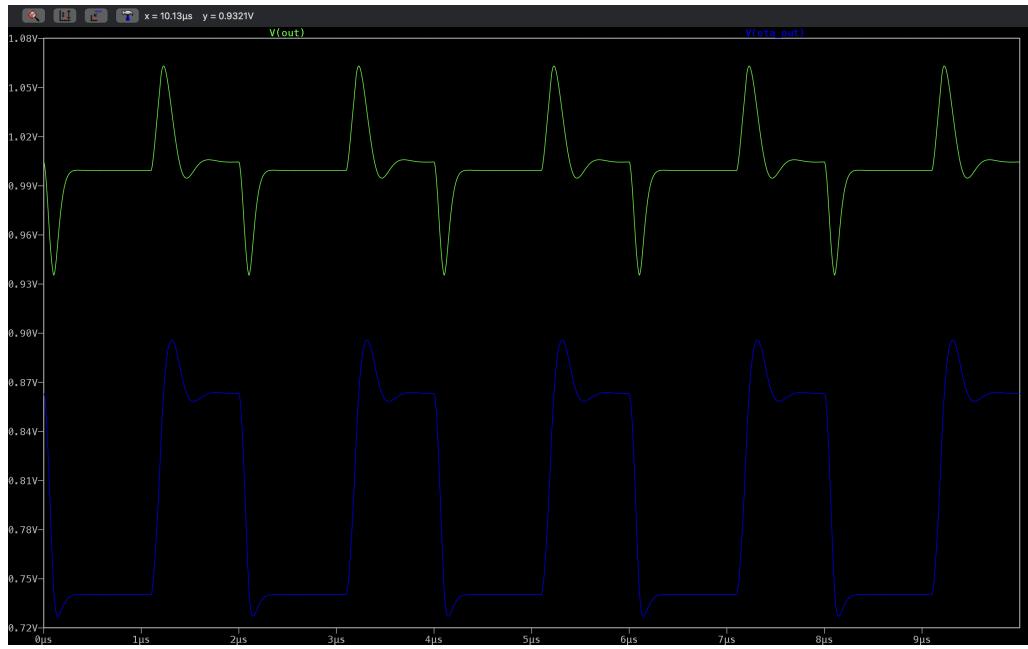
Transient Responce :

Figure 62: Transient simulation results.

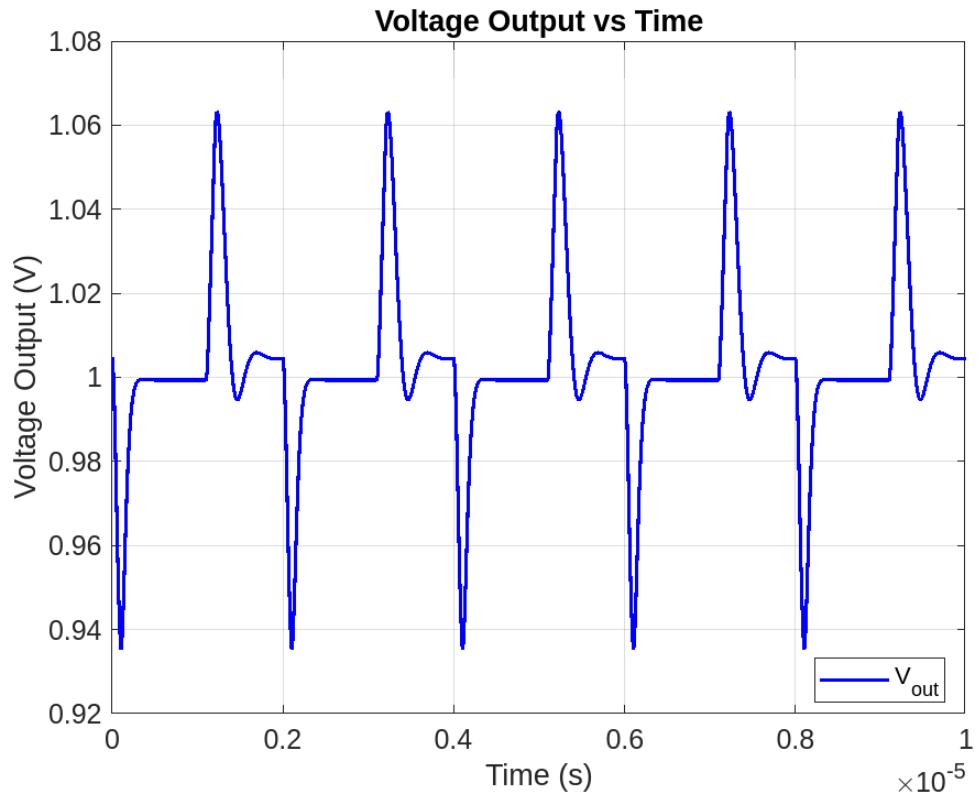


Figure 63: Transient simulation results.

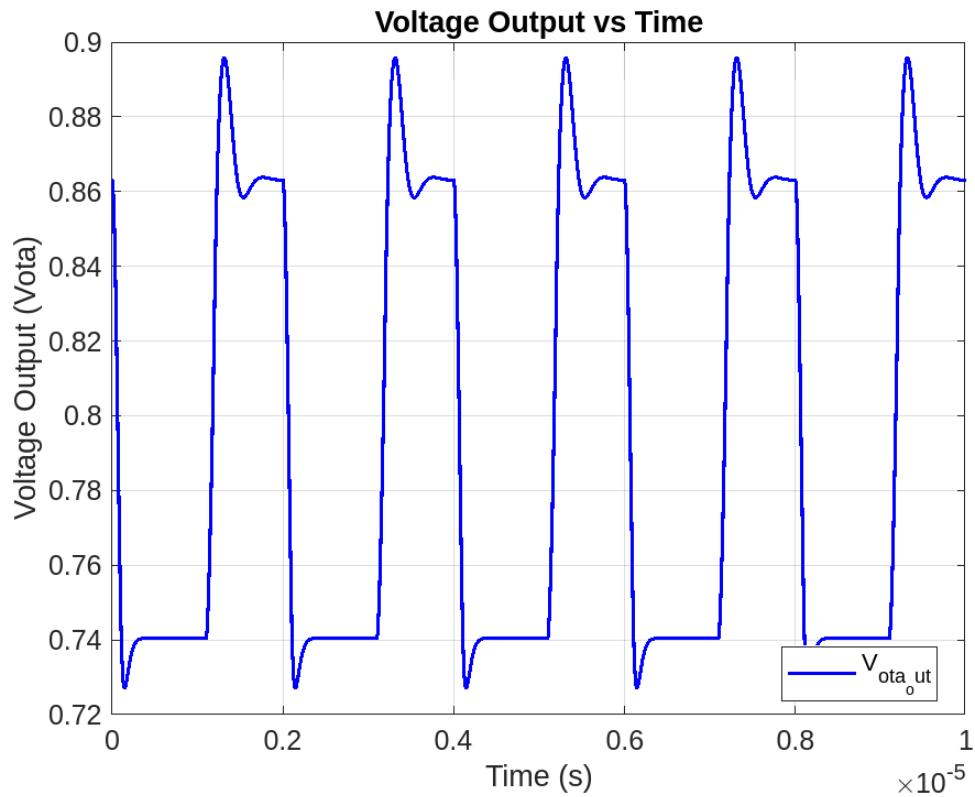


Figure 64: Transient simulation results.

C_c calculation: We get it from the formula $\mathbf{w}_{p2} = \mathbf{A} \cdot \mathbf{w}_{p1}$.

$$\mathbf{w}_{p2} = \frac{\mathbf{g}_{mpass}}{C_{load}}$$

$$\mathbf{w}_{p1} = \frac{1}{r_{odiff} \cdot \mathbf{A}_{pass} \cdot (C_c + C_{gd})}.$$