ANALOG TO DIGITAL CONVERTER (ADC) USING HITECH - PIC - 'C'

PIC-ADC Analog vs Digital

Digital Voltages:

Signal 0=0Volt,

Signal 1=5Volts

Vs

Analog Voltages:

0,1,2,3,..10,… and in fractions also like 2.7Volts, 9.9Volts etc.

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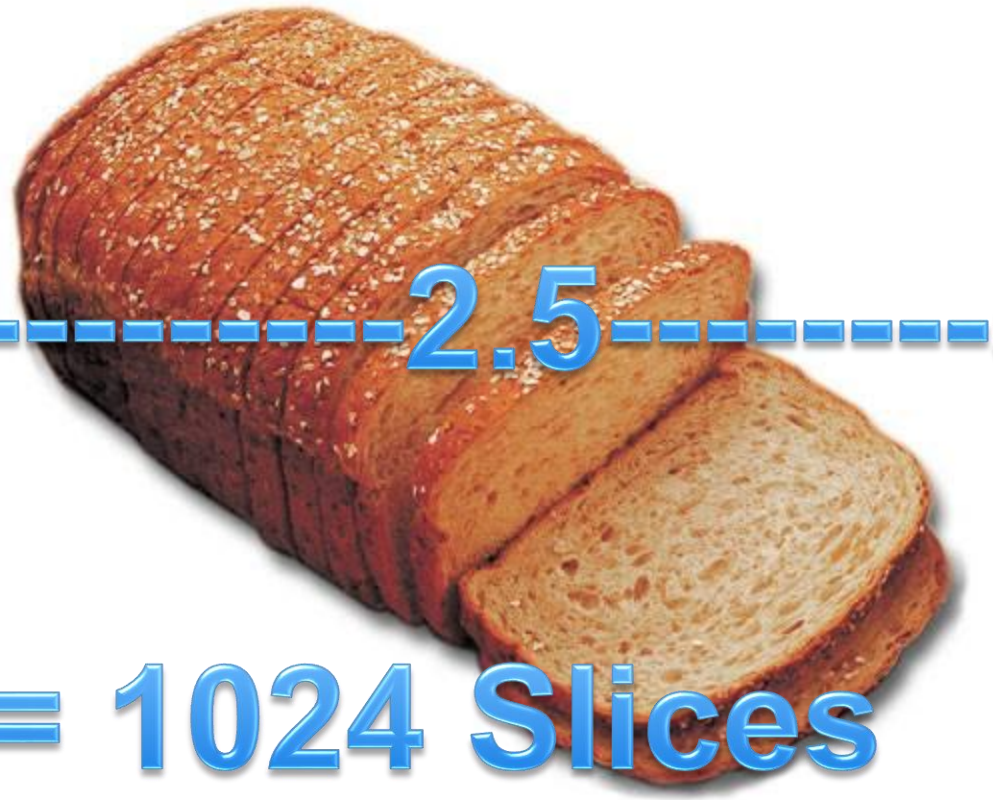
PIC-ADC Voltage Sampling



0---------2.5---------5V

10Bit = 1024 Slices

(Samplings)

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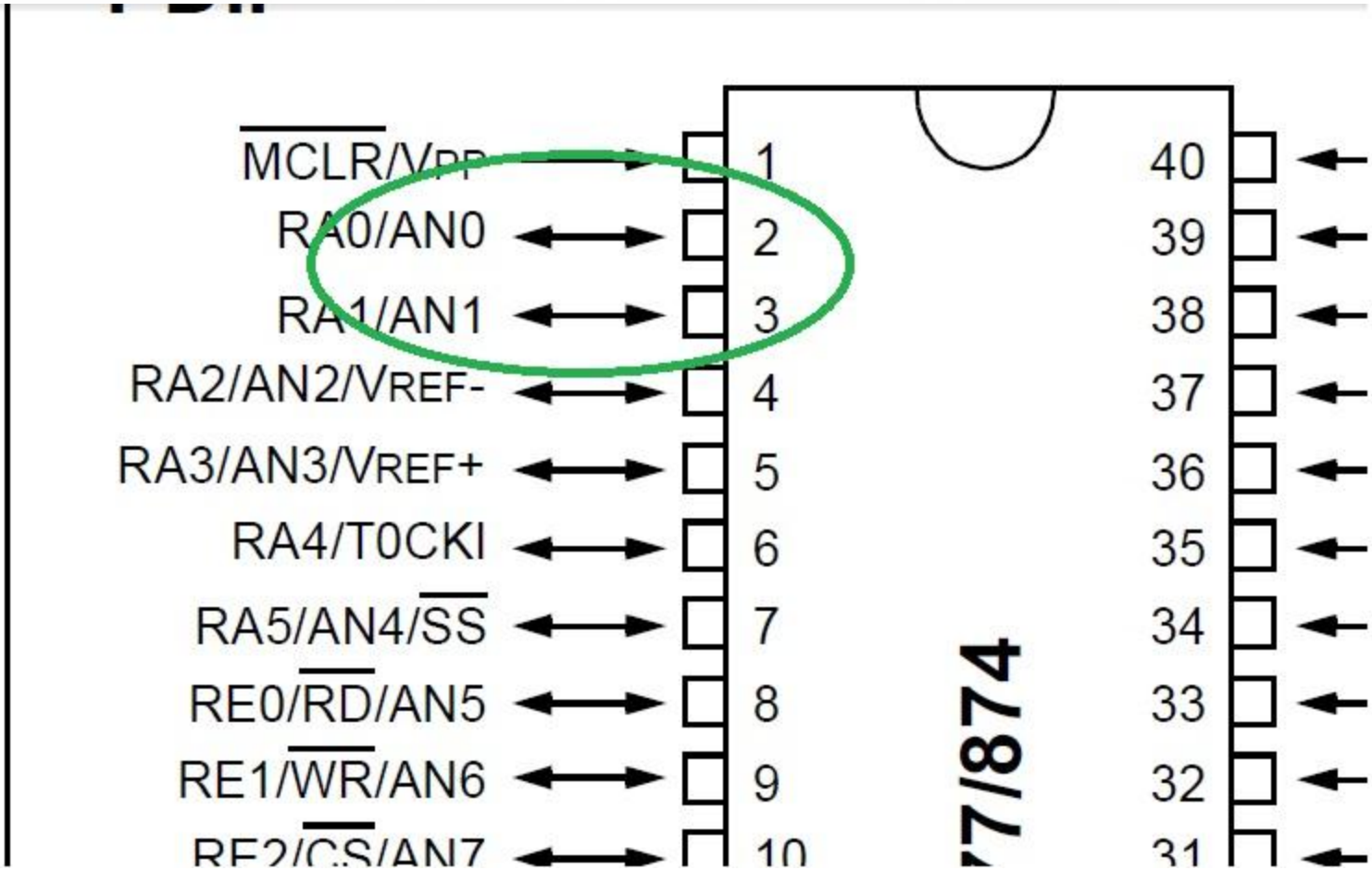
ADC Input Pins:



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ADC Registers

- ANSEL(ADC Selection Low)
- ANSELH(ADC Selection High)
- ADCON0 (ADC Enable)
- ADCON1 (ADC Setting)
- ADRESH (Converted Result High)
- ADRESL (Converted Result Low)

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ADCON0 Register:

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ADCS<1:0>: A/D Conversion Clock Select bits**
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

bit 5-2 **CHS<3:0>: Analog Channel Select bits**
0000 = AN0
0001 = AN1
0010 = AN2
0011 = AN3
0100 = AN4
0101 = AN5
0110 = AN6
0111 = AN7
1000 = AN8
1001 = AN9
1010 = AN10
1011 = AN11
1100 = AN12
1101 = AN13
1110 = CVREF
1111 = Fixed Ref (0.6V fixed voltage reference)

bit 1 **GO/$\overline{\text{DONE}}$: A/D Conversion Status bit**
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON: ADC Enable bit**
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

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ADCON1 Register

REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
ADFM	—	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM**: A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented**: Read as '0'

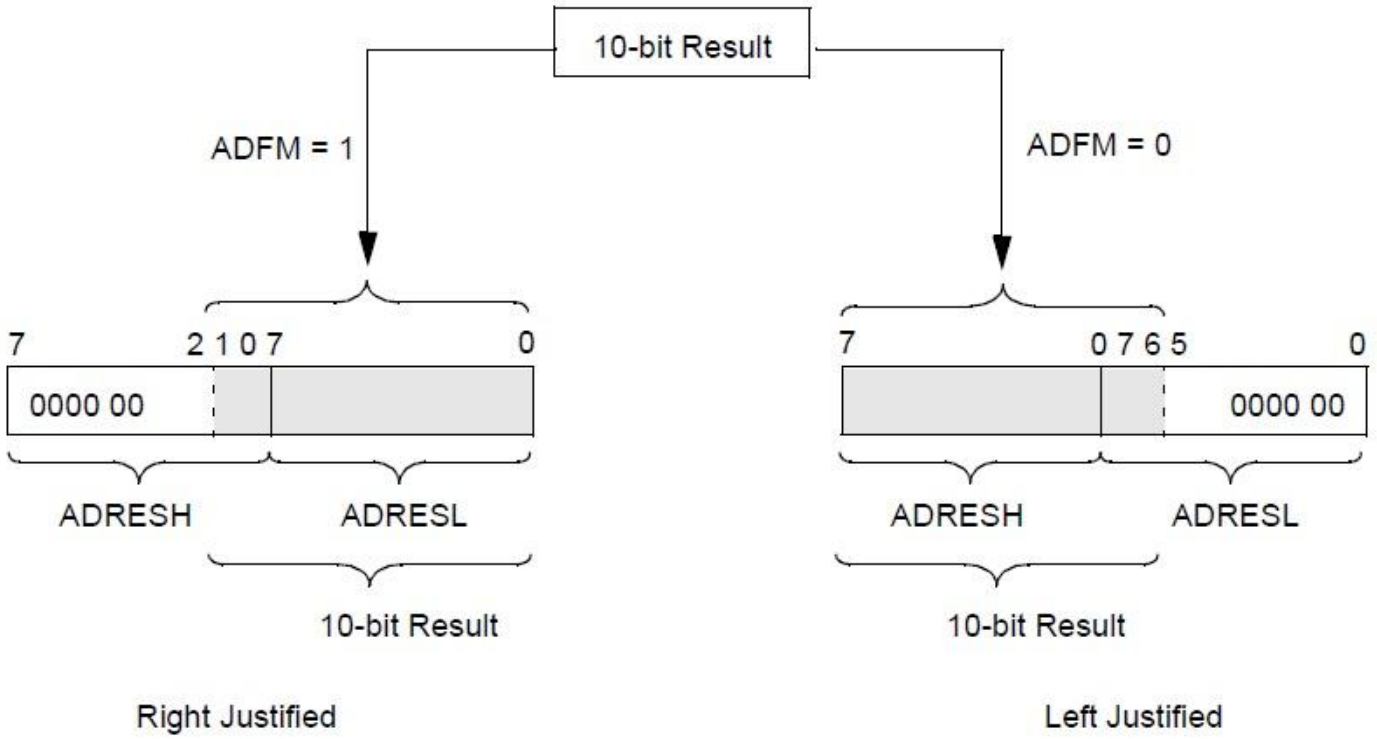
bit 5 **VCFG1**: Voltage Reference bit
1 = V_{REF-} pin
0 = V_{SS}

bit 4 **VCFG0**: Voltage Reference bit
1 = V_{REF+} pin
0 = V_{DD}

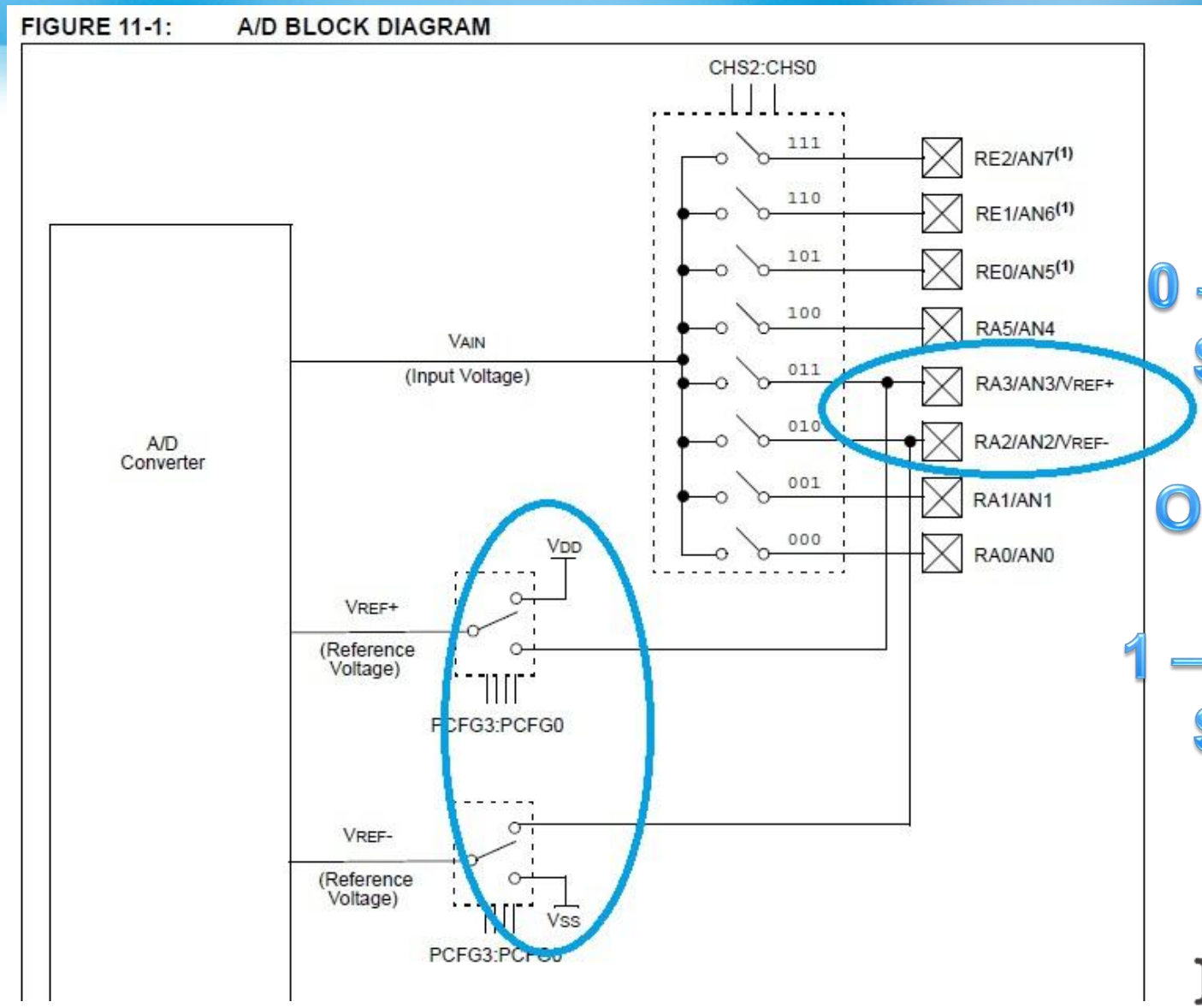
bit 3-0 **Unimplemented**: Read as '0'

Converted Result:

FIGURE 11-4: A/D RESULT JUSTIFICATION



Other Features: ADC Ref Pins



0 – 5V = 1024 Samplings

Or selectable

1 – 3.3V = 1024 Samplings

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Sample code to start with:

```
 void init()
 {
    ADCON0=ADCChannel; // select Fosc/32
    ADCON1=0b10000000; // Right Justified and No Reference pins
    ADON=1; // turn on the A2D conversion module
 }
unsigned int ReadADC(unsigned int Channel)
{
    InitADC(Channel);
   GO=1; // initiate conversion on the selected channel
   while(GO)continue;
   ADCLow=ADRESL;  // return of 8 LSB bits.
   ADCHigh=ADRESH; // return of 2 MSB bits.
   if(ADCHigh==0)ADCValue=ADCLow;
   if(ADCHigh==1)ADCValue=ADCLow+256;
   if(ADCHigh==2)ADCValue=ADCLow+512;
   if(ADCHigh==3)ADCValue=ADCLow+768;// Arrive ADCValue in 1 Variable.
   return ADCValue;
}
```

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QUERIES??

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