## Polarity and Clock Phase

The SPI interface defines no protocol for data exchange, limiting overhead and allowing for high speed data streaming. Clock polarity (CPOL) and clock phase (CPHA) can be specified as '0' or '1' to form four unique modes to provide flexibility in communication between master and slave as shown in Figure 2.

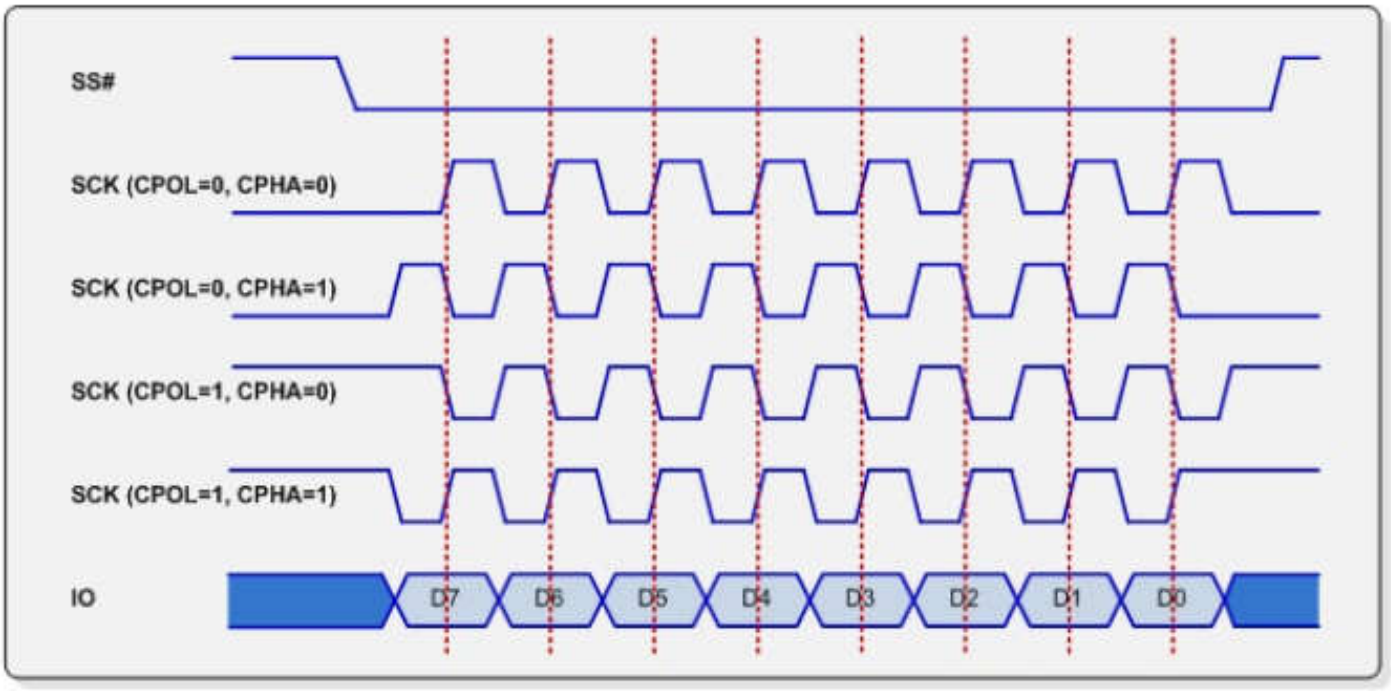


**Figure 2. SPI bus timing**

If CPOL and CPHA are both '0' (defined as Mode 0) data is sampled at the leading rising edge of the clock. Mode 0 is by far the most common mode for SPI bus slave communication. If CPOL is '1' and CPHA is '0' (Mode 2), data is sampled at the leading falling edge of the clock. Likewise, CPOL = '0' and CPHA = '1' (Mode 1) results in data sampled at on the trailing falling edge and CPOL = '1' with CPHA = '1' (Mode 3) results in data sampled on the trailing rising edge. Table 1 below summarizes the available modes.

| Mode | CPOL | CPHA |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

**Table 1. SPI mode definitions**