Clock Domain Crossing (CDC) Synchronizer using Verilog

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FPGA Design & Timing Closure Project

Abstract

Clock Domain Crossing (CDC) is an essential concept in FPGA and digital design where data needs to transfer safely between two asynchronous clock domains. This project demonstrates a 2-Flip-Flop synchronizer implemented in Verilog with Vivado XDC constraints to handle metastability and ensure reliable operation. The design includes a top-level wrapper, testbench, and timing constraints.

1. Introduction

In multi-clock systems, data transfer between asynchronous domains can cause metastability and unpredictable behavior. CDC techniques such as synchronizers and FIFOs are used to address these issues. This report focuses on implementing a simple 2-flop synchronizer for signal synchronization across two clock domains.

2. Objectives

- Implement a CDC synchronizer using Verilog. - Create XDC constraints for timing closure in Vivado. - Validate design through simulation and timing analysis.

3. Methodology

Tools Used: - Xilinx Vivado Design Suite - Verilog HDL - Simulation using Vivado Simulator Steps: 1. Design RTL for 2-FF synchronizer. 2. Create a top-level wrapper for synthesis. 3. Apply XDC constraints for multiple clocks. 4. Perform simulation to verify functionality.

4. RTL Design

cdc_sync.v: module cdc_sync (input wire clk_dest, input wire async_in, output reg sync_out); reg sync_ff1; always @(posedge clk_dest) begin sync_ff1 <= async_in; sync_out <= sync_ff1; end endmodule top.v: module top (input wire clk_src, input wire clk_dest, input wire async_in, output wire sync_out); cdc_sync u1 (.clk_dest(clk_dest), .async_in(async_in), .sync_out(sync_out)); endmodule

5. Vivado XDC Constraints

create_clock -name clk_src -period 10.000 [get_ports {clk_src}] create_clock -name clk_dest -period 14.000 [get_ports {clk_dest}] set_clock_groups -asynchronous -group {clk_src} -group {clk_dest} set_false_path -from [get_clocks clk_src] -to [get_clocks clk_dest] set_false_path -from [get_clocks clk_dest] -to [get_clocks clk_src]

6. Simulation & Results

Simulation demonstrates correct signal synchronization across asynchronous clocks using a 2-FF synchronizer. The waveform shows removal of metastability after two clock cycles in the destination domain. (Insert waveform screenshot here)

7. Timing Analysis

Vivado timing report shows no critical path violations after applying CDC constraints. Slack is positive, ensuring timing closure. (Insert timing summary screenshot here)

8. Applications

- Multi-clock FPGA systems - SoC interconnects - Communication interfaces (Ethernet, PCIe) - High-speed data transfer systems

9. Conclusion

This project successfully demonstrates a safe method for crossing asynchronous clock domains using a 2-flop synchronizer and Vivado timing constraints. It helps prevent metastability issues, improving the reliability of FPGA designs.

10. References

- Xilinx Vivado Design Suite User Guide - FPGA Prototyping by Verilog Examples - Xilinx CDC Design Techniques