

Date:**EXPERIMENT NO. 1****AIM: Study of logic gates (AND, OR, NOT, NAND, NOR, EX-OR) using ICs****SIMULATION WEBSITE:** <https://www.tinkercad.com/>**Components:**

Sr No.	Component	Specification	Quantity
1	AND Gate	IC 7408	1
2	OR Gate	IC 7432	1
3	NOT Gate	IC 7404	1
4	NAND Gate	IC 7400	1
5	NOR Gate	IC 7402	1
6	EX-OR Gate	IC 7486	1

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND & NOT are basic gates. NAND, NOR, X-OR are known as universal gates. Basic gates can be obtained from all this gates.

AND Gate:

The AND gate performs a logical multiplication commonly known as AND function. The output is high only when both the inputs are either one high or one low. When both the inputs are high the output is low level.

OR Gate:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high and the output is low level when both the inputs are low.

NOT Gate:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND Gate:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low. The output is low level when the inputs are high.



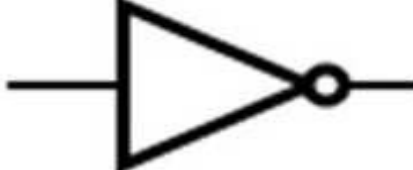

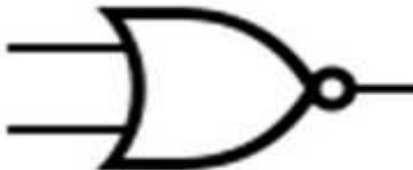

NOR Gate:

The NOR gate is contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

EX-OR Gate:

The output is high when any one of the input is high. The output is also low when both the inputs are low and both inputs are high.

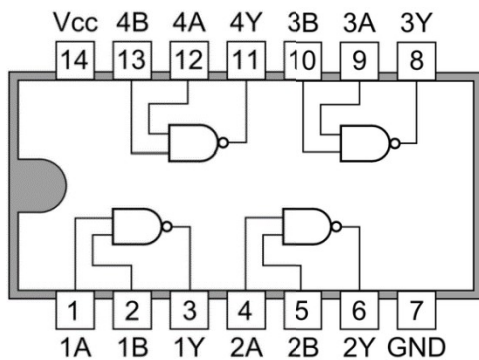
Digital Logic Gate Symbols

GATE	SYMBOL	NOTATION	TRUTH TABLE																		
<u>AND</u>		$A \cdot B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A AND B</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	INPUT		OUTPUT	A	B	A AND B	0	0	0	0	1	0	1	0	0	1	1	1
INPUT		OUTPUT																			
A	B	A AND B																			
0	0	0																			
0	1	0																			
1	0	0																			
1	1	1																			
<u>OR</u>		$A + B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A OR B</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	INPUT		OUTPUT	A	B	A OR B	0	0	0	0	1	1	1	0	1	1	1	1
INPUT		OUTPUT																			
A	B	A OR B																			
0	0	0																			
0	1	1																			
1	0	1																			
1	1	1																			
<u>NOT</u>		\overline{A}	<table><tr><th>INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>NOT A</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	INPUT	OUTPUT	A	NOT A	0	1	1	0										
INPUT	OUTPUT																				
A	NOT A																				
0	1																				
1	0																				
<u>NAND</u>		$\overline{A \cdot B}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A NAND B</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	INPUT		OUTPUT	A	B	A NAND B	0	0	1	0	1	1	1	0	1	1	1	0
INPUT		OUTPUT																			
A	B	A NAND B																			
0	0	1																			
0	1	1																			
1	0	1																			
1	1	0																			
<u>NOR</u>		$\overline{A + B}$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A NOR B</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	INPUT		OUTPUT	A	B	A NOR B	0	0	1	0	1	0	1	0	0	1	1	0
INPUT		OUTPUT																			
A	B	A NOR B																			
0	0	1																			
0	1	0																			
1	0	0																			
1	1	0																			
<u>XOR</u>		$A \oplus B$	<table><tr><th colspan="2">INPUT</th><th>OUTPUT</th></tr><tr><th>A</th><th>B</th><th>A XOR B</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	INPUT		OUTPUT	A	B	A XOR B	0	0	0	0	1	1	1	0	1	1	1	0
INPUT		OUTPUT																			
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0	0	0																			
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1	1	0																			

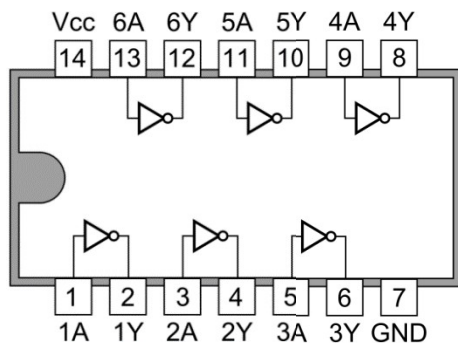
LOGIC GATES USING IC:

IC's PIN DIAGRAMS:

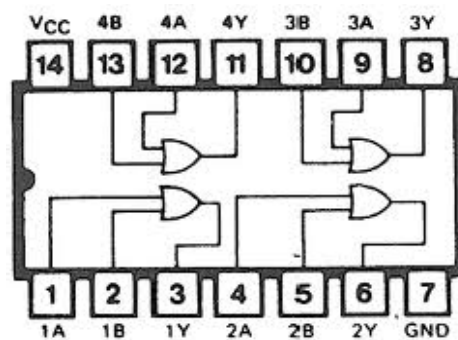
7400 Quad 2-input NAND Gates



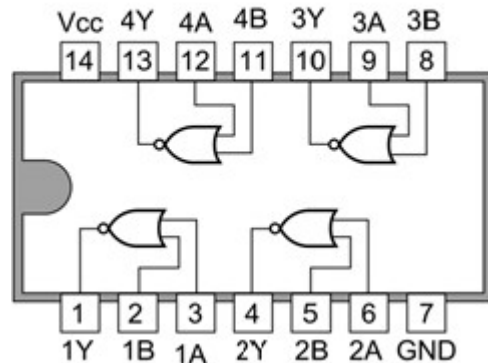
7404 Hex Inverters



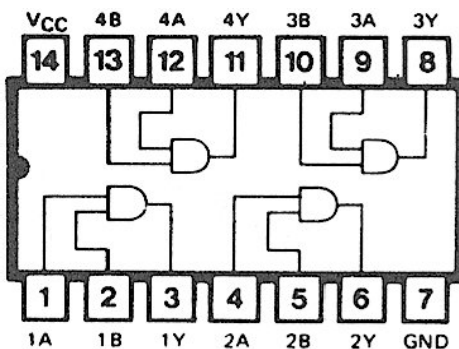
7432 OR Gates



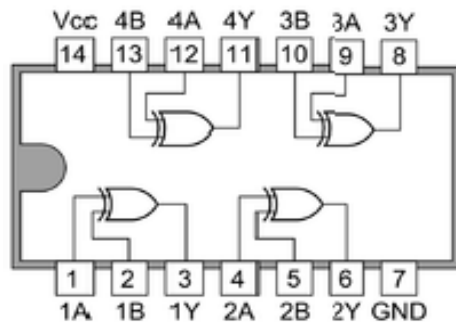
7402 Quad 2-input NOR Gates



7408 AND Gates



7486 Quad 2-input ExOR Gates



PROCEDURE:

- i) Do the connection as per IC Pin diagram. Connect Vcc (Pin 14) and Ground (Pin 7) with Power supply properly.
- ii) Apply Logical inputs as per truth table with considering Positive Logic (0V for 0 input and 5V for 1 input).
- iii) Observe and record the output voltage using DMM or test whether LED is on or off using LED tester in observation table.
- iv) Verify the working of gates by comparing the truth table and observation table.
- v) Repeat all the steps for each gate and complete the observation table.

OBSERVATION TABLES:

(i) Logic gates using IC:

Input A	Input B	Output of Gates				
		AND	OR	NAND	NOR	X-OR
0 (0V)	0 (0V)					
0 (0V)	1 (5V)					
1 (5V)	0 (0V)					
1 (5V)	1 (5V)					

For NOT Gate:

Input A	Output
0 (0V)	
1 (5V)	

OBSERVATIONS:

CONCLUSION:**Obtained Marks:****Faculty Sign:****Date:****ASSIGNMENT:**

1. List out various vendors or company names who are manufacturing various ICs.
2. What are different logic families using which logic gates ICs are manufactured?
3. Draw circuit diagrams of NAND and NOR gates using TTL and CMOS logic families and compare performance of both.