CHAPTER 6
SEQUENTIAL LOGIC

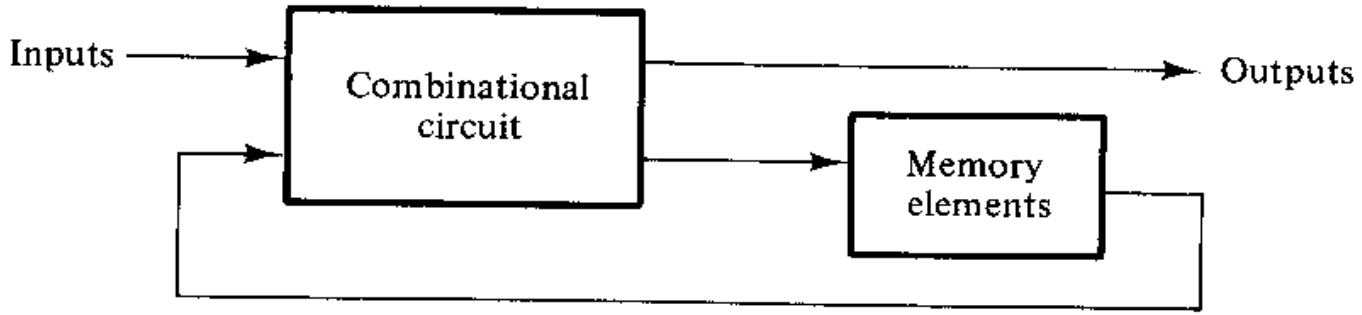
INTRODUCTION

Combinational Circuits: A circuit whose output, at any instant of time are dependent upon the input present at that time.

i.e. Half Adder, Full Adder

Sequential Circuits: A circuit whose output depends not only on the present inputs but also on the past history of inputs.

i.e. Flipflop



- The memory element is devices capable of storing binary information within them.
- The input is provided by external input.
- These inputs, together with the present state of the memory elements, determine the binary value at the Output terminal as well as the condition for changing the state in the memory elements.

Types of Sequential Circuits:

Synchronous Sequential Circuit: is a system whose behavior can be defined from the knowledge of its signals at discrete instant of time.

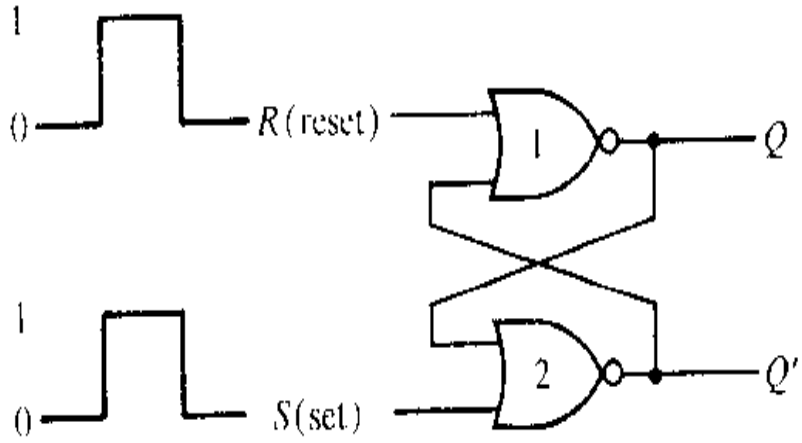
Asynchronous Sequential Circuit: is a system whose behavior depends upon the order in which its input signals change and can be affected at any instant of time.

Clocked Sequential Circuit: Synchronous Sequential Circuits that use clock pulses in the inputs of memory elements are called Clocked Sequential Circuit.

FlipFlops:

- The memory elements used in sequential circuits are called as FlipFlops.
- These circuits are binary cells capable of storing **one bit** of information.
- A FlipFlop has **two outputs**, one for the **normal value** and one for the **complement value** of the bit stored in it.

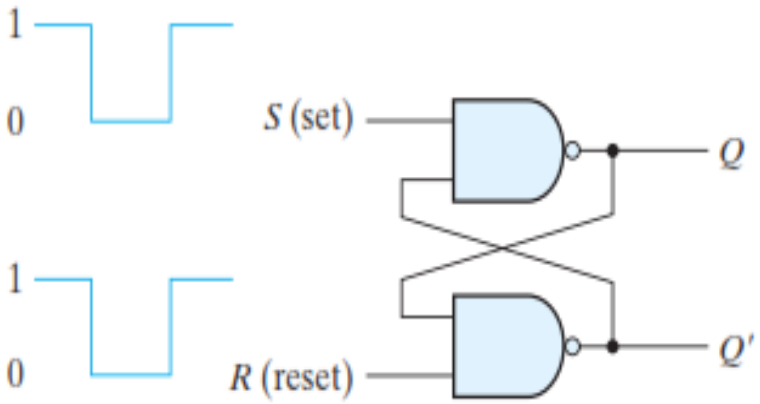
- FlipFlop circuit can be constructed from two NAND gates or two NOR gates.
- The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path.
- Each FlipFlop has two outputs, Q and Q', and two inputs SET and RESET.
- This type of FlipFlop is called DIRECT COUPLED RS FLIPFLOPS or SR LATCH.



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

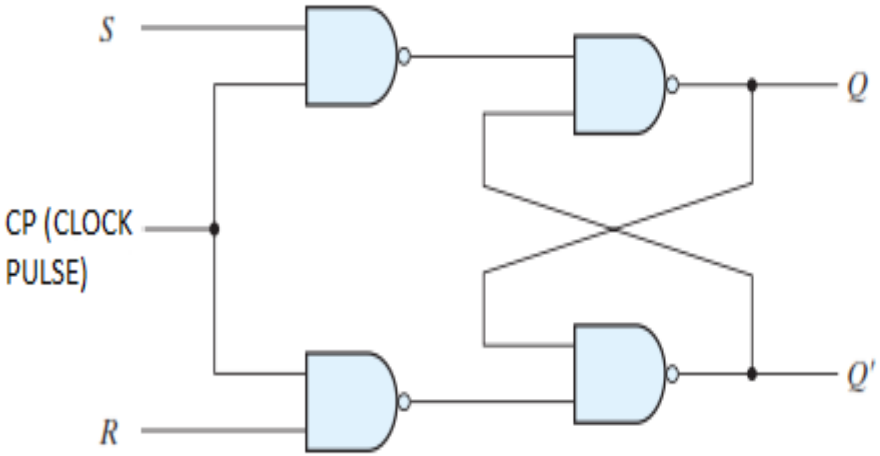
(b) Truth table



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table



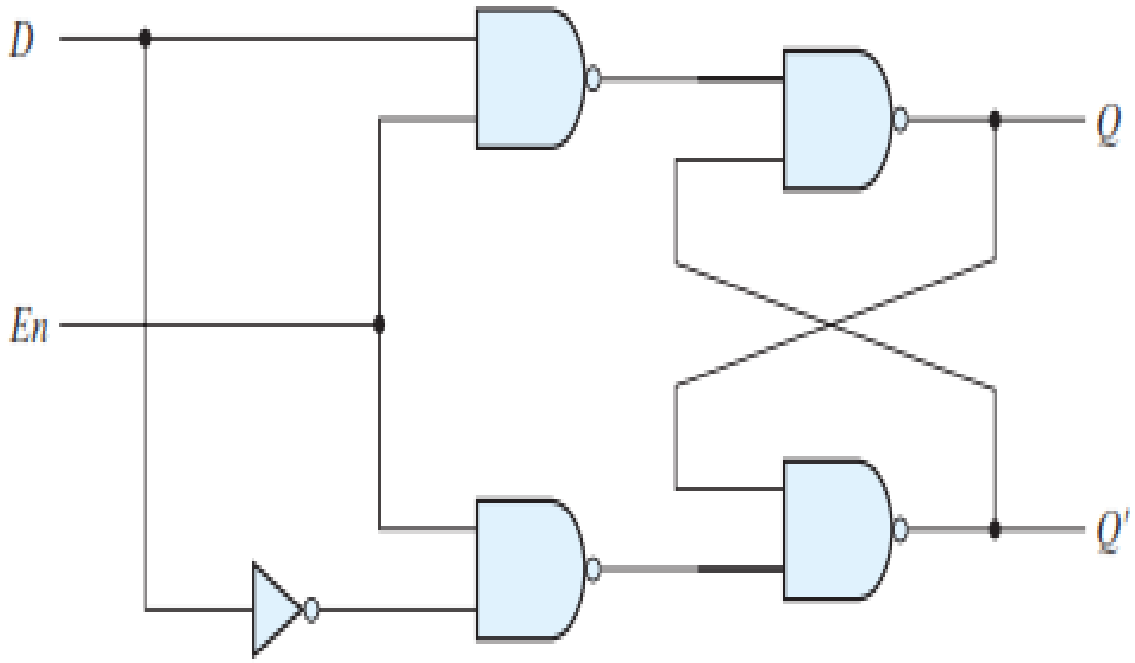
(a) Logic diagram

CP	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

SR latch with control input

D FLIP-FLOP

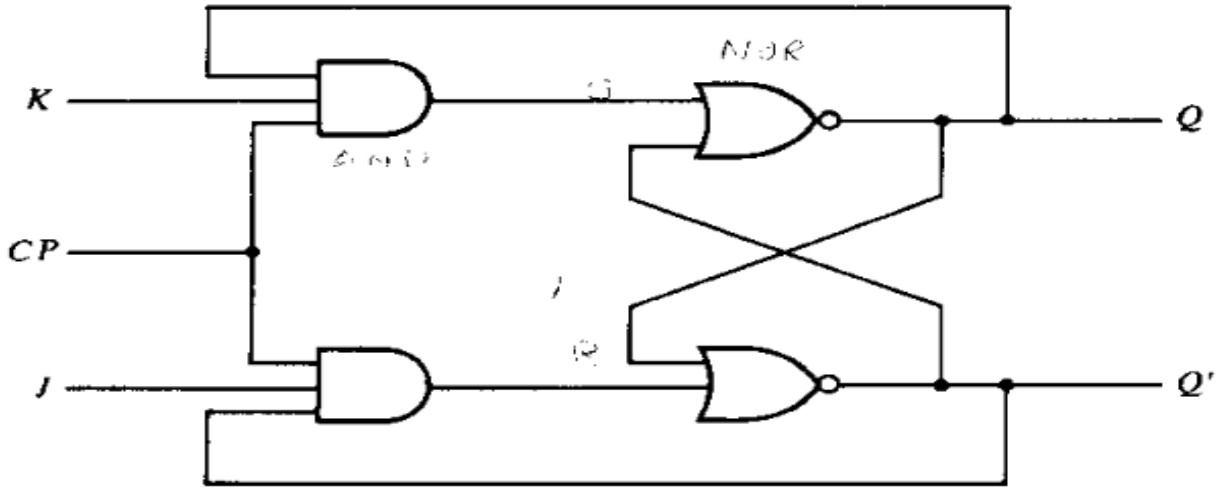


(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

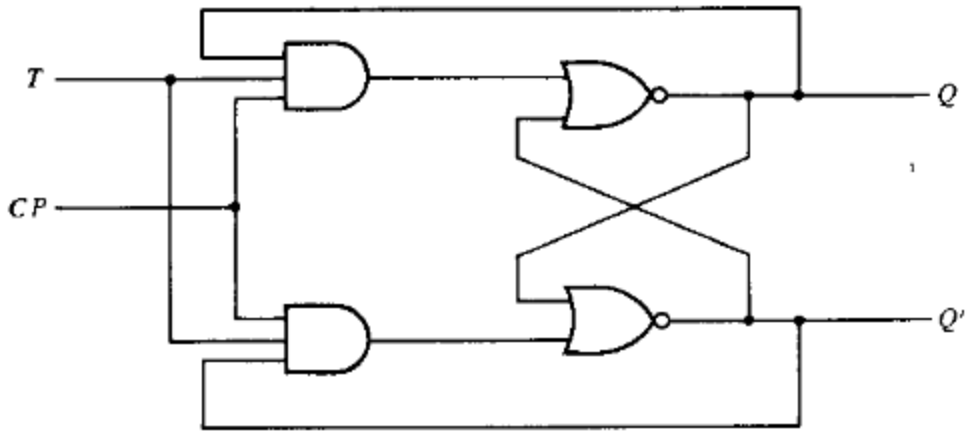
JK FLIP-FLOP



Q	J	K	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Characteristic table

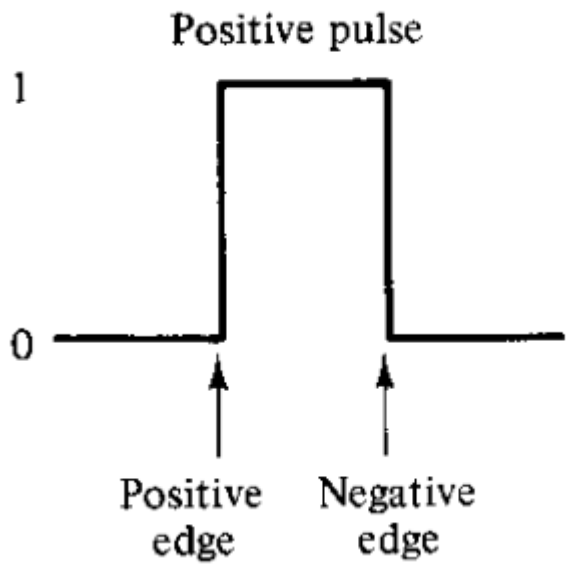
T FLIP FLOP

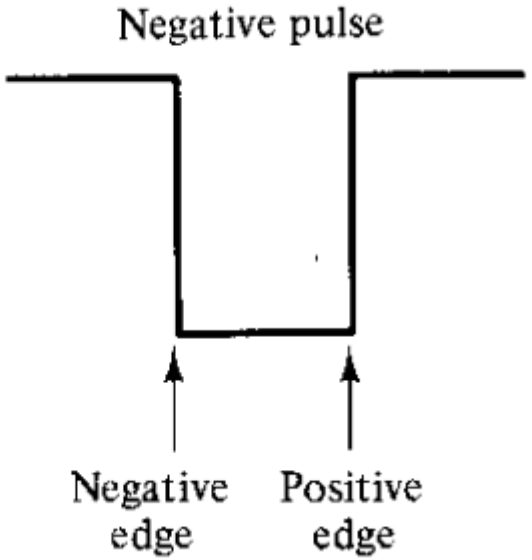


Q	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

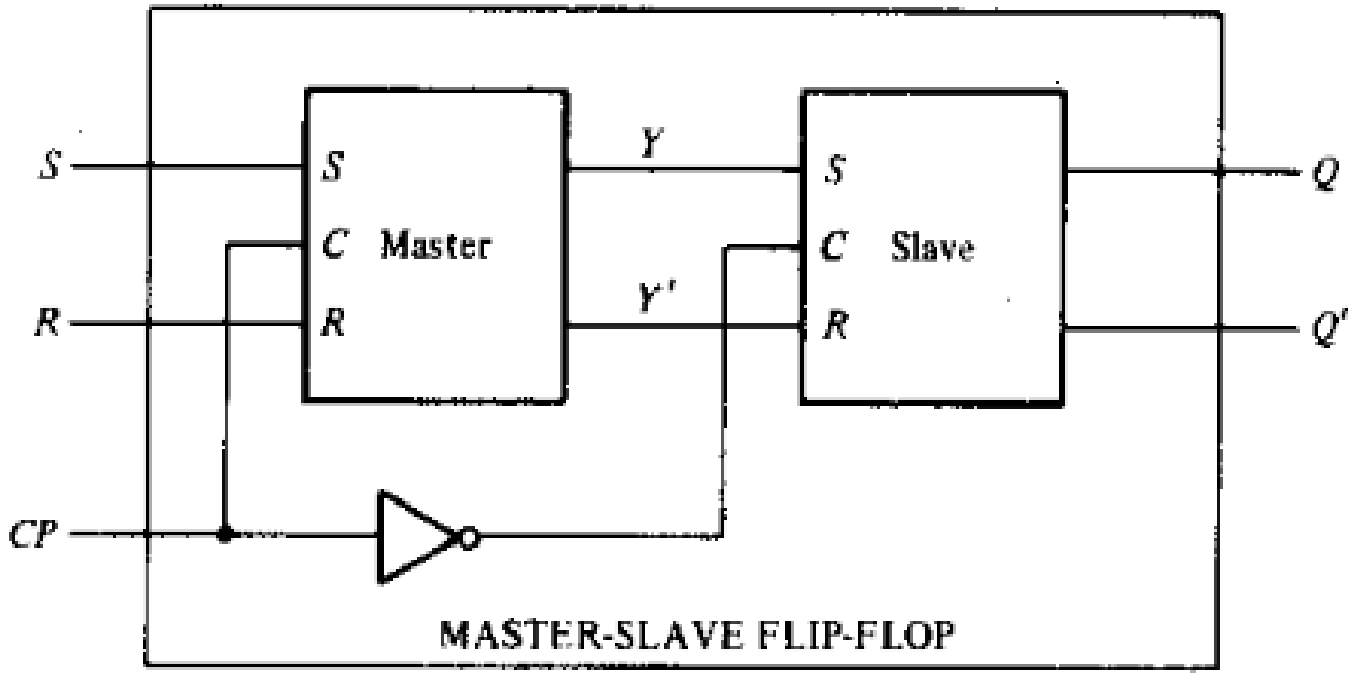
Characteristic table

TRIGGERING OF FLIP FLOPS

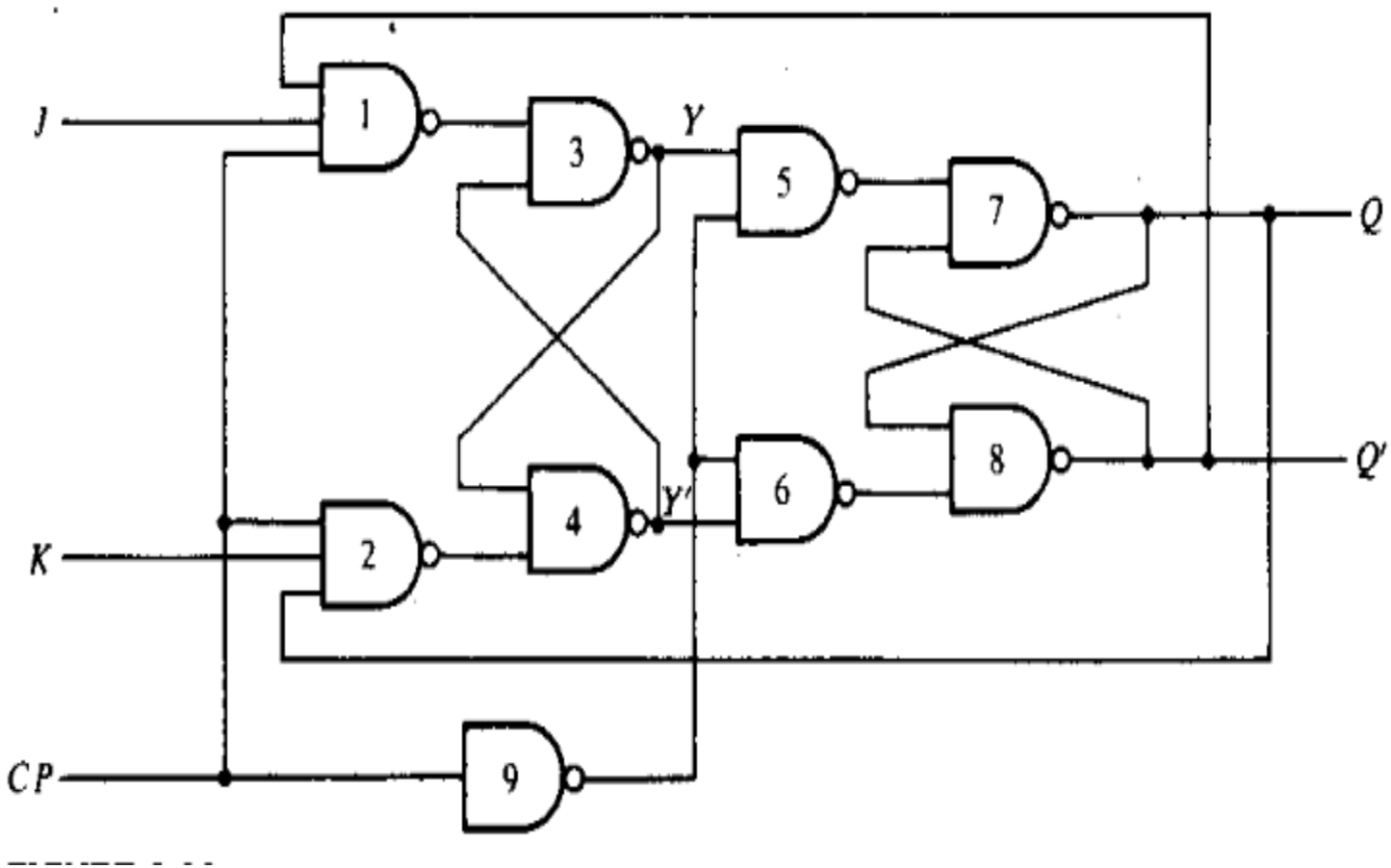




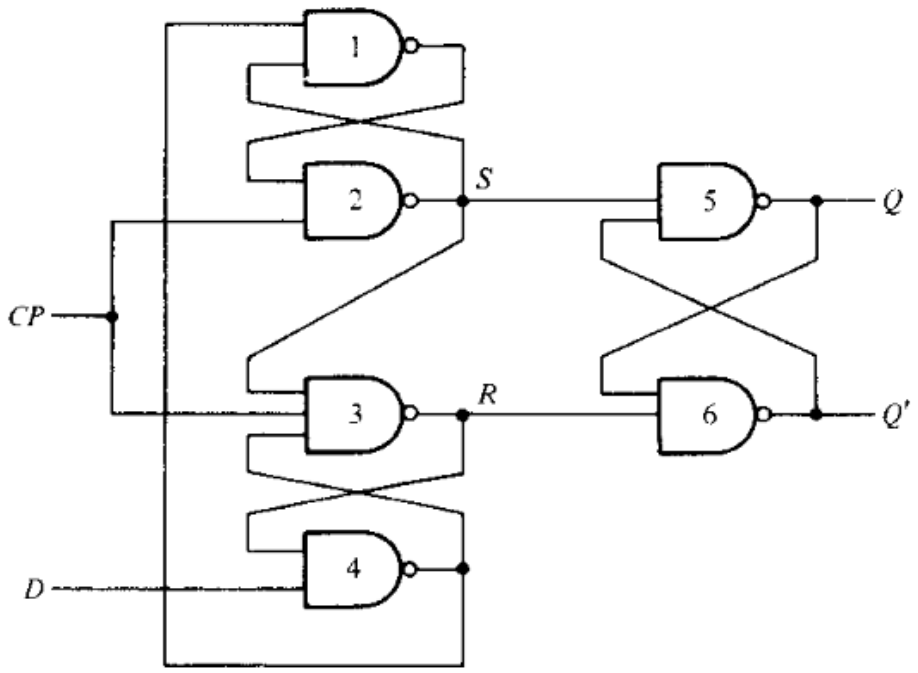
MASTER SLAVE FLIP-FLOP



MASTER SLAVE FLIP-FLOP

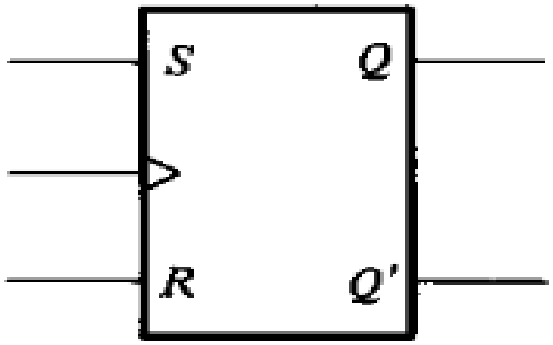


EDGE-TRIGGERED FLIP-FLOP

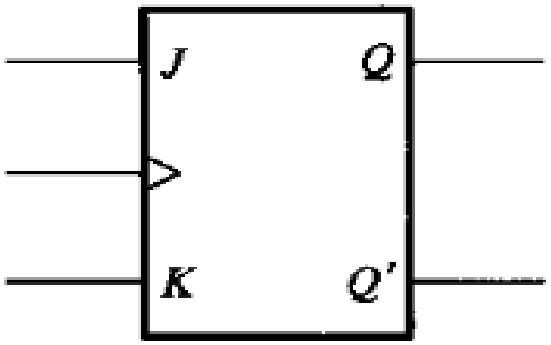


- CP = 0 => S & R = 1 => STEADY STATE OUTPUT
- D = 0 & CP = 1 => S = 1, R = 0 => Q = 0
- D = 1 & CP = 1 => S = 0, R = 1 => Q = 1

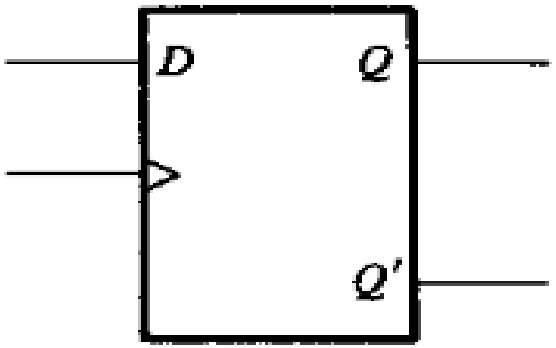
Graphic Symbols



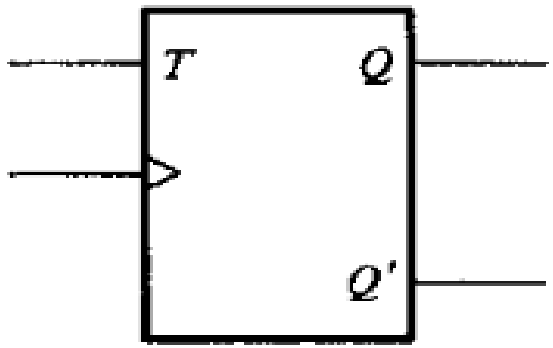
(a) *RS*



(b) *JK*

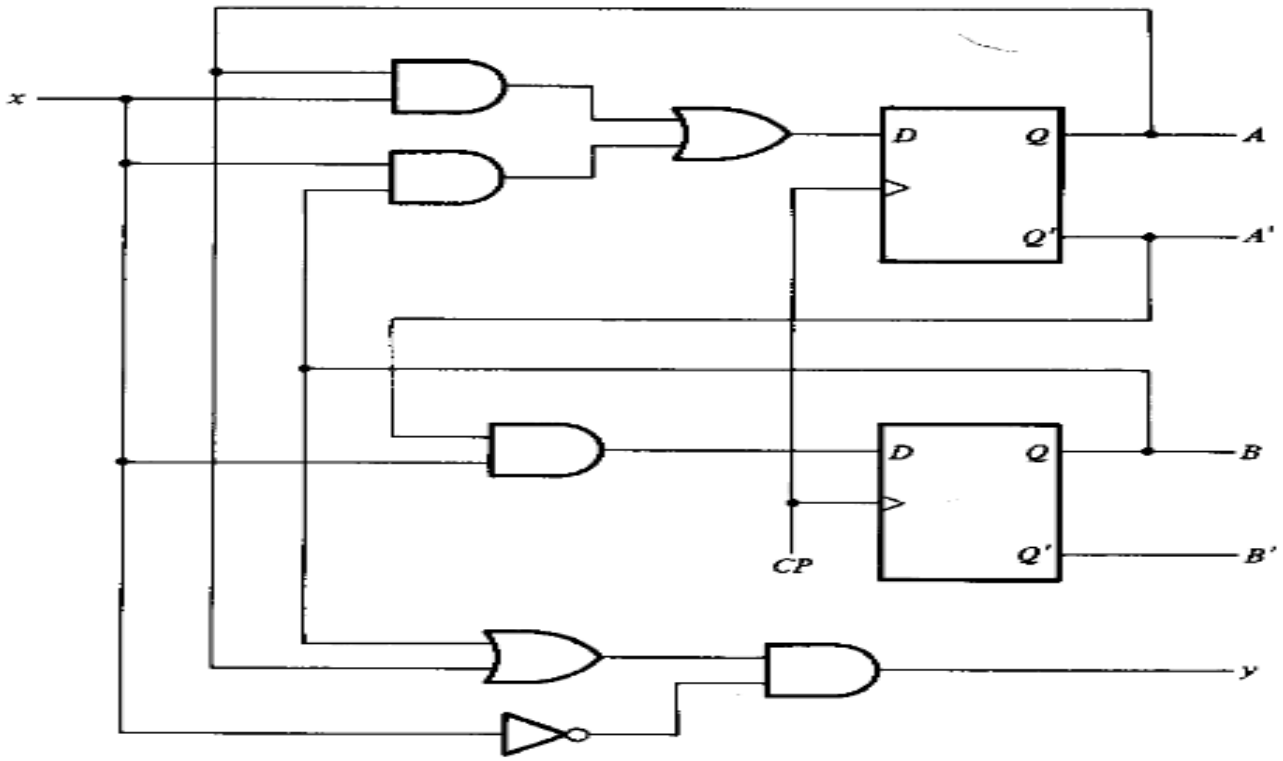


(c) *D*



(d) *T*

Analysis of Clocked Sequential Circuit



$$A(t+1) = Ax + Bx$$

$$B(t+1) = A'x$$

$$y = (A + B)x'$$

State - Table

State Table for the Circuit

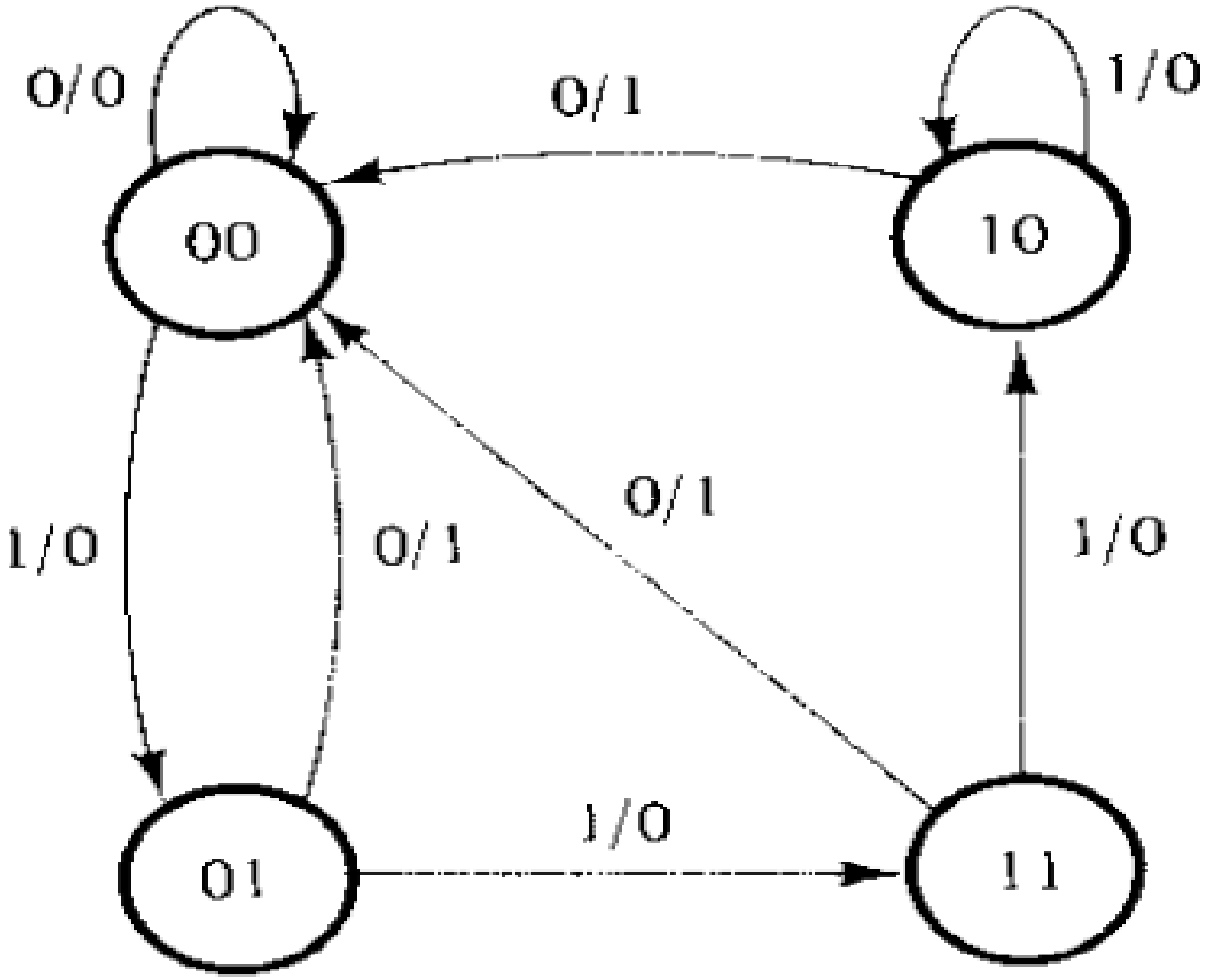
Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

State - Table

Second Form of the State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
AB	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

State Diagram

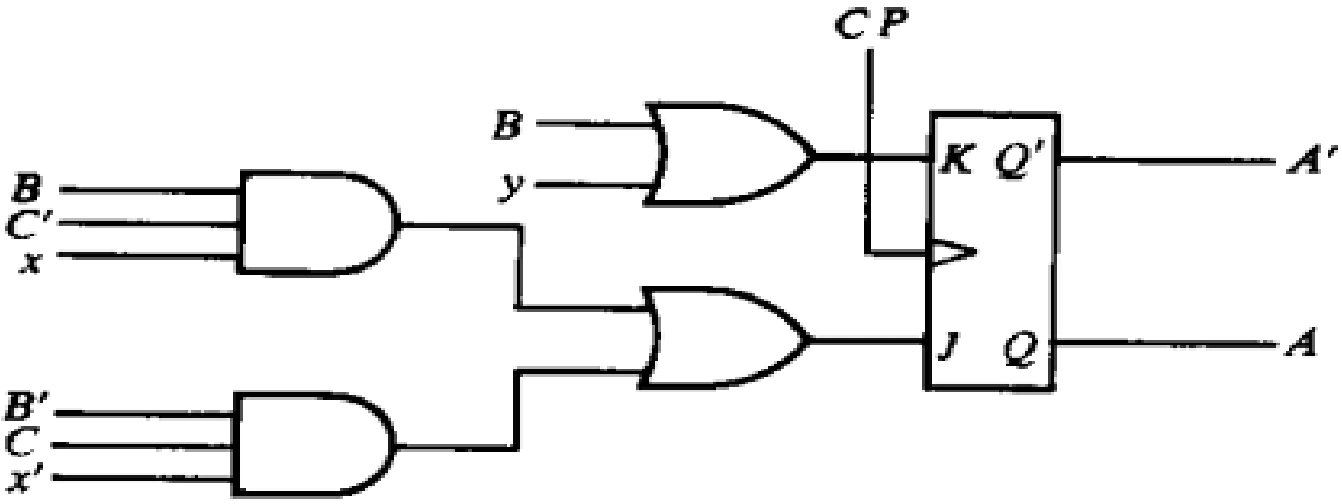


Flip – Flop Input Function

$$JA = BC'x + B'Cx'$$

$$KA = B + y$$

$$y = (A + B)x'$$



Flip – Flop Characteristic Tables

Flip-Flop Characteristic Tables

JK Flip-Flop

J	*K*	*Q*(*t* + 1)	
0	0	*Q*(*t*)	No change
0	1	0	Reset
1	0	1	Set
1	1	*Q*′(*t*)	Complement

RS Flip-Flop

S	*R*	*Q*(*t* + 1)	
0	0	*Q*(*t*)	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Unpredictable

D Flip-Flop

D	*Q*(*t* + 1)	
0	0	Reset
1	1	Set

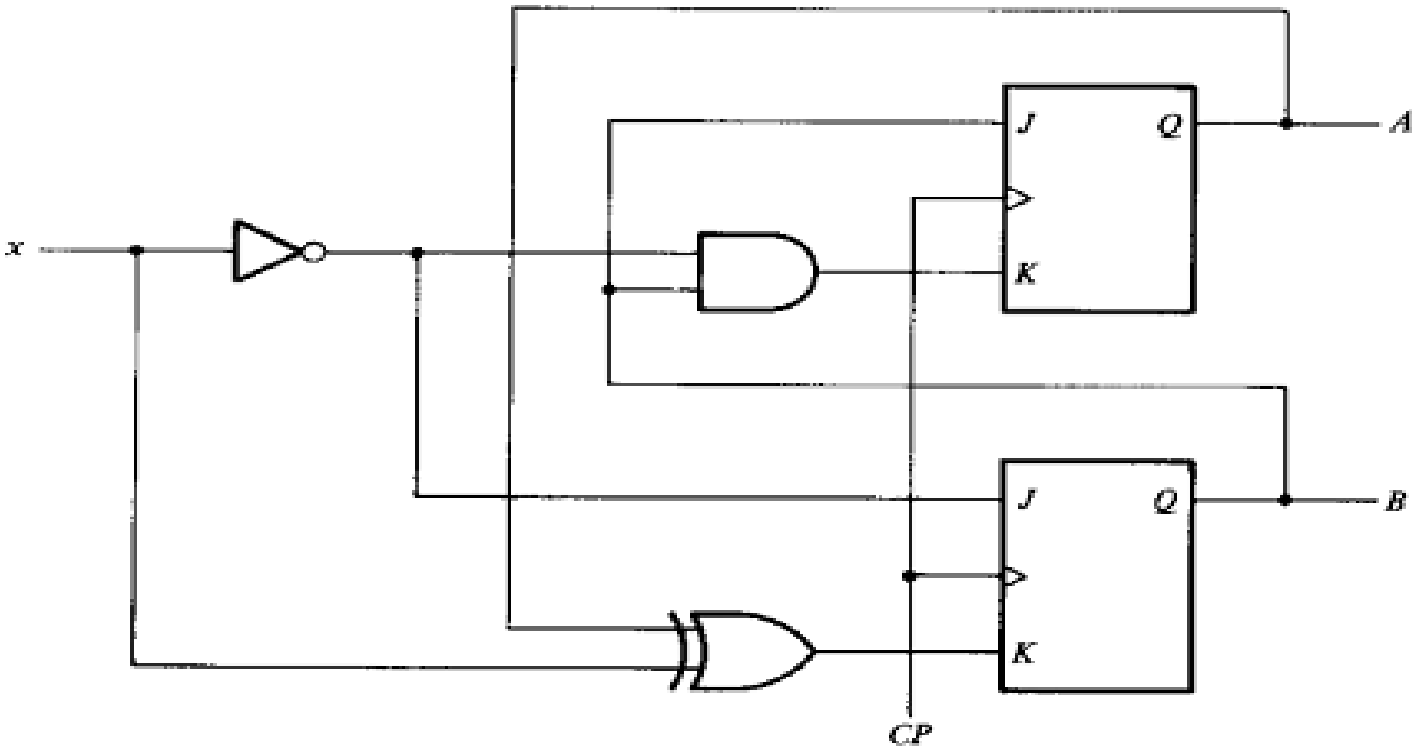
T Flip-Flop

T	*Q*(*t* + 1)	
0	*Q*(*t*)	No change
1	*Q*′(*t*)	Complement

Sequential Circuit With J-K Flip-Flop

$$JA = B \qquad JB = x'$$

$$KA = Bx' \qquad KB = A'x + Ax' = A \oplus x$$

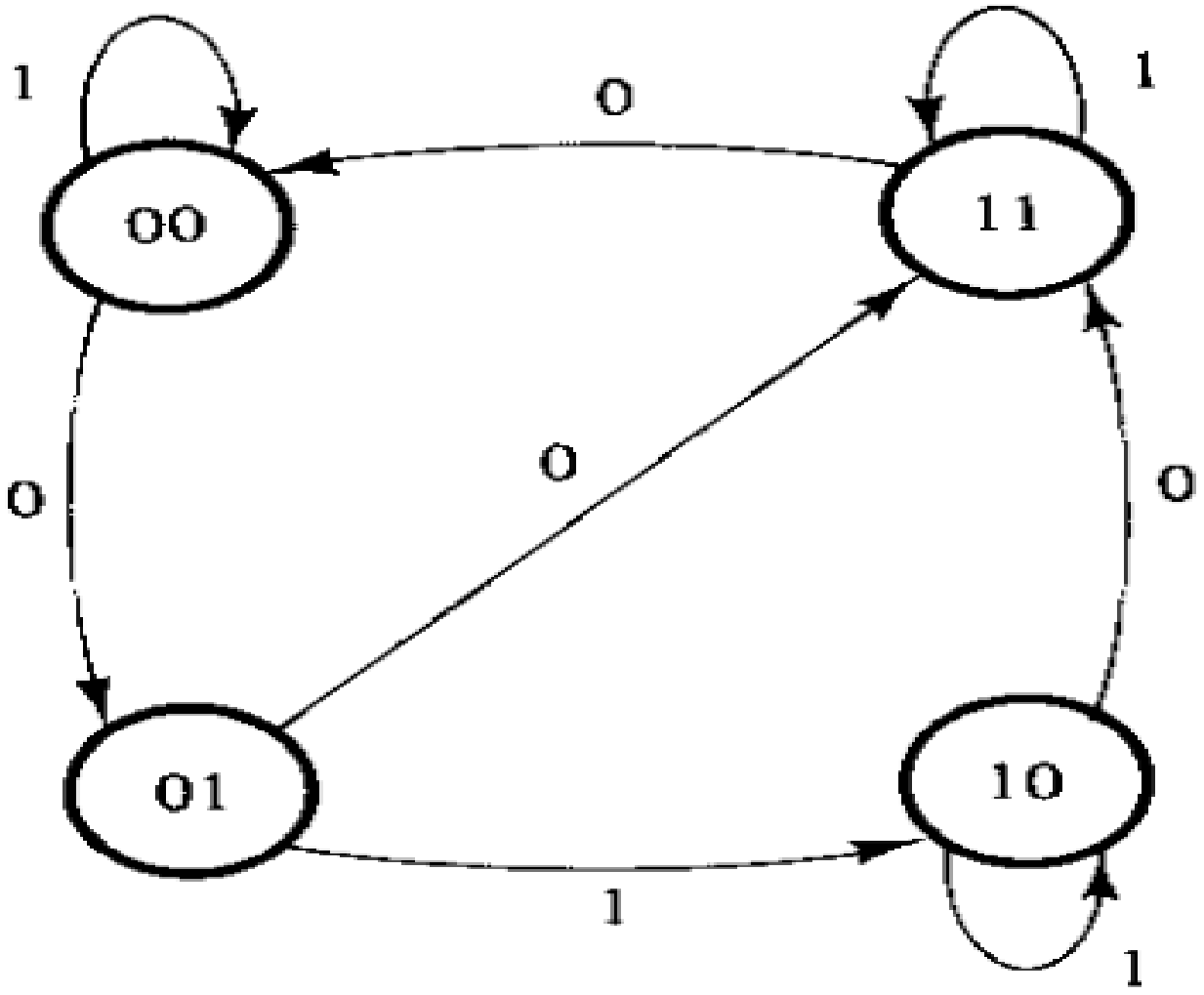


Sequential Circuit With J-K Flip-Flop

State Table for Sequential Circuit with *JK* flip-Flops

Present state		Input	Next state		Flip-flop inputs			
A	*B*	*x*	*A*	*B*	*JA*	*KA*	*JB*	*KB*
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Sequential Circuit With J-K Flip-Flop



Mealy & Moore Models

- **Mealy Model**

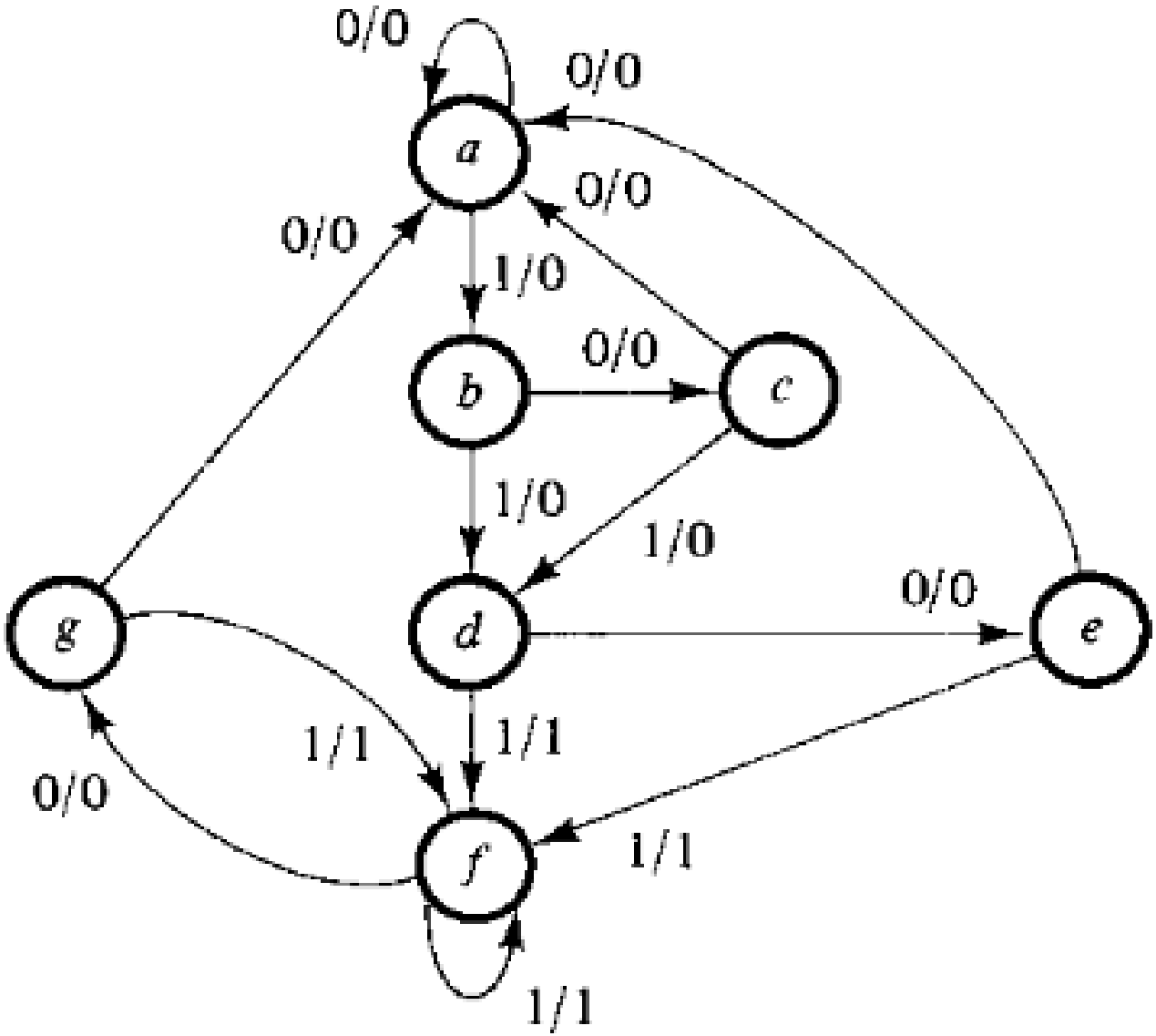
- The outputs are functions of both the **Present state & Inputs**
- In figure 6.16, output Y is function of both input X & the present state of A & B
- The outputs may change if the inputs change during the clock pulse period.

Mealy & Moore Models

- **Moore Model**

- The outputs are a function of the **Present state only**
- In figure 6.19, the output is taken from flipflop and are a function of present state only
- The outputs of sequential circuit are synchronized with the clock because they depend on only flipflop outputs that are synchronized with the clock

State Reduction and Assignment



State Reduction and Assignment

State Table

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

State Reduction and Assignment

Reducing the State Table

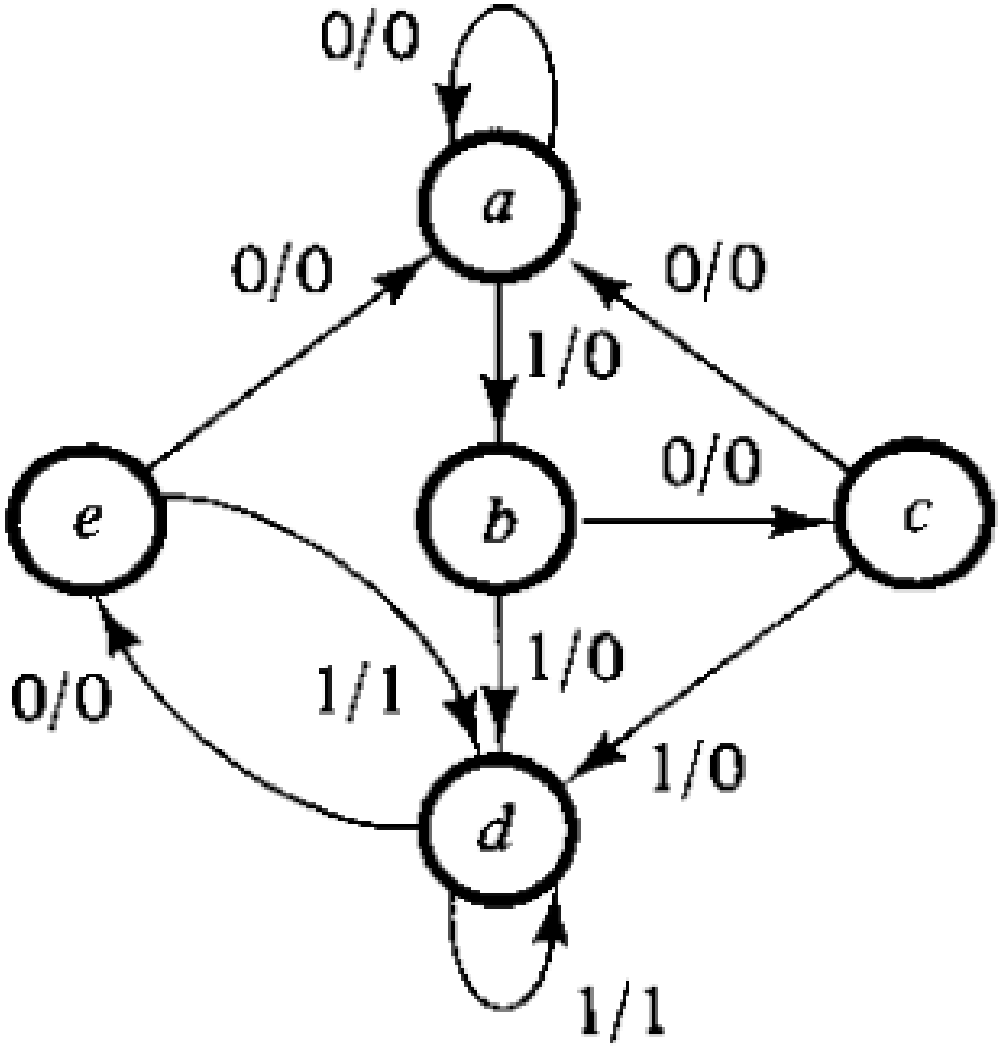
	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

State Reduction and Assignment

Reduced State Table

	Next state		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

State Reduction and Assignment



State Reduction and Assignment

Three Possible Binary State Assignments

State	Assignment 1	Assignment 2	Assignment 3
a	001	000	000
b	010	010	100
c	011	011	010
d	100	101	101
e	101	111	011

State Reduction and Assignment

Reduced State Table with Binary Assignment 1

	Next State		Output	
Present state	$x = 0$	$x = 1$	$x = 0$	$x = 1$
001	001	010	0	0
010	011	100	0	0
011	001	100	0	0
100	101	100	0	1
101	001	100	0	1

Flip Flop Excitation Tables

Flip-Flop Excitation Tables

$Q(t)$	$Q(t+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(a) RS

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) JK

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

(c) D

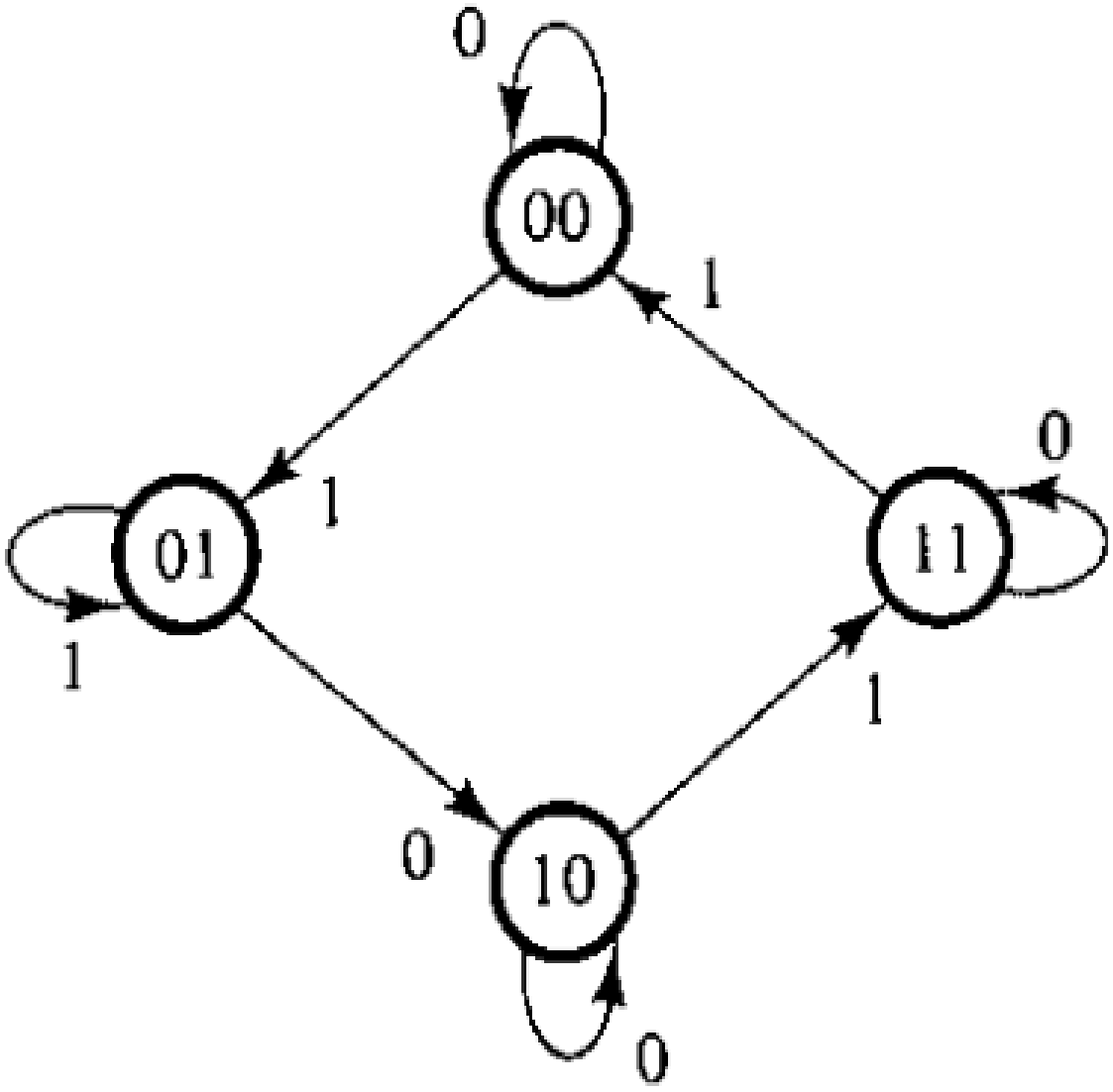
$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) T

Design Procedure

1. The word description of the circuit behavior is stated. This may be accompanied by a state diagram, a timing diagram, or other pertinent information.
2. From the given information about the circuit, obtain the state table.
3. The number of states may be reduced by state-reduction methods if the sequential circuit can be characterized by input–output relationships independent of the number of states.
4. Assign binary values to each state if the state table obtained in step 2 or 3 contains letter symbols.
5. Determine the number of flip-flops needed and assign a letter symbol to each.
6. Choose the type of flip-flop to be used.
7. From the state table, derive the circuit excitation and output tables.
8. Using the map or any other simplification method, derive the circuit output functions and the flip-flop input functions.
9. Draw the logic diagram.

Circuit Design Using JK Flip Flop



Circuit Design Using JK Flip Flop

State Table

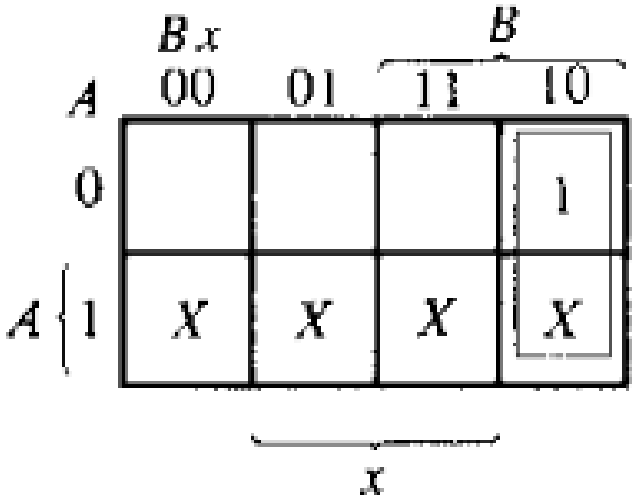
Present State		Next State			
		$x = 0$		$x = 1$	
A	B	A	B	A	B
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

Circuit Design Using JK Flip Flop

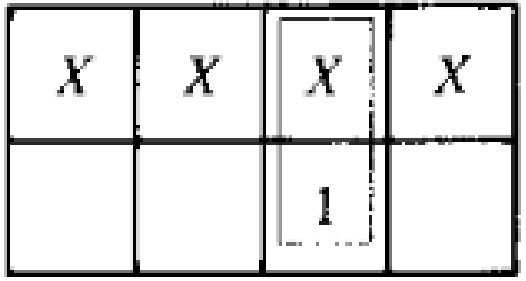
Excitation Table

Inputs of Combinational Circuit			Next State		Outputs of Combinational Circuit			
Present State		Input			Flip-Flop Inputs			
A	*B*	*x*	*A*	*B*	*JA*	*KA*	*JB*	*KB*
0	0	0	0	0	0	*X*	0	*X*
0	0	1	0	1	0	*X*	1	*X*
0	1	0	1	0	1	*X*	*X*	1
0	1	1	0	1	0	*X*	*X*	0
1	0	0	1	0	*X*	0	0	*X*
1	0	1	1	1	*X*	0	1	*X*
1	1	0	1	1	*X*	0	*X*	0
1	1	1	0	0	*X*	1	*X*	1

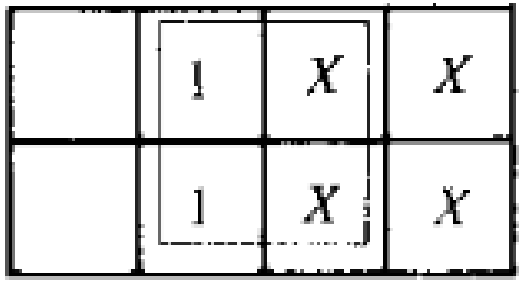
Circuit Design Using JK Flip Flop



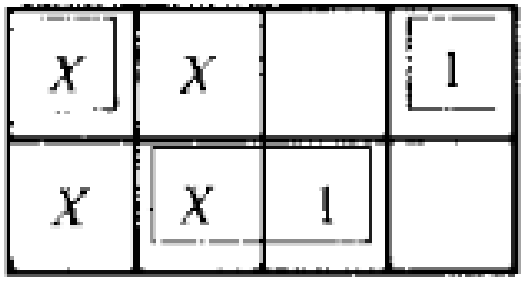
$JA = Bx'$



$KA = Bx$

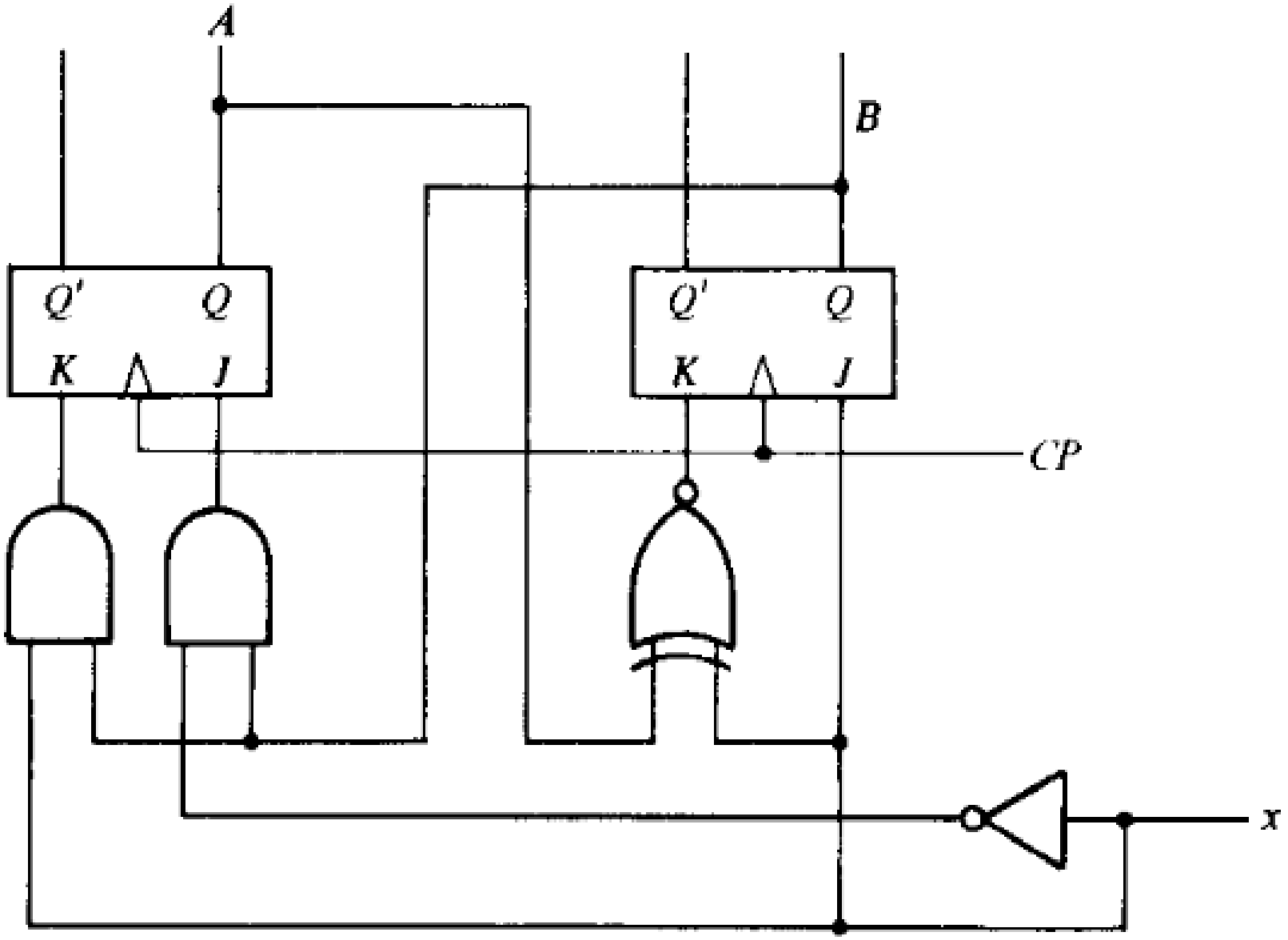


$JB = x$



$KB = (A \oplus x)'$

Circuit Design Using JK Flip Flop



Circuit Design Using D Flip Flop

$$DA(A, B, x) = \Sigma\,(2, 4, 5, 6)$$

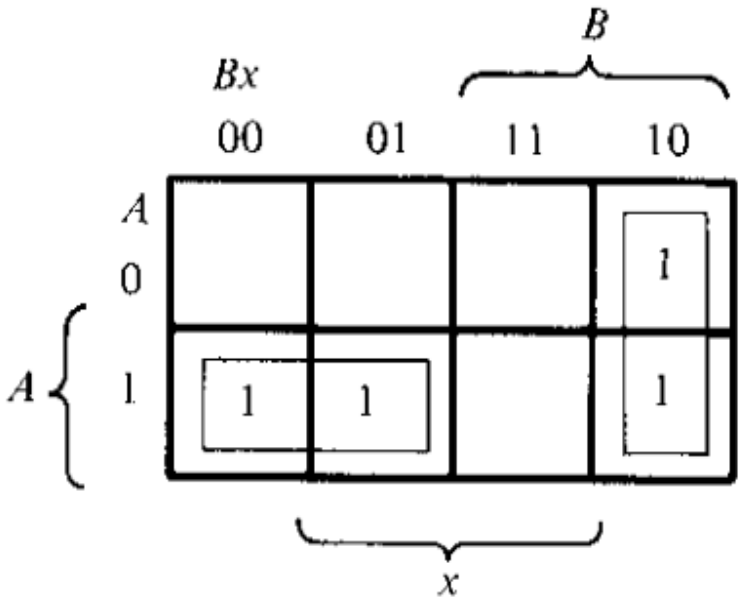
$$DB(A, B, x) = \Sigma\,(1, 3, 5, 6)$$

$$y(A, B, x) = \Sigma\,(1, 5)$$

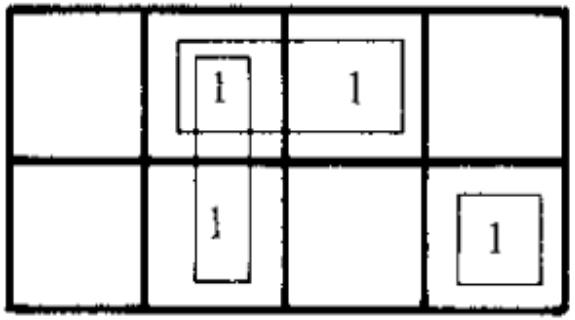
State Table for Design with *D* Flip-Flops

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

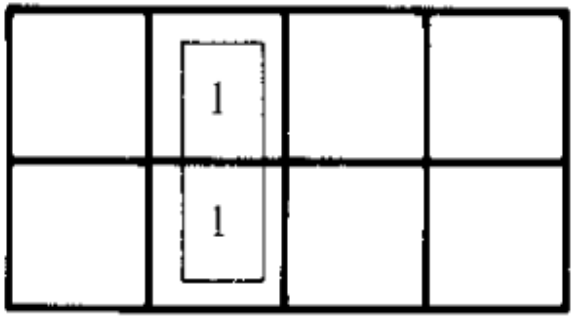
Circuit Design Using D Flip Flop



$DA = AB' + Bx'$

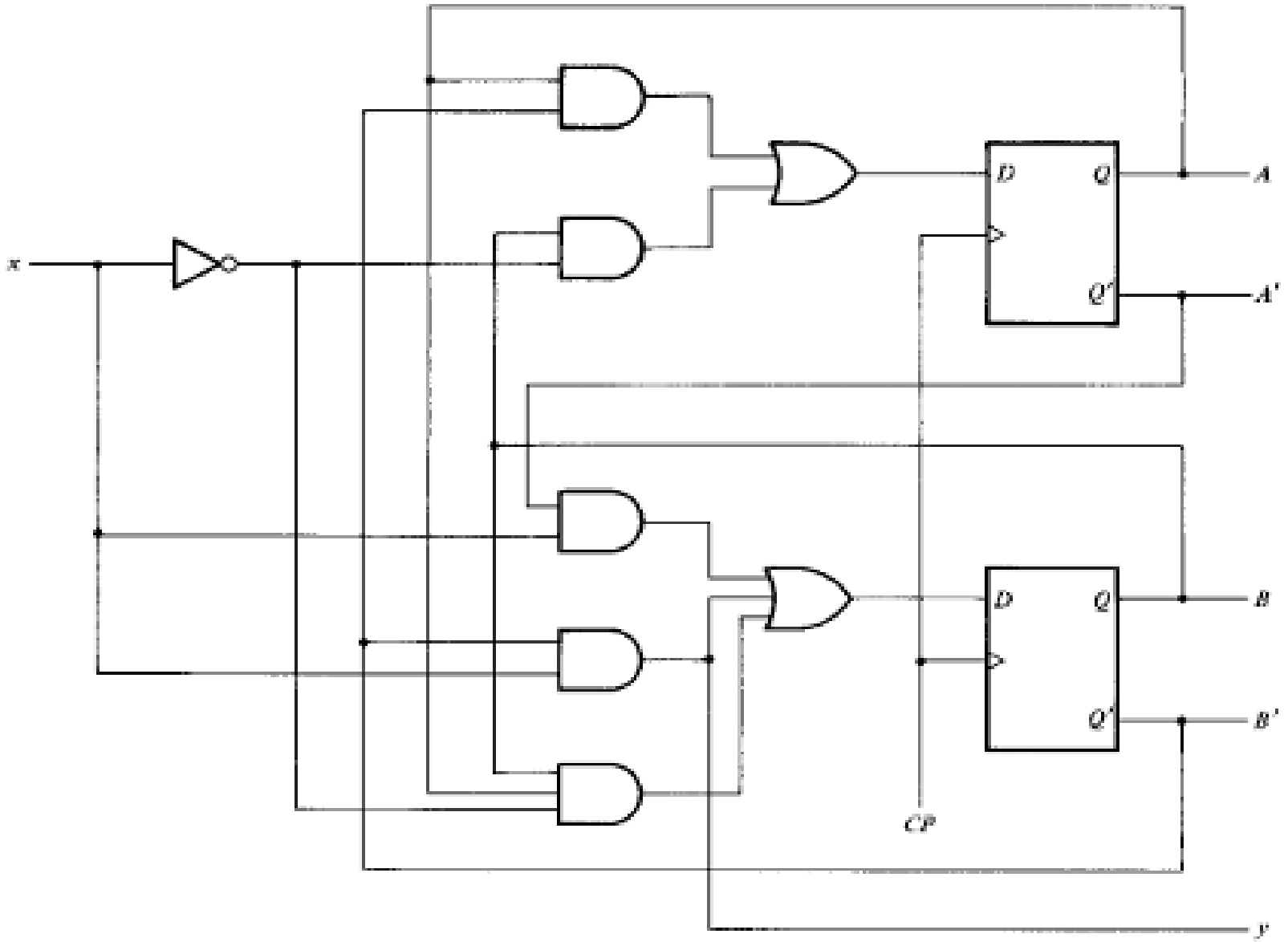


$DB = A'x + B'x + ABx'$



$y = B'x$

Circuit Design Using D Flip Flop

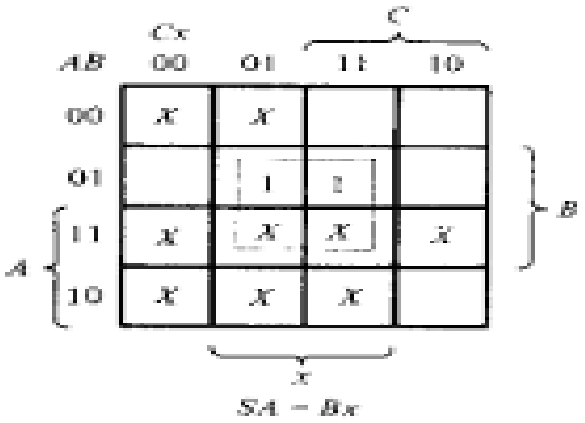


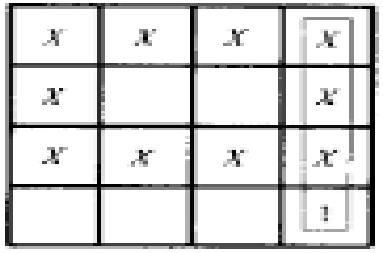
Design With Unused States Using SR Flip Flop

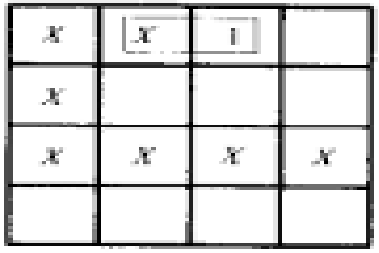
State Table with Unused States

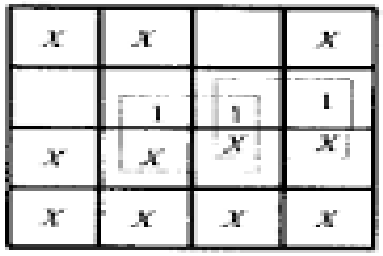
Present State			Input	Next State			Flip-Flop Inputs						Output
A	*B*	*C*	*x*	*A*	*B*	*C*	*SA*	*RA*	*SB*	*RB*	*SC*	*RC*	*y*
0	0	1	0	0	0	1	0	X	0	X	X	0	0
0	0	1	1	0	1	0	0	X	1	0	0	1	0
0	1	0	0	0	1	1	0	X	X	0	1	0	0
0	1	0	1	1	0	0	1	0	0	1	0	X	0
0	1	1	0	0	0	1	0	X	0	1	X	0	0
0	1	1	1	1	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	1	X	0	0	X	1	0	0
1	0	0	1	1	0	0	X	0	0	X	0	X	1
1	0	1	0	0	0	1	0	1	0	X	X	0	0
1	0	1	1	1	0	0	X	0	0	X	0	1	1

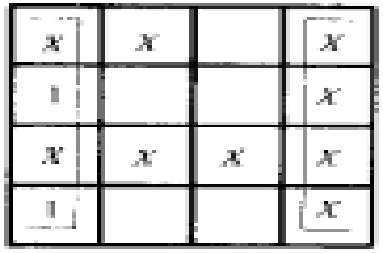
Design With Unused States Using SR Flip Flop

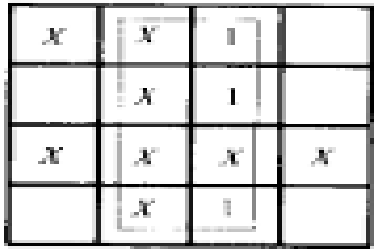


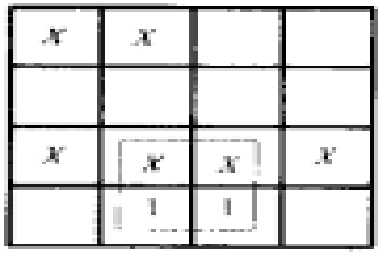




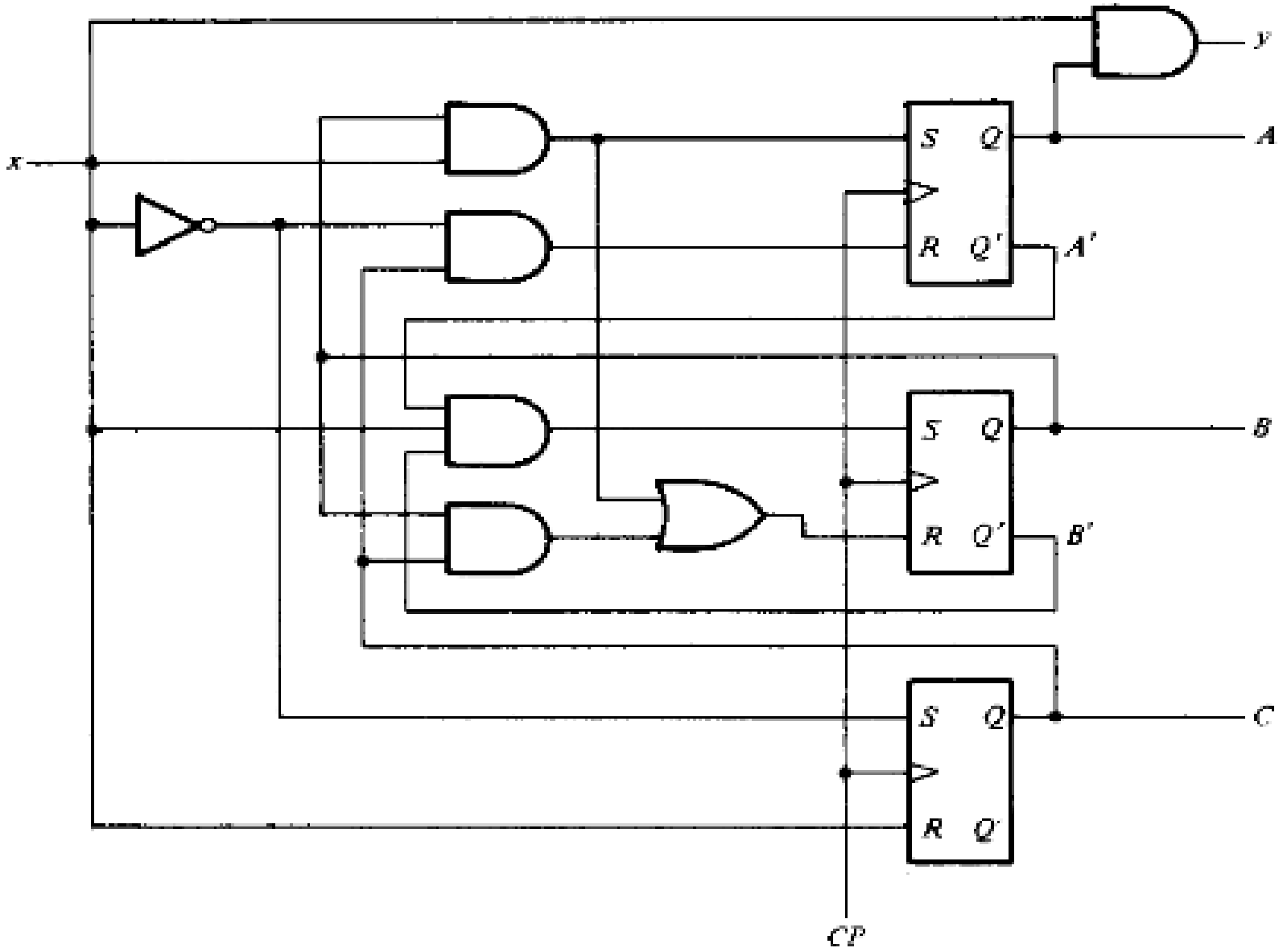




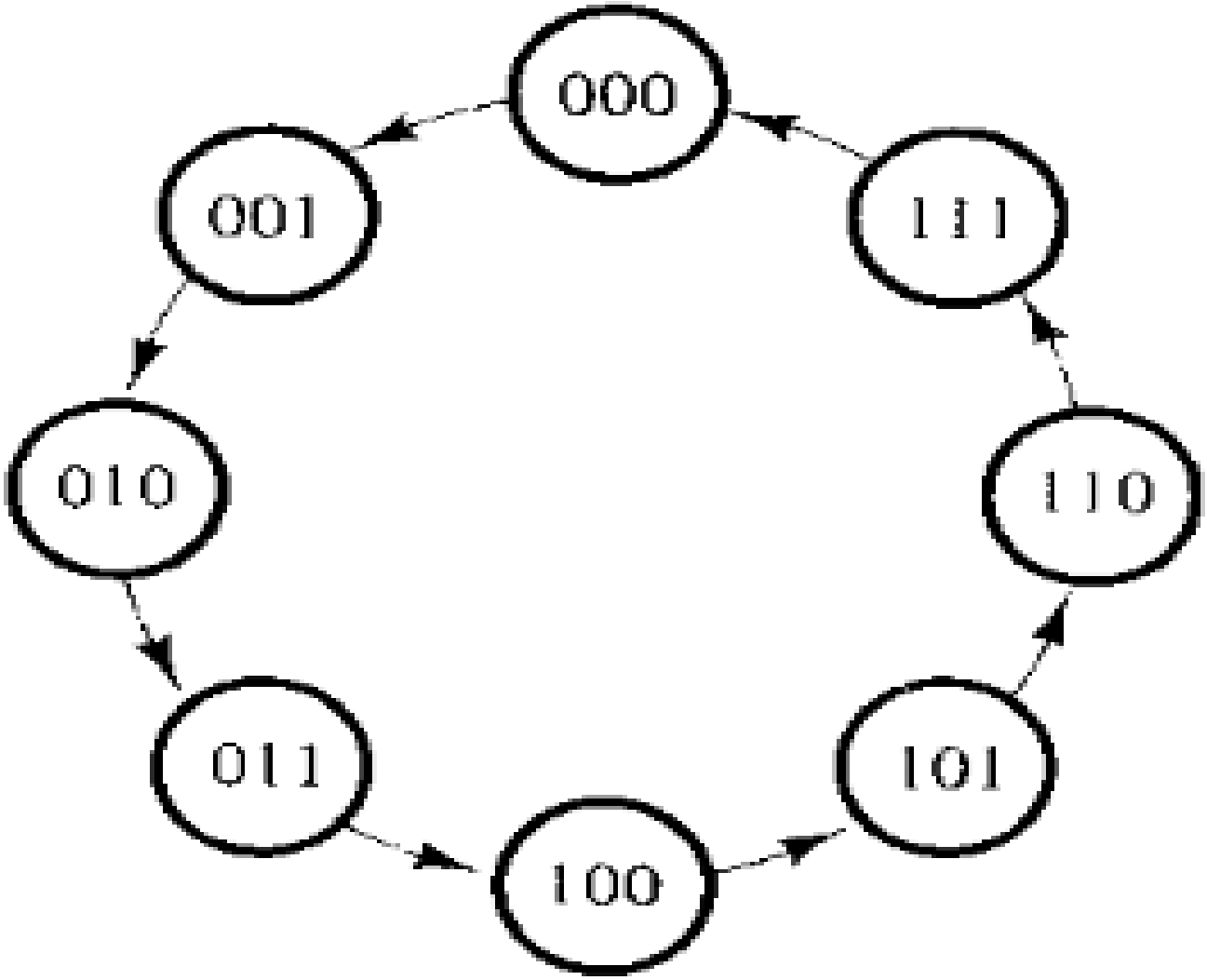




Design With Unused States Using SR Flip Flop



Design of Counter

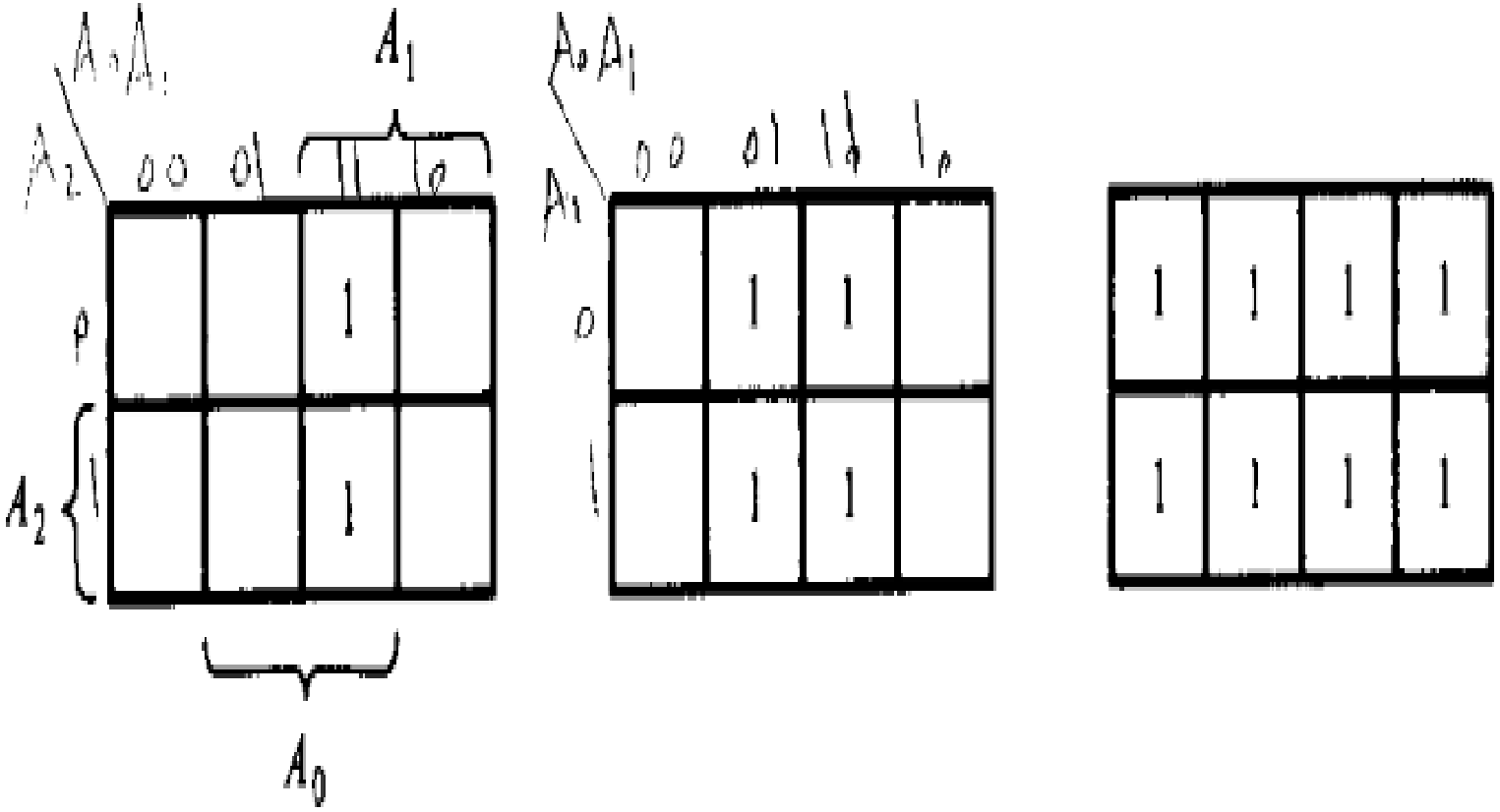


Design of Counter

Excitation Table for 3-Bit Counter

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Design of Counter

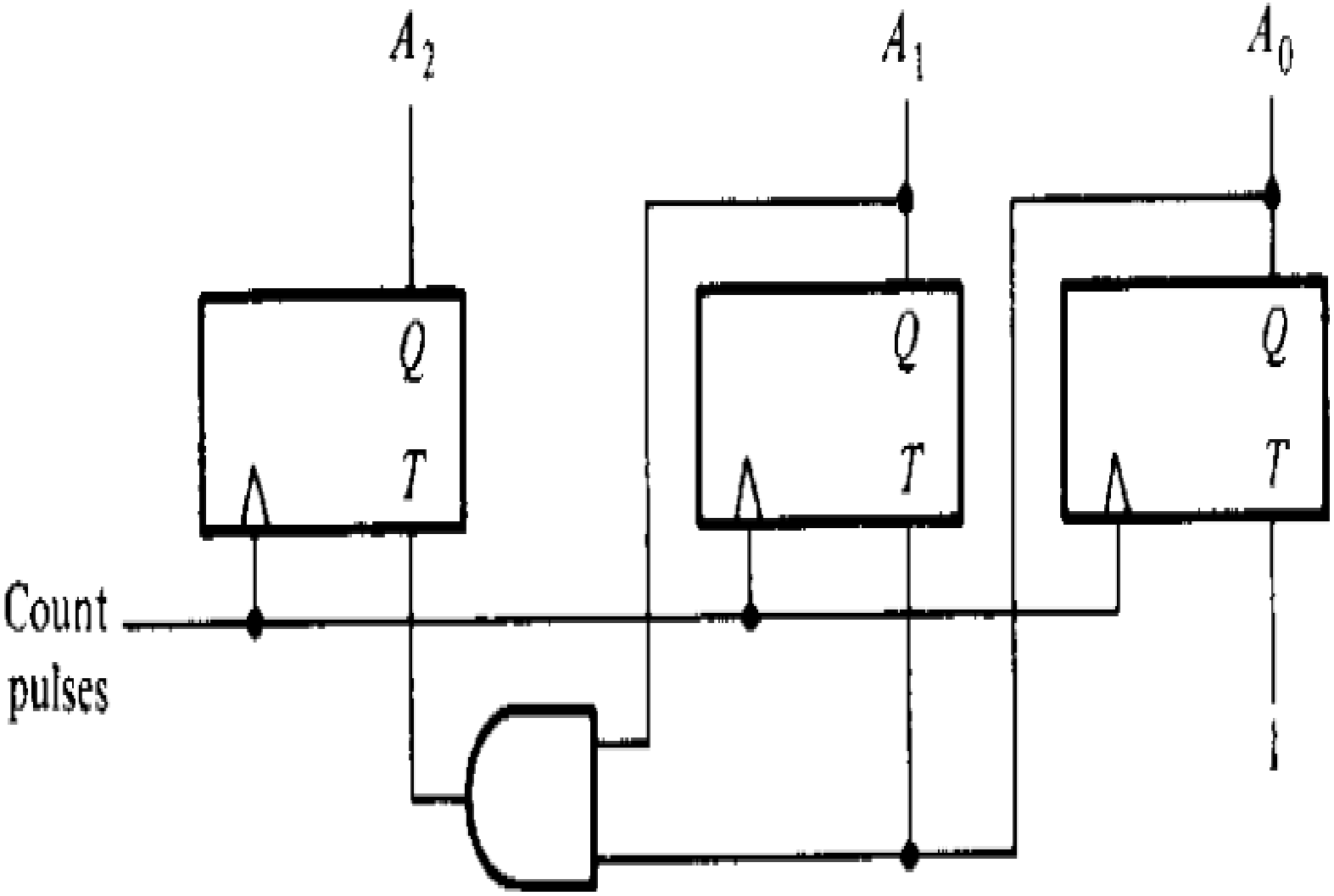


$TA_2 = A_1A_0$

$TA_1 = A_0$

$TA_0 = 1$

Design of Counter



Counter for Non-Binary Sequence

Excitation Table for Counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Counter for Non-Binary Sequence