CO2-Pipelined-Mips-2017

Documentation

G47

SEC: 3

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  - Forward Unit.
  - Hazard Detection Unit.
  - Data Memory.
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  - ALUSrcMux.
  - forwardingUnitSuperMux.
  - CPU.

- Each Module Design

Fetch Stage

-Fetch module:

Consists of:

- PC: to fetch the instruction, in normal conditions PC incremented by 4 each clock cycle.

In a branch equal instruction, after the pc is incremented by 4, the module checks one of the inputs name SEL which comes from the execution stage which indicates whether the branch is taken or not taken and thus add the offset value to the pc incremented value to fetch the instruction stored there.

Stall procedures to stall the pipelined processor after a beq instruction, or a lw instruction (if hazard detected)

This is done by stopping the increment by 4 of the PC and setting the instruction value in the IFID register to zero to apply a shift left logical R operation which is translated into a no operation instruction as it does not make any changes in any of the registers or the data or instruction memories.

This no operation is detected through an if condition (mux) and thus we thought we don't need a whole hazard detection unit as its job is simple and can be implemented by mux modules and if conditions.

-Instruction Memory: It consists of 32 instruction (32 word- 128 bytes) divided into bytes (not words) each word/instruction consists of 4 bytes.

The output is put into the IFIDIR Register for the following Decode Stage to start another clock cycle.

DECODE STAGE

-Control Unit module:

Takes the OP code from the instruction word (first 6 bits) as an input and evaluates the output which is the control signals to different muxes and ALUop control signals (which goes to the ALU Control Unit input).

The control signals are 8 control signals (including ALUop): RegDest-> Register Destination to determine whether the register file should write in the register address that comes from rt or rd(lw or R type instructions).

Branch-> Flag to tell if this instruction is a beq or not. MemRead-> Memory read this is an input the DataMemory to enable or disable reading from it

MemtoReg-> Memory To Register To determine whether the value to be written to the register

comes from ALU result or the data read from data memory

ALUOP-> a 2 bit control signal goes to the ALU control unit to determine the operations to be held there (add, sub, sll, etc..)

MemWrite->An input to the data memory module, to determine whether this instruction can write in the memory or not

ALUSrc-> determines whether the ALU second operand (input) should come from the register file read values or the Sign Extended number that comes from the immediate field in i-type instructions

RegWrite-> Input to the register file module to determine whether this instruction can write in a register inside the register file or not.

The main control unit supports:

add, sub, sll, beq, lw, sw, and, or.

-Register file: consists of 32 registers each one of 32 bits.

you can read values from the registers (two values at a time)at any time but you can write (one value at a time)only at positive clock edge and if the write enable input signal is set to 1.

This is done by taking the registers' addresses, write enable, clock as inputs, and outputting the read values.

EXECUTION STAGE

-ALU Control Unit:

It takes a 2bit input from the main Control unit alongside with the 6 bit function field from the instruction word. And outputs 3 bits signal to the ALU to determine which combinational operation should be held now.

The ALU control unit supports:

add, sub, sll, beq, lw, sw, and, or.

-ALU:

Takes two 32 bit values as inputs and applies the operation determined in the ALU control unit, the output is a 32 bit result value.

This ALU unit supports:

add, sub,lw, sw, and .

sll-> shift left logical by taking the shift amount value as an input to the alu.

beq-> by supporting a Zero Flag output. In detail: it subtracts the input values, if the result is zero the

Zero Flag is set to 1, otherwise it is set to 0.

-Sign Extender:

It takes 16 bit number as input and arthmitically outputs a 32 bit extended number (concatinates the 16'th bit 16 times to the left of the input number)

-Forward Unit:

This unit is set up for Data Hazard cases, it forwards ready values to demanding places: -from memory to ALU two inputs-from ALU result to ALU two inputs.

-Hazard Detection Unit:

It detects the lw instruction

MEMORY STAGE and WRITE BACK STAGE

-Data Memory:

Consists of 128 bytes. It takes control signal inputs which are MemWrite and MemRead to determind whether this instruction can use the data memory to read or write values.
Including a 32 bit input as the address that the data should be read from or written to.
The only output is a 32 bit read value which is sent to a Mux alongside with the ALU result value and then it is determined in the Write Back Stage which one should be written to the register file.

MUXES

- writeRegMux:

it takes RegDst (register destination) as an input which determines whether the register file should write in the register address that comes from rt for lw instruction or rd for R type instructions according to the OP code.

- ALUSrcMux:

it takes ALUSrc as an input which determines whether the ALU second operand (input) should come from the register file read values or the Sign Extended number that comes from the immediate field in i-type instructions

- forwardingUnitSuperMux:

This mux controls the input values for the two input wires to the ALU whether it should be the value forwarded from the memory stage or the value forwarded from the alu result or the value read from the register file of the address rt or the address rs according to the dependancy.

- Main board module′ s design:

- CPU:

Contains all the modules previously mentioned, all the pipelined registers and connects all the stages together, through wires.

We have 4 pipelined registers:

IFID register connects between fetch and decode stages.

IDEX register connects between decode and execution stages.

EXMEM register connects between execution and memory stages.

MEMWB register connects between memory and write back stages.

Each register contains sub registers, for example rt values are saved in registers called rt_IFIDIR → rt value in the pipelined register between the fetch and decode stages.

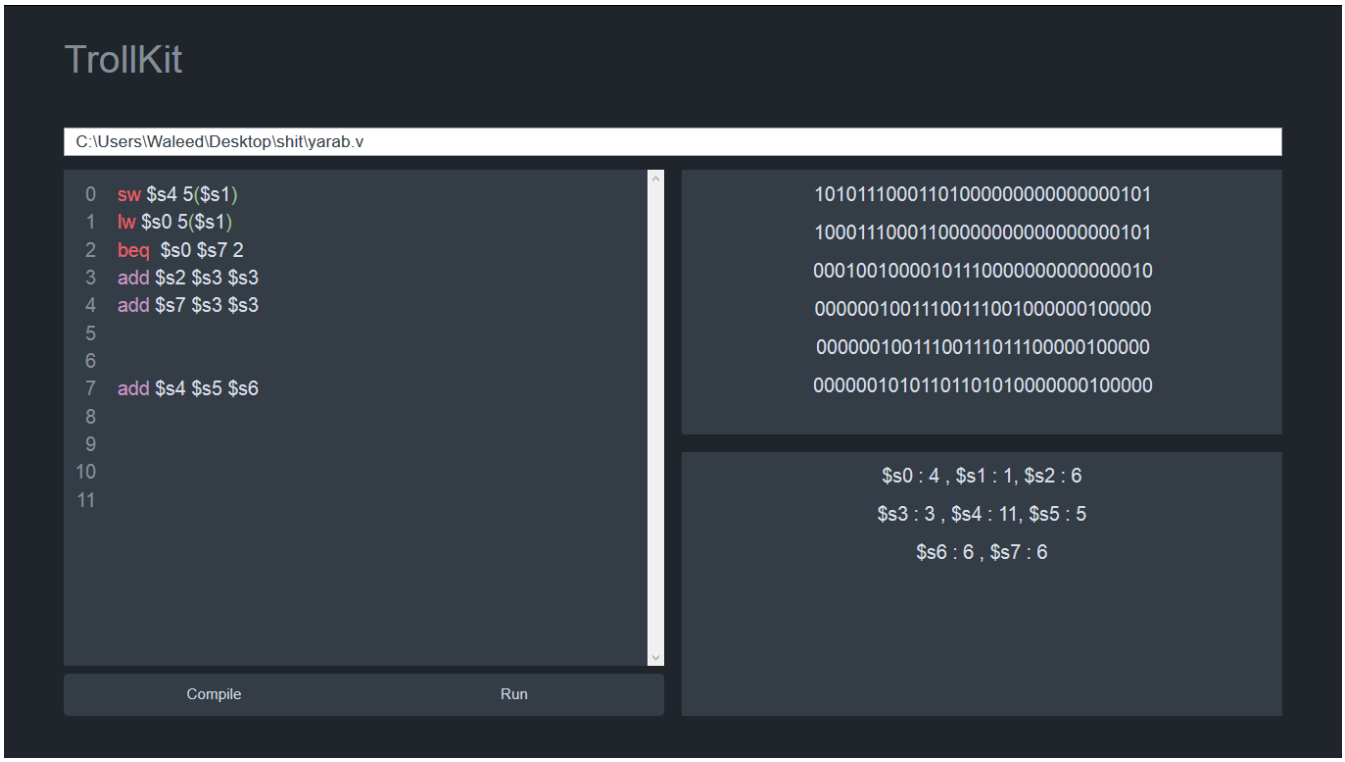
MemRead_IEMEMIR → Memory Read control signal value in the pipelined register between execution and memory.

- CPU initializations:
  - In the Register File we initialized registers starting from $s0=0, $s1=1, …,$s7=7.
  - In the Data Memory

Test Cases

1) With control and data hazards:

To make sure the sw stores in the memory and the lw reads from the same place, the beq depends on the lw result,(not true beq) we needed to make sure it works with a complicated test case.



TrollKit

C:\Users\Waleed\Desktop\shit\yarab.v

```
0  add $s0 $s1 $s2
1  and $s1 $s0 $s3
2  or $s4 $s1 $s5
3
```

Compile Run

```
00000010001100101000000000100000
00000010000100111000100000100100
00000010001101011010000000100101
```

```
$s0 : 3 , $s1 : 3, $s2 : 2
$s3 : 3 , $s4 : 7, $s5 : 5
$s6 : 6 , $s7 : 7
```

TrollKit

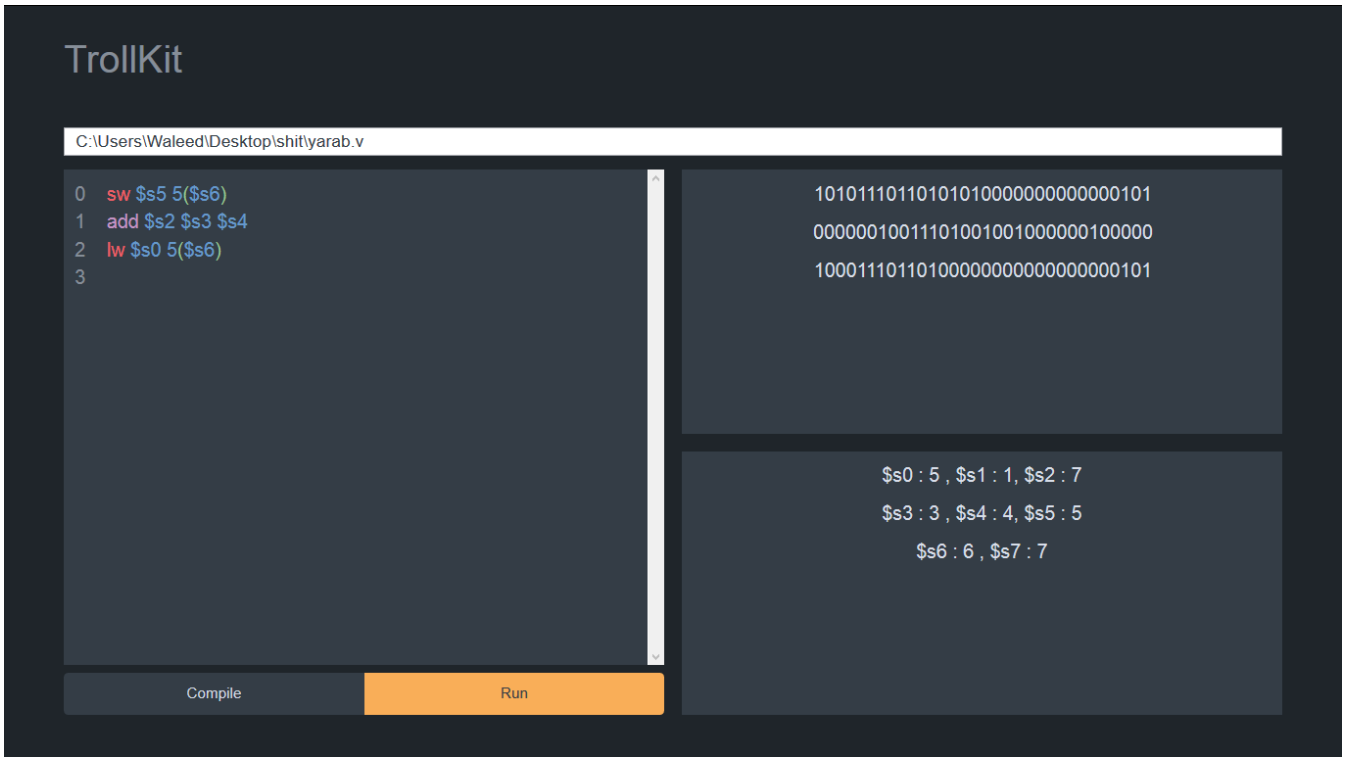
C:\Users\Waleed\Desktop\shit\yarab.v

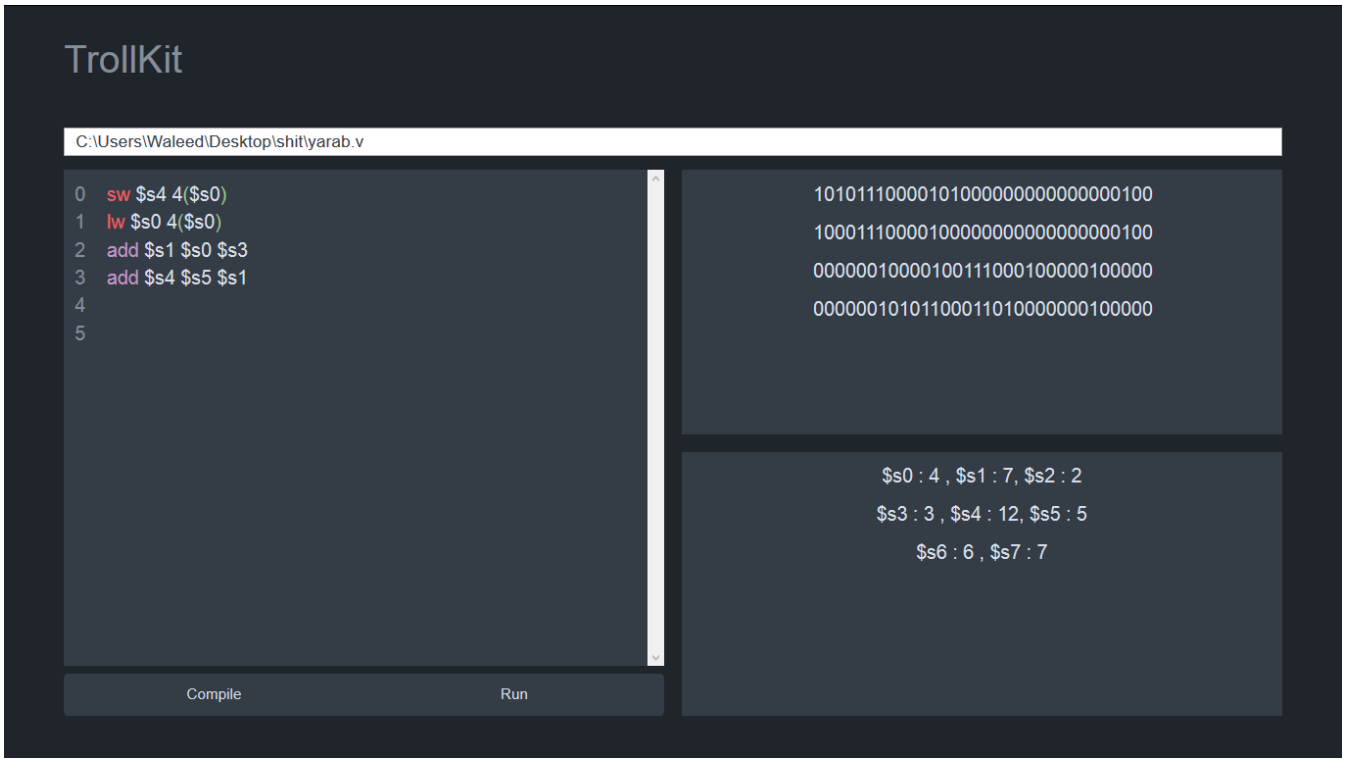
```
0  add $s0 $s1 $s2
1  sub $s3 $s4 $s5
2  sll $s6 $s7 2
3
```

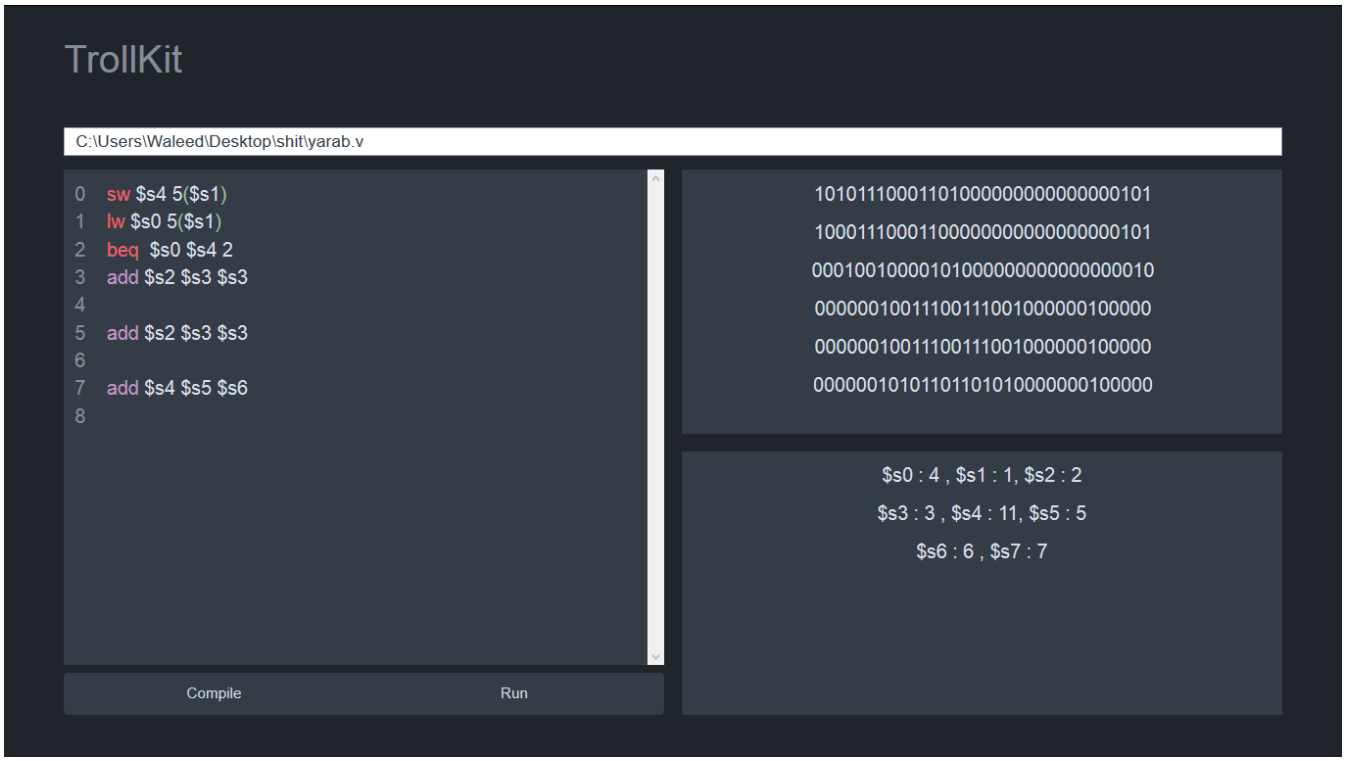
Compile Run

```
00000010001100101000000000100000
00000010100101011001100000100010
00000000000010111101100001000000
```

```
$s0 : 3 , $s1 : 1, $s2 : 2
$s3 : -1 , $s4 : 4, $s5 : 5
$s6 : 28 , $s7 : 7
```


TrollKit
C:\Users\Waleed\Desktop\shit\yarab.v
0 sw $s5 5($s6)
1 add $s2 $s3 $s4
2 lw $s0 5($s6)
3
Compile
Run
10101110110101010000000000000101
00000010011101001001000000100000
10001110110100000000000000000101
$s0 : 5 , $s1 : 1, $s2 : 7
$s3 : 3 , $s4 : 4, $s5 : 5
$s6 : 6 , $s7 : 7


TrollKit
C:\Users\Waleed\Desktop\shit\yarab.v
0 sw $s4 4($s0)
1 lw $s0 4($s0)
2 add $s1 $s0 $s3
3 add $s4 $s5 $s1
4
5
Compile
Run
10101110000101000000000000000100
10001110000100000000000000000100
00000010000100111000100000100000
00000010101100011010000000100000
$s0 : 4 , $s1 : 7, $s2 : 2
$s3 : 3 , $s4 : 12, $s5 : 5
$s6 : 6 , $s7 : 7



2) Second screenshot is data hazard test case for normal forwarding operations also to test or, and instructions.

3) Third screenshot is for normal without hazards instructions to test sll, sub (signed), add instructions.

4) Without hazards to test sw, lw and add.

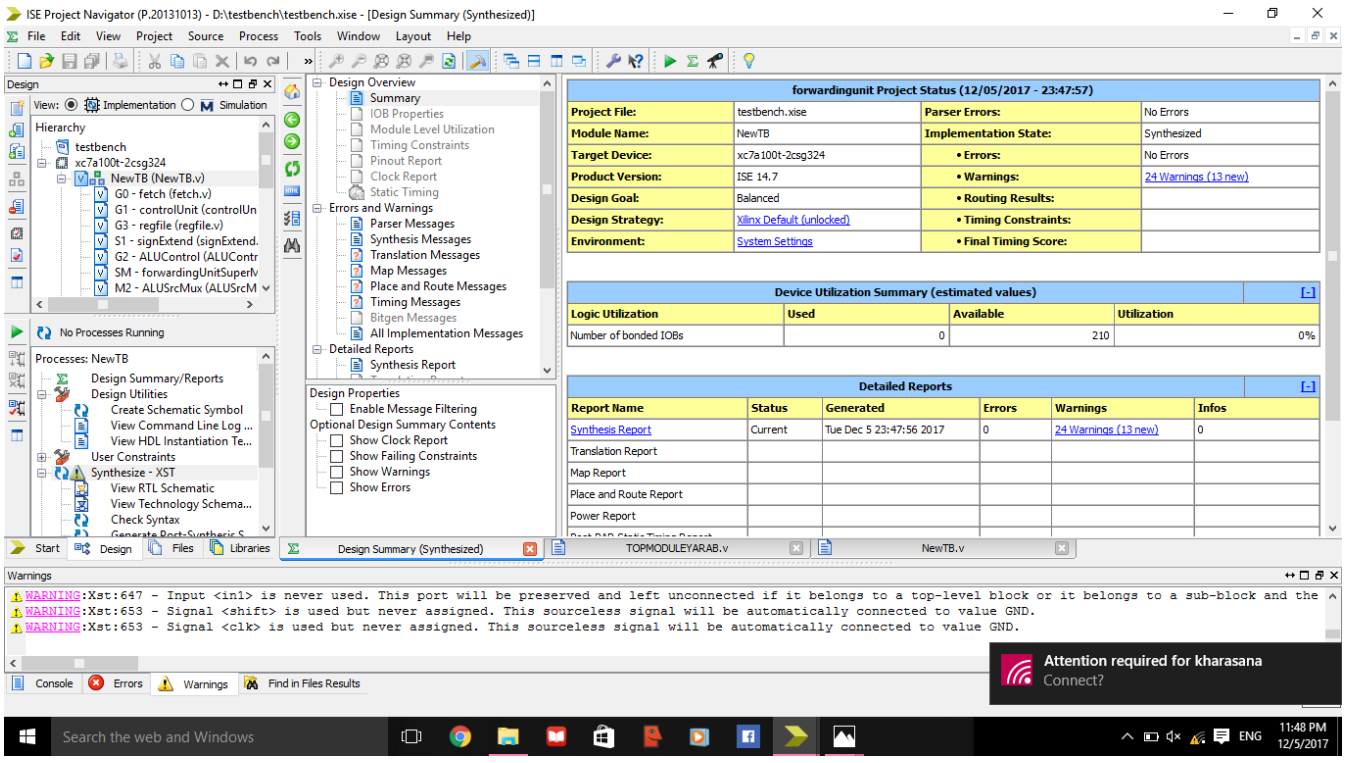
5) To test add instruction depending on lw instruction.

6) To test a complicated instruction with a true beq. (same as number 1 but true beq).

Input to the processor

We implemented a GUI (Check the details in the GUI documentation), the GUI allows you to write your assembly code (instructions) in, assemble them into machine (binary) code, then run it through ModelSim. You can always check what is inside the register through the GUI.

Synthesizability

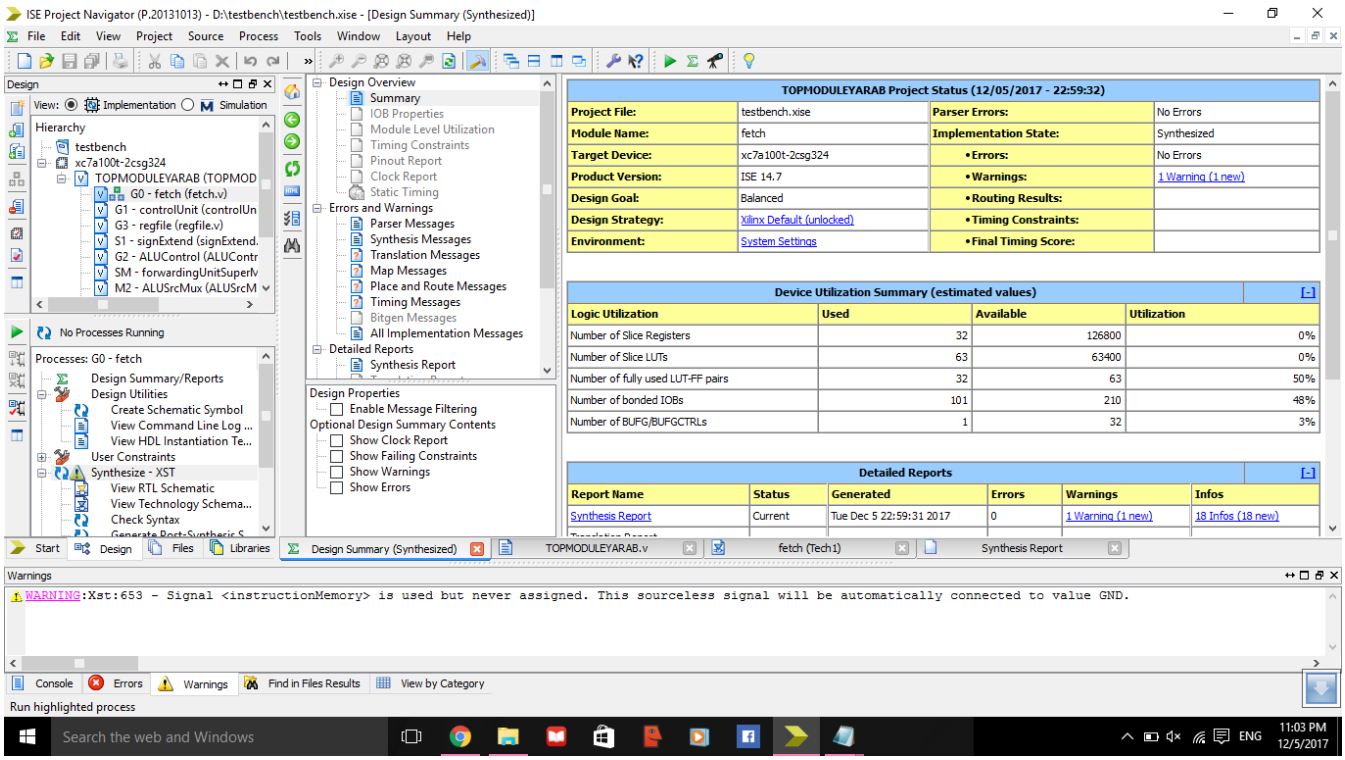


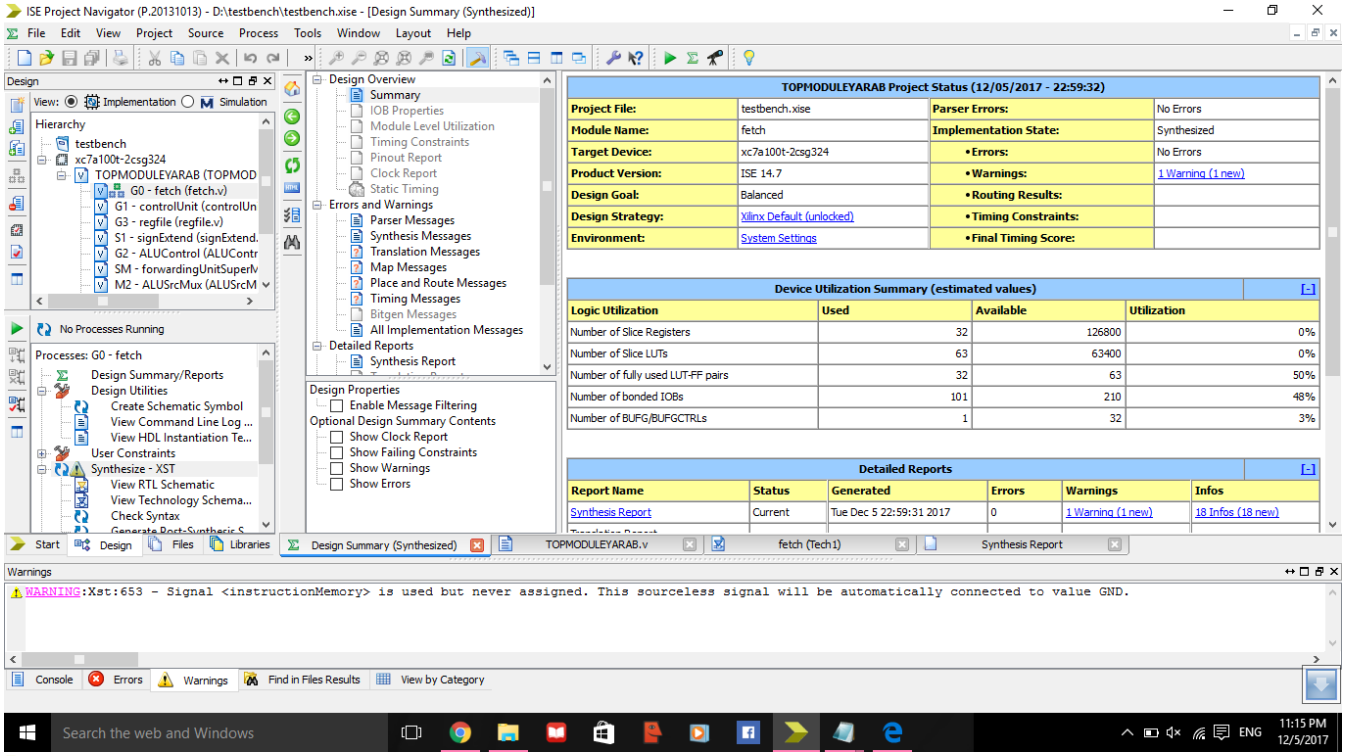
All modules are synthesized separately, the synthesized report is attached in the zipped file with screenshots.

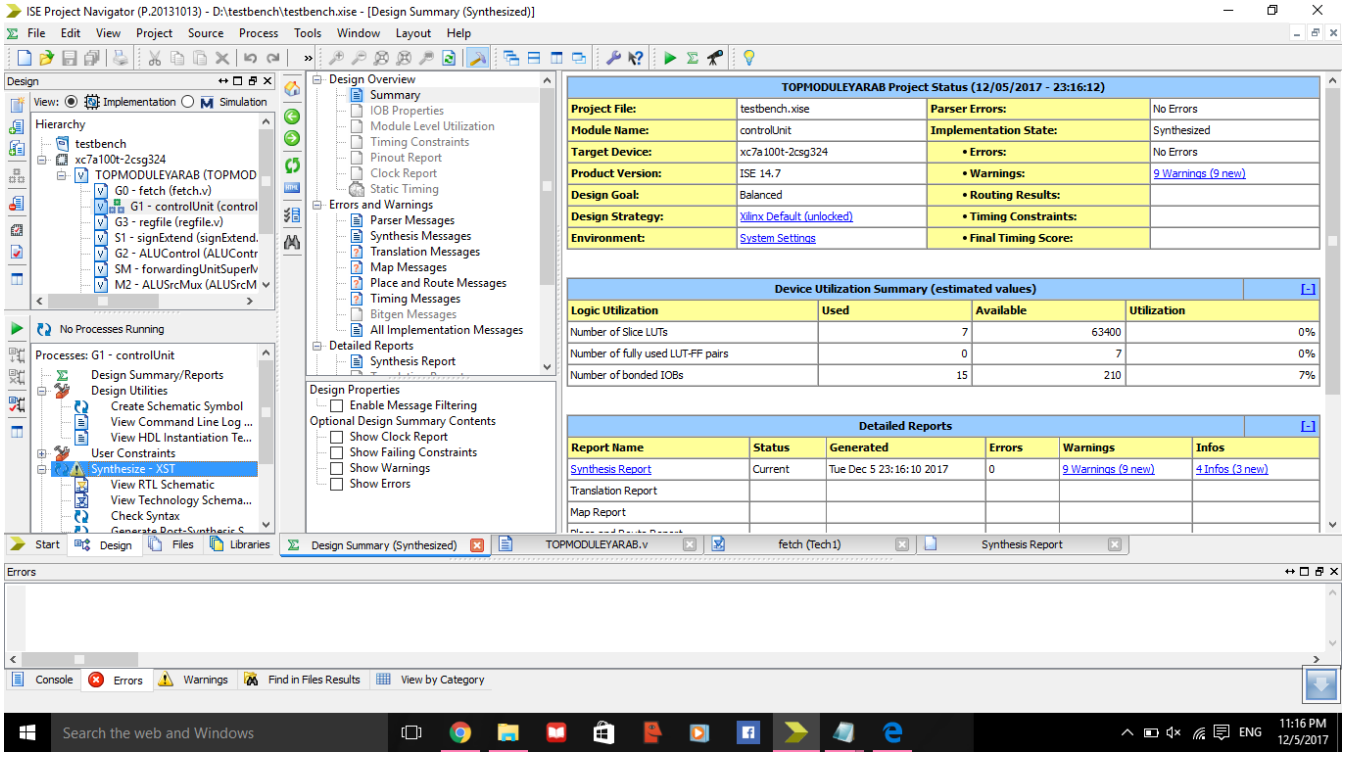
1) Fetch module.

2) Control unit.

3) Register File.
4) Signe Extend.
5) ALU Control.
6) Forwarding Unit Super Mux.
7) ALUSrc Mux.
8) ALU.
9) WriteRegMux.
10) Data Memory.
11) Forward Unit.




ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
testbench
xc7a100t-2csg324
TOPMODULEYARAB (TOPMOD
G0 - fetch (fetch.v)
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperIv
M2 - ALUSrcMux (ALUSrcM
No Processes Running
Processes: G0 - fetch
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 22:59:32)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: fetch
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: 1 Warning (1 new)
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice Registers | 32 | 126800 | 0%
Number of Slice LUTs | 63 | 63400 | 0%
Number of fully used LUT-FF pairs | 32 | 63 | 50%
Number of bonded IOBs | 101 | 210 | 48%
Number of BUFG/BUFGCTRLs | 1 | 32 | 3%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 22:59:31 2017 | 0 | 1 Warning (1 new) | 18 Infos (18 new)
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Warnings
WARNING:Xst:653 - Signal <instructionMemory> is used but never assigned. This sourceless signal will be automatically connected to value GND.
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:15 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
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xc7a100t-2csg324
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G1 - controlUnit (control
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperIv
M2 - ALUSrcMux (ALUSrcM
No Processes Running
Processes: G1 - controlUnit
Design Summary/Reports
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All Implementation Messages
Detailed Reports
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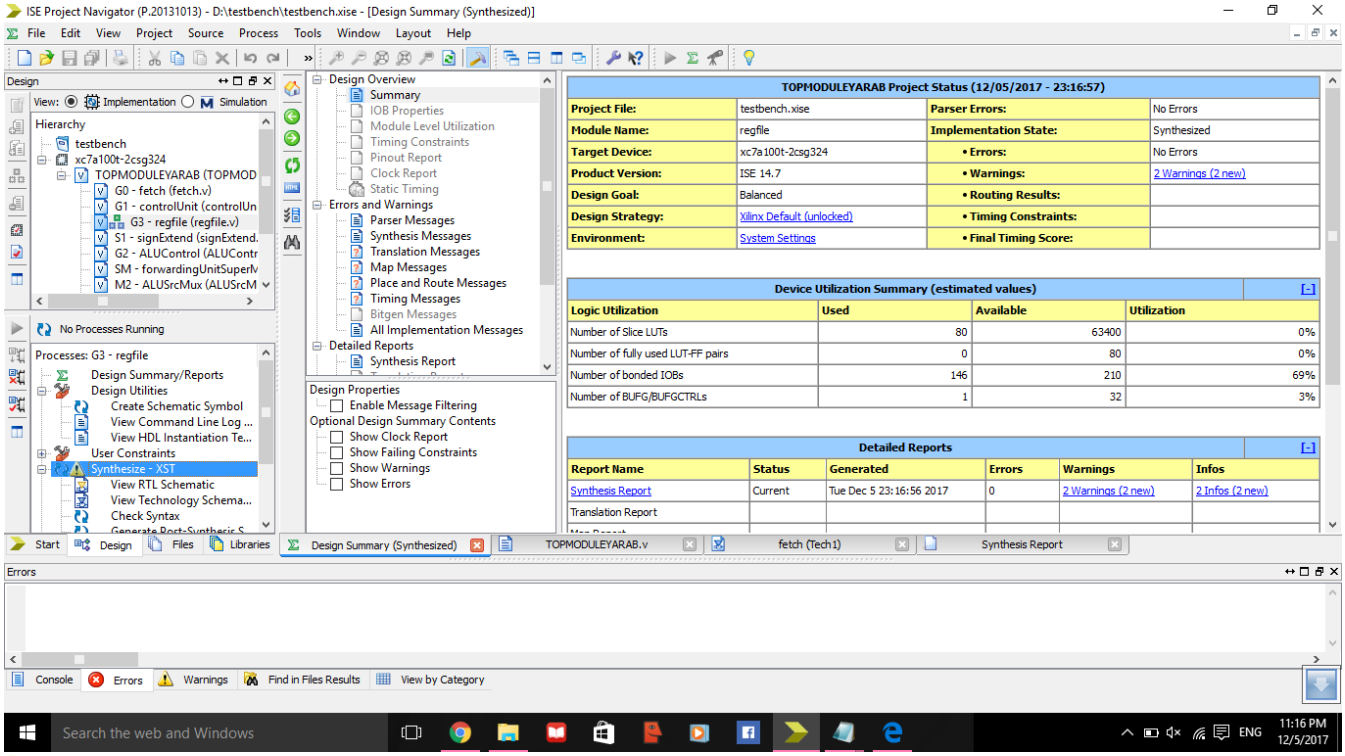
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:16:12)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: controlUnit
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: 9 Warnings (9 new)
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice LUTs | 7 | 63400 | 0%
Number of fully used LUT-FF pairs | 0 | 7 | 0%
Number of bonded IOBs | 15 | 210 | 7%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:16:10 2017 | 0 | 9 Warnings (9 new) | 4 Infos (3 new)
Translation Report
Map Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:16 PM
12/5/2017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No Processes Running
Processes: G3 - regfile
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
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User Constraints
Synthesize - XST
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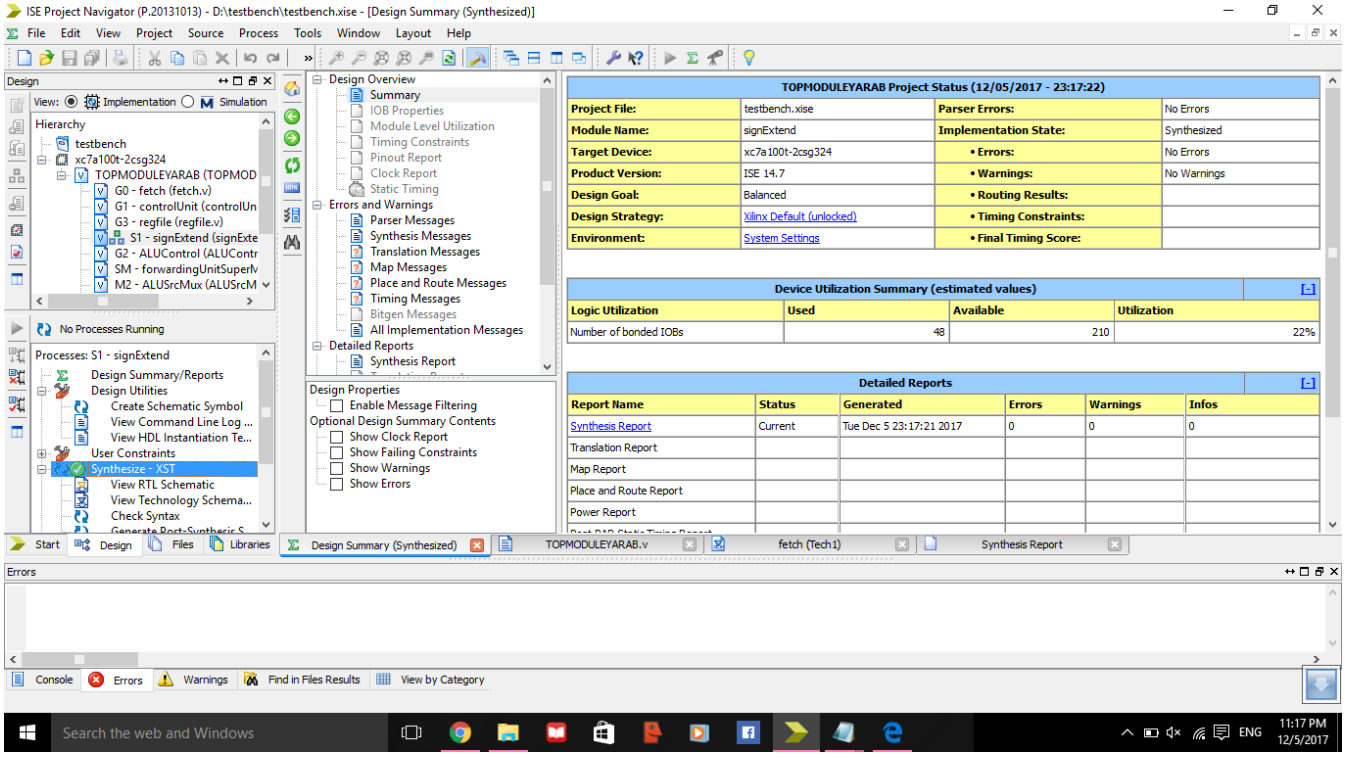
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:16:57)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: regfile
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: 2 Warnings (2 new)
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice LUTs | 80 | 63400 | 0%
Number of fully used LUT-FF pairs | 0 | 80 | 0%
Number of bonded IOBs | 146 | 210 | 69%
Number of BUFG/BUFGCTRLs | 1 | 32 | 3%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:16:56 2017 | 0 | 2 Warnings (2 new) | 2 Infos (2 new)
Translation Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:16 PM
12/5/2017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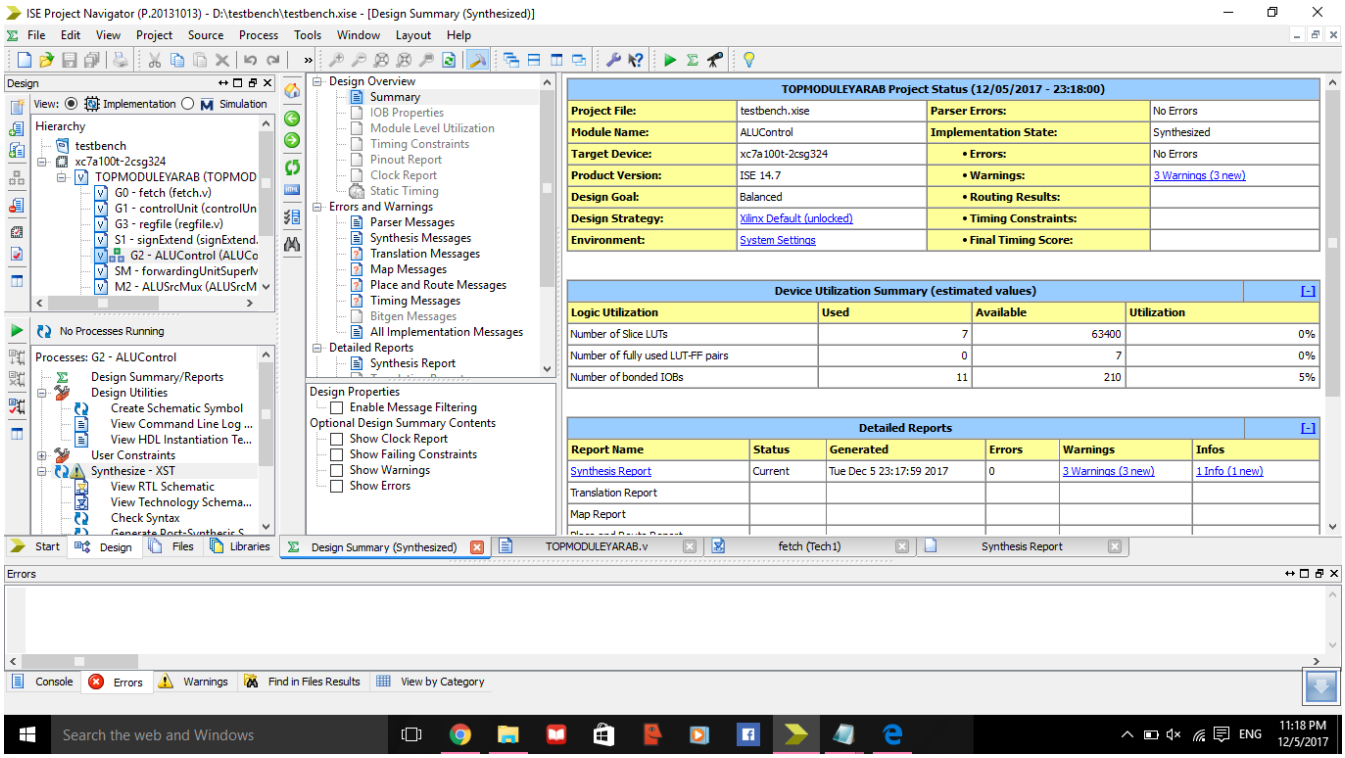
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:17:22)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: signExtend
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: No Warnings
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of bonded IOBs | 48 | 210 | 22%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:17:21 2017 | 0 | 0 | 0
Translation Report
Map Report
Place and Route Report
Power Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:17 PM
12/5/2017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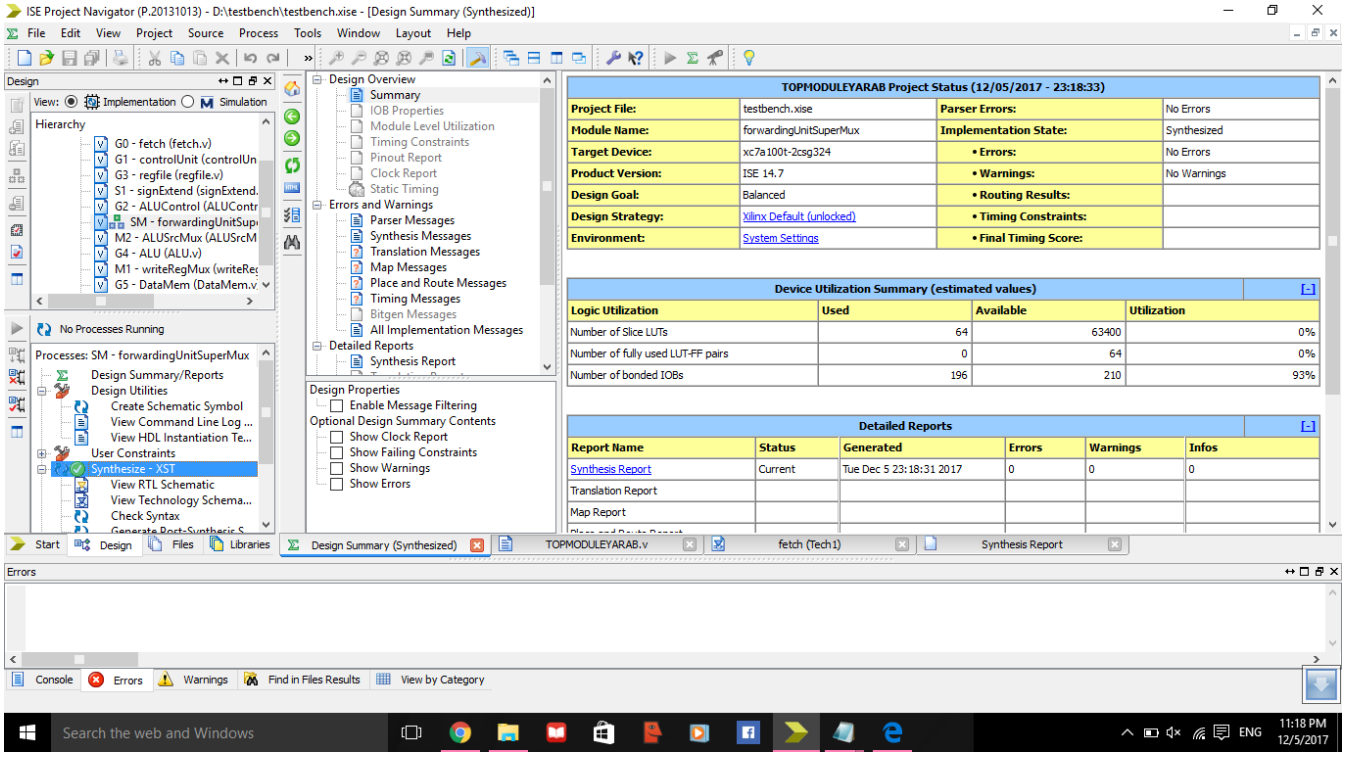
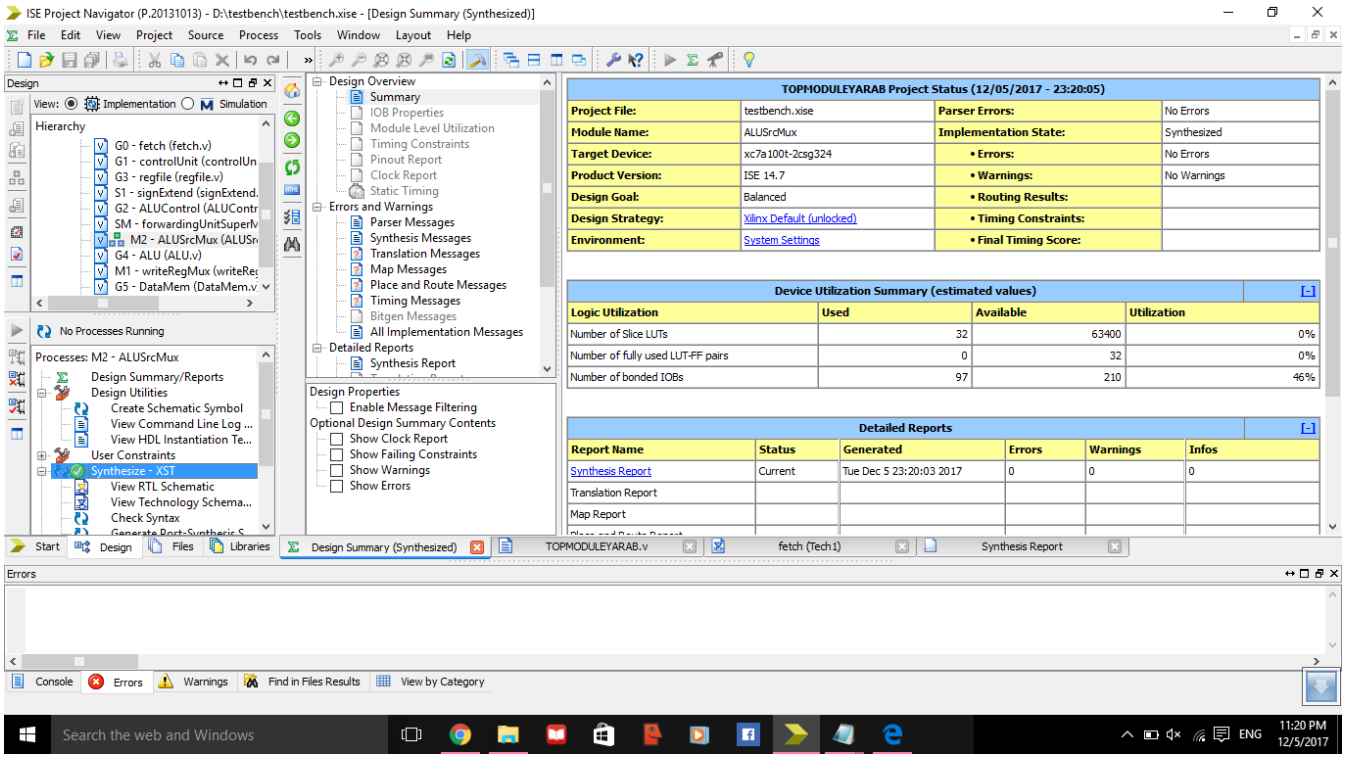
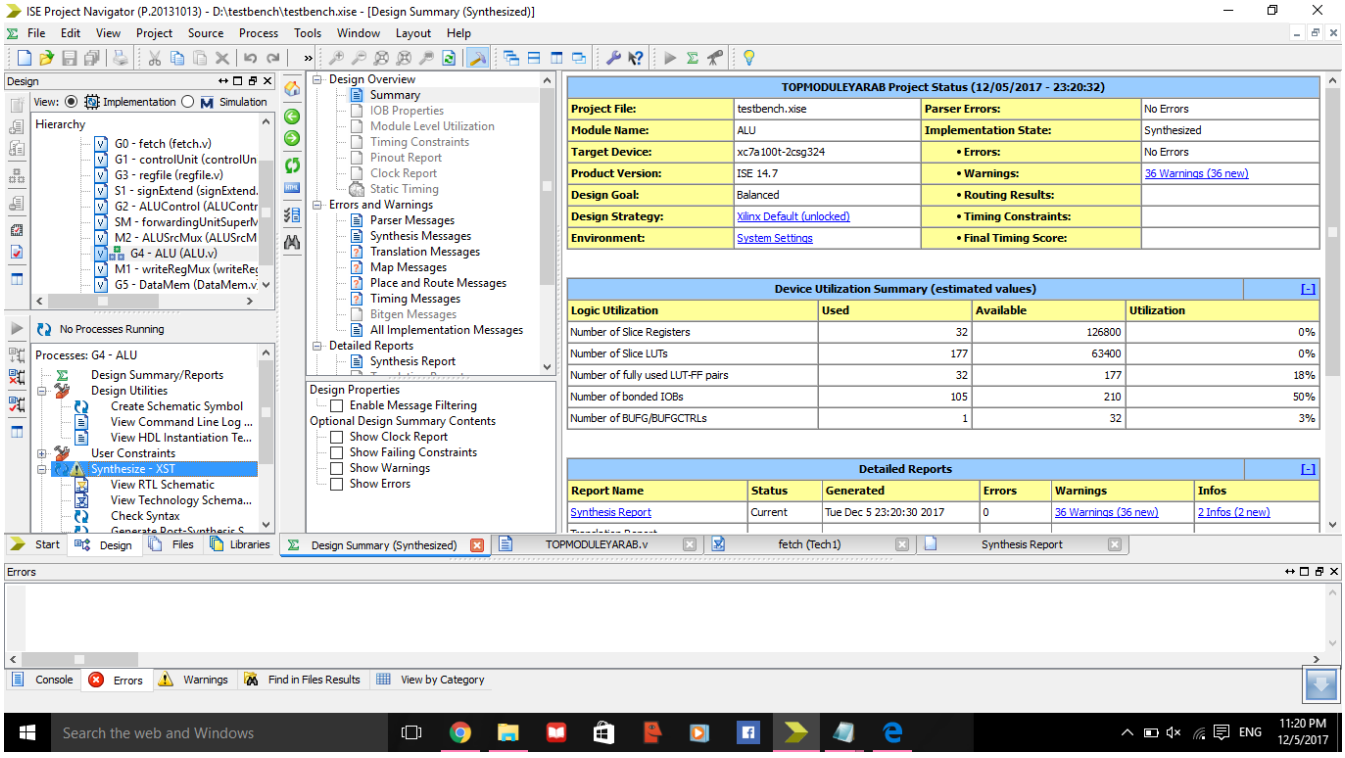
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:18:00)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: ALUControl
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: 3 Warnings (3 new)
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice LUTs | 7 | 63400 | 0%
Number of fully used LUT-FF pairs | 0 | 7 | 0%
Number of bonded IOBs | 11 | 210 | 5%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:17:59 2017 | 0 | 3 Warnings (3 new) | 1 Info (1 new)
Translation Report
Map Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:18 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
G0 - fetch (fetch.v)
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSup
M2 - ALUSrcMux (ALUSrcM
G4 - ALU (ALU.v)
M1 - writeRegMux (writeReg
G5 - DataMem (DataMem.v
No Processes Running
Processes: SM - forwardingUnitSuperMux
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:18:33)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: forwardingUnitSuperMux
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: No Warnings
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice LUTs | 64 | 63400 | 0%
Number of fully used LUT-FF pairs | 0 | 64 | 0%
Number of bonded IOBs | 196 | 210 | 93%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:18:31 2017 | 0 | 0 | 0
Translation Report
Map Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:18 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
G0 - fetch (fetch.v)
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperM
M2 - ALUSrcMux (ALUSr
G4 - ALU (ALU.v)
M1 - writeRegMux (writeReg
G5 - DataMem (DataMem.v
No Processes Running
Processes: M2 - ALUSrcMux
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:20:05)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: ALUSrcMux
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: No Warnings
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization Used Available Utilization
Number of Slice LUTs 32 63400 0%
Number of fully used LUT-FF pairs 0 32 0%
Number of bonded IOBs 97 210 46%
Detailed Reports
Report Name Status Generated Errors Warnings Infos
Synthesis Report Current Tue Dec 5 23:20:03 2017 0 0 0
Translation Report
Map Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:20 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
G0 - fetch (fetch.v)
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperM
M2 - ALUSrcMux (ALUSrcM
G4 - ALU (ALU.v)
M1 - writeRegMux (writeReg
G5 - DataMem (DataMem.v
No Processes Running
Processes: G4 - ALU
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
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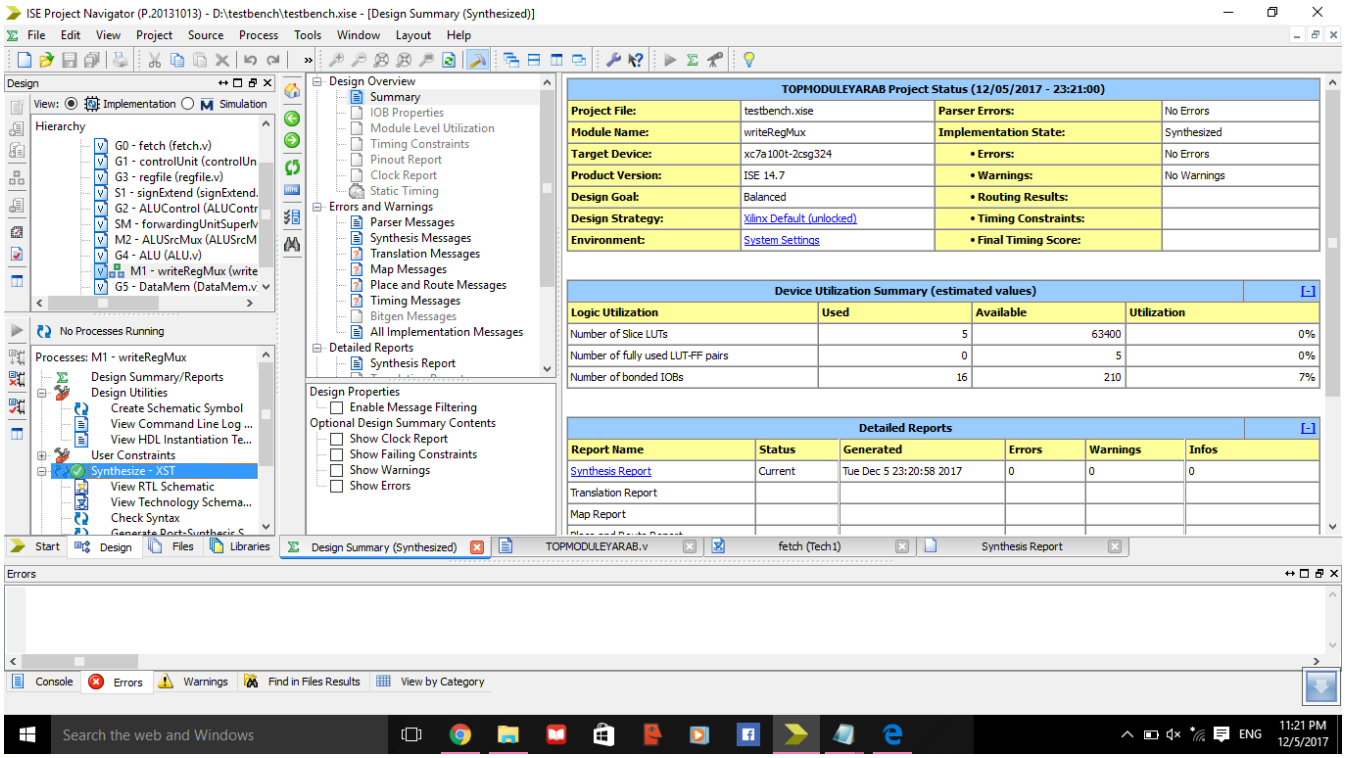
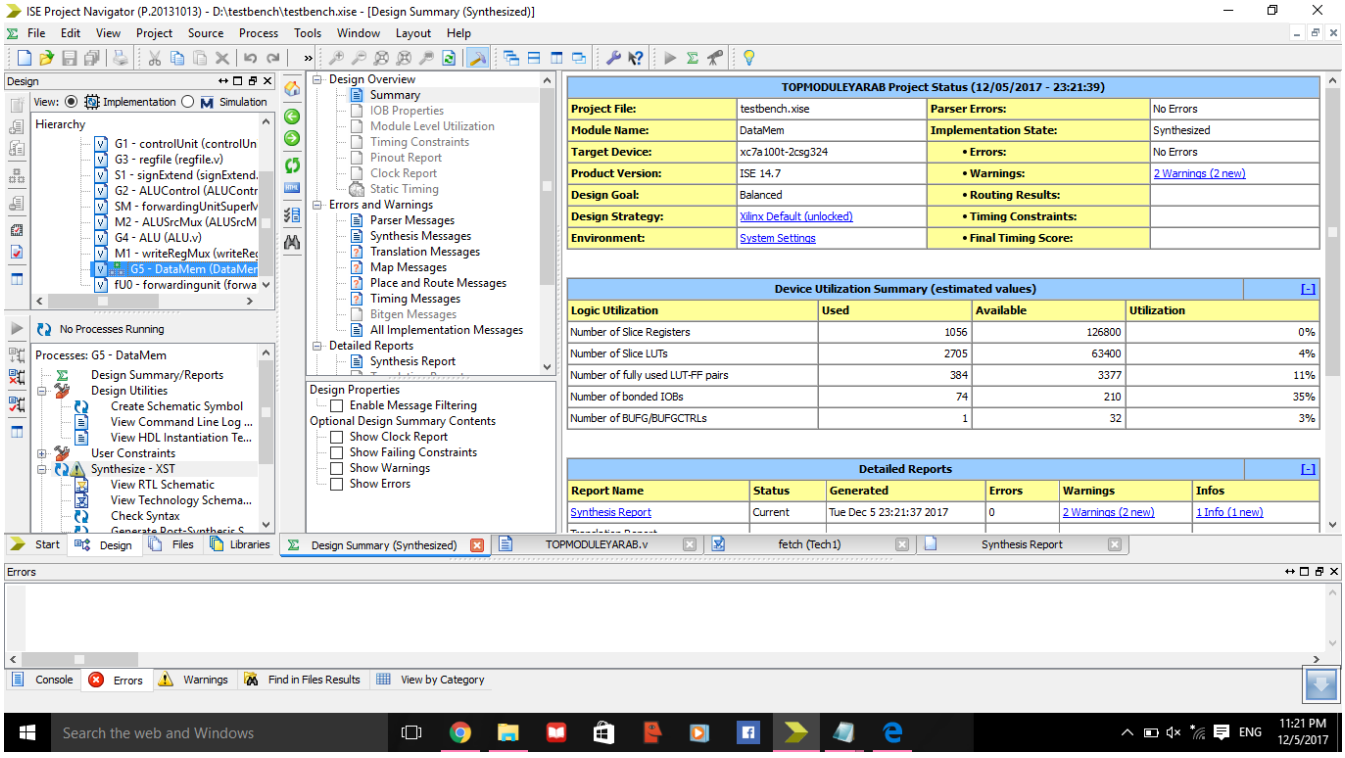
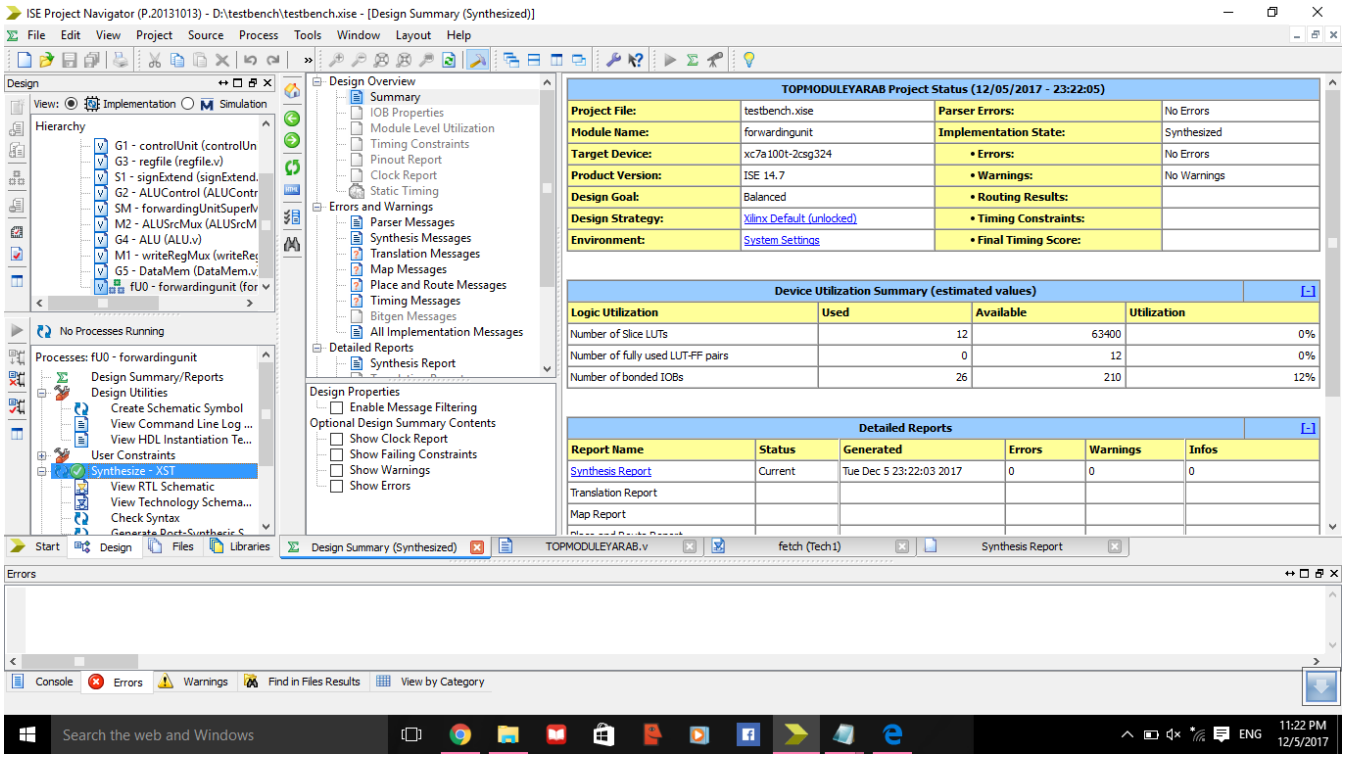
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:20:32)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: ALU
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: 36 Warnings (36 new)
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization Used Available Utilization
Number of Slice Registers 32 126800 0%
Number of Slice LUTs 177 63400 0%
Number of fully used LUT-FF pairs 32 177 18%
Number of bonded IOBs 105 210 50%
Number of BUFG/BUFGCTRLs 1 32 3%
Detailed Reports
Report Name Status Generated Errors Warnings Infos
Synthesis Report Current Tue Dec 5 23:20:30 2017 0 36 Warnings (36 new) 2 Infos (2 new)
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:20 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
G0 - fetch (fetch.v)
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperV
M2 - ALUSrcMux (ALUSrcM
G4 - ALU (ALU.v)
M1 - writeRegMux (write
G5 - DataMem (DataMem.v
No Processes Running
Processes: M1 - writeRegMux
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:21:00)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: writeRegMux
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: No Warnings
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice LUTs | 5 | 63400 | 0%
Number of fully used LUT-FF pairs | 0 | 5 | 0%
Number of bonded IOBs | 16 | 210 | 7%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:20:58 2017 | 0 | 0 | 0
Translation Report
Map Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:21 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperV
M2 - ALUSrcMux (ALUSrcM
G4 - ALU (ALU.v)
M1 - writeRegMux (writeReg
G5 - DataMem (DataMem
fU0 - forwardingunit (forwa
No Processes Running
Processes: G5 - DataMem
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:21:39)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: DataMem
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: 2 Warnings (2 new)
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization | Used | Available | Utilization
Number of Slice Registers | 1056 | 126800 | 0%
Number of Slice LUTs | 2705 | 63400 | 4%
Number of fully used LUT-FF pairs | 384 | 3377 | 11%
Number of bonded IOBs | 74 | 210 | 35%
Number of BUFG/BUFGCTRLs | 1 | 32 | 3%
Detailed Reports
Report Name | Status | Generated | Errors | Warnings | Infos
Synthesis Report | Current | Tue Dec 5 23:21:37 2017 | 0 | 2 Warnings (2 new) | 1 Info (1 new)
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:21 PM
12/5/2017


ISE Project Navigator (P.20131013) - D:\testbench\testbench.xise - [Design Summary (Synthesized)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
G1 - controlUnit (controlUn
G3 - regfile (regfile.v)
S1 - signExtend (signExtend.
G2 - ALUControl (ALUContr
SM - forwardingUnitSuperM
M2 - ALUSrcMux (ALUSrcM
G4 - ALU (ALU.v)
M1 - writeRegMux (writeReg
G5 - DataMem (DataMem.v
fU0 - forwardingunit (for
No Processes Running
Processes: fU0 - forwardingunit
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log ...
View HDL Instantiation Te...
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schema...
Check Syntax
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Static Timing
Errors and Warnings
Parser Messages
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Implementation Messages
Detailed Reports
Synthesis Report
Design Properties
Enable Message Filtering
Optional Design Summary Contents
Show Clock Report
Show Failing Constraints
Show Warnings
Show Errors
TOPMODULEYARAB Project Status (12/05/2017 - 23:22:05)
Project File: testbench.xise
Parser Errors: No Errors
Module Name: forwardingunit
Implementation State: Synthesized
Target Device: xc7a100t-2csg324
• Errors: No Errors
Product Version: ISE 14.7
• Warnings: No Warnings
Design Goal: Balanced
• Routing Results:
Design Strategy: Xilinx Default (unlocked)
• Timing Constraints:
Environment: System Settings
• Final Timing Score:
Device Utilization Summary (estimated values)
Logic Utilization Used Available Utilization
Number of Slice LUTs 12 63400 0%
Number of fully used LUT-FF pairs 0 12 0%
Number of bonded IOBs 26 210 12%
Detailed Reports
Report Name Status Generated Errors Warnings Infos
Synthesis Report Current Tue Dec 5 23:22:03 2017 0 0 0
Translation Report
Map Report
Start Design Files Libraries
Design Summary (Synthesized)
TOPMODULEYARAB.v
fetch (Tech1)
Synthesis Report
Errors
Console Errors Warnings Find in Files Results View by Category
Search the web and Windows
ENG
11:22 PM
12/5/2017