Final Report Outline & Guidelines

Purpose:

In industry or academia, project reports are an unavoidable step in the process of maintaining funding, staff, and space to be able to carry out a design or research project. In the case of ECE337, it is an unavoidable step in passing the course. A project report is used to describe what you have accomplished in previous or current projects in an effort to update or remind others of the positive results achieved with resources that they previously provided, are currently providing, or you would like them to provide. Investors expect to be informed of the progress you are currently making with your resources, as well as what you were able to accomplish with previous resources as part of deciding whether to start, continue, or if need stop investing in your design/research team.

You will find that the structure of the final report document is very similar to the full proposal. Assuming that the scope of your project hasn't changed dramatically, the final report will just be an update to your proposal. Be sure to update the sections to reflect the changes to your design you have made since your proposal was written. Take into consideration the comments made by your TA and instructor on your proposal.

Make sure to follow the outline provided below, deviations from this format will count against your score.

0. Title page (1 page)

This should contain the title of your project, the words "Final Report", your name, your partners' names, the name of this class (ECE337), your lab day and time, the date the report is due, and your TA's name. At the bottom, all people who prepared the report should place their signatures indicating that they have reviewed the entire report and approve of its contents. Everything should be centered and neatly spaced on a single page.

1. Executive Summary (1/2 to 1 page)

The executive summary is the first part of your report. Company executives or prospective investors will look at this to decide whether or not to bother with the rest of the report. **Assume that the reader of the executive summary is either an executive or investor.** The reader of the rest of the report would probably be someone who can evaluate the technical merits. The executive summary should be short, to the point, and give the reader some reason to want to buy or produce your design. Keep in mind that what all you have done this semester is to design a simulatable prototype of the design. Before actually making a product out of it, far more testing and verification is likely be required. The summary should answer very briefly the following questions:

- What did you design?
- Why is it important? (is there a big market for it? will it save the company time or money?)

- What is unique about your design that will make it important?
- What is in the rest of the report?

2. Design Specifications

See original proposal guidelines for what is needed in this section. This section shouldn't change much from your original proposal unless there are significant changes in the objectives for your design or unless significant improvements were required to your original proposal.

2.1. Interfacing Specifications

This section should describe the intended use of the design and should include what external devices and/or standards are required to interface with your design. The purpose of this diagram is to enable system builders and designers to quickly develop a basic understanding of how your design could be used in various systems, so that they can quickly decide if the design has the potential to fulfill a needed role in a their system or not. With this in mind, this section should contain:

- The System Usage Diagram as specified in the full proposal guidelines
- A complete list of implemented standards and/or protocols
- A complete list of required interface standards and/or protocols, including:
    - Transmission rates for communication interfaces
    - Communication/Data formatting used if not governed by an existing standard
- A quick list of the features of the design

2.2. Operational Characteristics (3 to 10 pages)

See original proposal guidelines for what is needed in this section. The only substantial change is to provide more detail regarding top level input/output ports. Do not include signals that are internal to your chip in this section. See the sample table below for the additional required information. Otherwise, this section shouldn't change much from your original proposal unless there are significant changes in the objectives for your design or unless significant improvements were required to your original proposal. Describe the intended operation of the chip using as many of the following approaches as are appropriate for the type of design you are creating.

- A timing diagram illustrating the sequence of operation of the chip.
- A flow-chart or state transition diagram illustrating the sequence of operations or operating modes of the chip.
- If the design includes mathematical computation, describe the computation in the form or either pseudo-code (like you might find in a book on algorithms), mathematical equations, or a data-flow diagram illustrating the computation (like you might see in a book on signal processing or control systems)

Try to imagine yourself in the position of a designer who has to use your chip with only your documentation to work from. You need a concise and complete specification of the chip.

Also, make sure to use sub-headers to break up this section into the different function/logic groups, ie at least use a sub-header for the pin-out table and another one for the section describing the operation of the chip.

Table 1: Example Pin-out Table

Signal Name	Type In/Out/Bidir.	Number of bits	Data Format or Active High/Low	Description, timing constraints
RST	IN	1	Active High	Asynchronous reset for all memory elements in the design. High-low transition must not occur within 0.2ns of active clock edge.
Address	IN	16	Unsigned binary number	Address output to byte addressable memory. Output value is undefined except when Memory Read-enable or Write-enable are also asserted.

2.3. Requirements (up to 1 page)

This section shouldn't change much from your original proposal unless there are significant changes in the objectives for your design

See original proposal guidelines.

3. Final Design

3.1. Design Architecture

This section shouldn't change much from your original proposal unless there are significant changes in the objectives for your design

See original proposal guidelines.

3.2. Functional Block Diagram (typically 2 to 10 pages)

This sub-section is very similar to the "Initial Design" in your proposal, but it should be based on up to date diagrams for your design. You should break up the diagrams hierarchically. Include a brief description of the function performed by each block and the type of circuitry contained in the block such as a simple state machine, shift register, multiplexer, combinational multiplier, etc.

3.3. Standards and Protocols (1 to 3 pages)

This section should provide the rationale for the various external devices, standards, protocols you chose for you design to either internally implement or require for interfacing. While they have been

described in section 2.1 that section's purpose is to provide a system builder with a image of what your design requires to work as well how it could fit in a system, this section's purpose is to explain the design decisions you made to chose those requirements and features. Justify your choices in terms of the benefits to the user of your chip such as reduced cost, higher performance, reduced circuit board size, etc. This section should refer to excerpts from data sheets to be included in your appendix.

3.4. Timing and Area Budgets (2 to 3 pages)

Prepare a summary of the following data, arranged in a table to allow comparison:

- Critical path constraint (1/clock rate) and area targets from your proposal success criteria.
- Critical path (delay and start/end location) and total area from your design budgeting assignment. Estimate the dimensions of the I/O pad frame as shown in the course notes. Indicate whether your design is core bound or I/O bound (again, see course notes)
- Critical path (delay and start/end location) and area estimates based on final synthesis report results (if different from design budgeting assignment)
- Critical path and area reported by SOC Encounter

Comment on possible reasons for differing results from your budgeting assignment, final synthesis results, and final layout results. If you failed to meet the initial delay (clock rate) and area targets, explain why you could not meet this targets and what steps you took to bring your design closer to the targets (this may help you in terms of partial credit on the success criteria).

4. Testing (2 to 4 pages)

Testing is the most crucial stage in any VLSI design effort. Many of the best designed VLSI chips, even from the largest companies, do not work when initially fabricated because they were not tested adequately. This wastes time and vast sums of money. In this section, outline the chip level functions you tested as well as the steps you took to verify each block at each level of hierarchy. Identify any special or illegal operating conditions that need be tested. Include timing as well as functional tests to make sure your design meets specifications.

In the appendix, reference locations of the test benches you used, along with some explanation of each test in the form of comments in the test bench file. Snapshots of the most interesting test waveforms should be included in the appendix.

5. Layout (1 page)

You will need to have your design synthesized in order to have a layout created. This section is simply a picture of your layout that was auto generated for you by SOC Encounter and then imported into Virtuoso (icfb). Include a table describing the layout parameter values you used (aspect ratio, row utilization, etc.) and the results you got (dimensions, area in mm2, number of gates). Make sure that there are no gaps between I/O pads and that the layout is complete and passes the connectivity and geometry checks without errors.

6. Results (1 page)

List all fixed as well as design specific success criteria. Design specific success criteria must have already been approved by your TA and/or instructor. For each criterion, give your status: completed, partially completed, or not completed at all. If a criterion is partially completed, briefly describe the extent to which it is completed. Note: deficiencies in testing or demonstration of your success criteria may result in a lower instructor assessment of the extent to which you met your success criteria. Inconsistencies between your actual level of success and statements in this paragraph will result in a loss of points for this section.

7. Appendix A - Data Sheets and Guide to Design Data (1 to 4 pages not counting data sheets)

This section should serve as a guide and index to your data sheets and design data. Before writing this section, organize all of your design VHDL code, all mapped VHDL code, scripts, test benches, schematics, electronic copies of datasheets, a copy of the PowerPoint file (or pdf) used in the final presentation, and synthesis and layout report files into a single new project directory in one of your project accounts. Make sure that all design and test bench code contains a meaningful description in the form of header comments.

Now that your data is organized, prepare something that looks like a table of contents, except that instead of section titles and page numbers you give short descriptions and file names. Use indentation and blank lines to make it easier to read. Your listing in the report should look something like:

Account and directory where all of the files are located: mg999/ECE337/Project

Top level structural VHDL code source/TopLevel.vhd

Control Unit source/MainCtrl.vhd

State Counter source/StCnt.vhd

Test Benches

Simple top level test source/tb_TopLevel1.vhd

Advanced top level test source/tb_TopLevel2.vhd

Organize report files, scripts, presentation, and datasheets in a similar manner with appropriate subdirectories.

8. Appendix B – Simulation Results (no page limit)

Include as many simulation results as necessary to illustrate how your design satisfies all design specific success criteria. In most cases, these results should be presented as waveforms from Modelsim (TM), but depending on the function of your design it may also help to present outputs generated by scripts that you wrote to analyze the simulation results. Annotate all pictures with arrows and text to identify key details and include a short description of what is demonstrated.

If all blocks are working together correctly in the mapped simulation, only use whole-chip results to demonstrate success criteria. If some features only work at the block level, present block level simulation results for those features for partial credit.

Overall Report Format

Single spaced, 12 point font for text, 14 point for section headers. Include page numbers at the bottom center of each page. All illustrations must be computer generated and have appropriate figure designations and captions. Approximate number of pages: 15 to 35 pages not including appendices. The report must be either in pdf or MS Word format. Name the file in the following manner:

[last name]_[first name]_report.pdf or [last name]_[first name]_report.doc

where [last name] and [first name] correspond to the last and first names of one of the project team members (last and first names must be for the same person).

The report is to be submitted in through the posted Blackboard Assignment.