ECE337 Full Project Proposal Outline & Guidelines

Purpose:

In industry or academia, proposals are an unavoidable step in the process of getting money, staff, and space to be able to carry out a design or research project. In the case of ECE337, it is an unavoidable step in passing the course. A proposal is used to describe what you want to do so as to persuade others to provide resources for your project. If people are giving you money and staff to develop a project, then they expect you to already have a good idea of what you want to do, how you want to do it, and what is needed in order to do it. Consequently, some of the research and design work already has to be done before you even present your proposal in order for anyone to believe it.

These sections are also similar to what you might find in industry. Deviations from this format will count against you. Keep in mind also that your final report will also include much of the same information. Therefore, a good job on the proposal will save you time later. **Be warned! You have to make several design decisions in order to write a reasonable proposal. This should become apparent as you read the requirements for this proposal.** In some cases you may feel like you don't know enough to make the necessary design decisions. You might have to guess or make some arbitrary choices. That is ok. Even if you are confident of what you are going to do, you will probably have to make some corrections as you get into the details of the design.

0. Title page (1 page)

This should contain the title of your project, the words "Full Proposal", your name, your partners' names, the name of this class (ECE337), your lab day and time, the date the report is due, and your TA's name. At the bottom, all people who prepared the report should place their signatures indicating that they have reviewed the entire report and approve of its contents. Everything should be centered and neatly spaced on a single page.

1. Executive Summary (from 1/2 to 1 page)

The executive summary is the first part of your proposal. Company executives or prospective investors will look at this to decide whether or not to bother with the rest of the proposal. **Assume that the reader of the executive summary is an executive or investor.** The reader of the rest of the proposal would probably be someone who can evaluate the technical merits. The executive summary should be short while giving the reader some reason to want to give you resources for implementation. The summary should answer the following questions:

- What is it you want to design and build?
- Why is it important? (is there a market for it? will it save the company time or money?)
- What will be unique about your design that will make it important?
- Why is this design appropriate for an ASIC implementation
- What will it take to do it?
- What is in the rest of the proposal?

2. Design Specifications

This section describes the chip you are designing. The description should include (but is not limited to) the following sections.

The chip you specify here must be consistent with the project idea already approved by your TA or instructor (in writing, or email in the TA or instructor's possession). If the idea you are writing is different from what was approved, be sure to clear the idea first.

2.0. System Usage Diagram

You need to create a super high-level block diagram that illustrates how your intended use of the design and must show what external devices will connect to your design and how they will be connected in terms of interface standards and the types of information that will be sent between them. The purpose of this diagram is to enable system builders and designers to quickly develop a basic understanding of how your design could be used in various systems, so that they can quickly decide if the design has the potential to fulfill a needed role in a their system or not.

2.1. Operational Characteristics (between 2 and 6 pages for most projects)

You need to describe the functions that are to be performed by your chip. This section should provide the most detail into your chip's operation. First, identify all external input and output pins of the chip. For this purpose, include a table listing all inputs and outputs of your chip including clock, reset, power, ground, and all data signals unique to your design. Organize the table as shown below. For the design review, you will be required to refine the input/output descriptions to specify data formats, active high/low, and timing requirements.

Signal Name	Type In/Out/Bidir.	Number of bits	Description
RST	IN	1	Asynchronous reset for all memory elements in the design.

Inputs and outputs need to be specified in a way that will be compatible with the external devices to which your chip will be connected. For example, if your chip needs to interface with a keypad, it is NOT reasonable to have a separate input pin for each button. Find a commercially available keypad datasheet online and see how the inputs and outputs work.

Identify the general type of commercial part to which your final chip would be connected, and any relevant industry standards for data interfaces. For the design review to come later you will need to provide a copy of relevant data sheets and/or standards documents. Note: because of the limited time for this project, you may find it necessary to use simplified versions of some industry standard or commercial interfaces.

Describe the intended operation of the chip using one or more of the following approaches depending on what is appropriate for the type of design you are creating.

- A timeline describing the sequence of operation of the chip.
- A list of features or functional blocks with an explanation of each.

Where possible, use tables, charts, state transition diagrams, or timing diagrams accompanied by some explanatory text to describe functions of your chip. If your chip requires a particular format for input data, memory contents, or output data, indicate that a detailed data format will need to be defined.

Try to imagine yourself in the position of a designer who has to use your chip with only your documentation to work from. You need a concise and complete specification of the chip.

2.2. Requirements (1/2 to 1 page)

Include a discussion of how the intended application affects special requirements for your chip. For example, a hand held game probably requires low power dissipation and a small pin count. An automotive application might require tolerance of wide temperature variations and rugged packaging. For your chip, what are the most critical design parameters? Speed? Low Power? Area? High I/O bandwidth? Think about the environment in which the chip has to operate and how it is to be packaged.

Indicate whether your primary optimization objective is going to be speed or minimum area. If the speed requirements for your design are not very tight, then you will be required to optimize for minimum area. Minimizing area reduces the chances of manufacturing defects and will often also reduce power. Be advised that just telling the synthesis program to optimize for area will not be enough. Find ways to structure your design to minimize the size of the design. If speed requirements are tight, you should still try to minimize area when possible, but only as a second priority. Again, just telling the synthesis program to optimize speed is not enough. Think about ways of structuring your design that will make it fast. In the upcoming design review, you will need to explain the steps you are taking to optimize your design.

Finally, your target for total chip area is to be no more than 3mm x 3mm, total input/output pins no more than 40, clock rate, and data throughput (in bytes/second for communication interfaces) based on the intended application. Throughput will depend on the application. For example, if you are sending 16 bit uncompressed CD quality audio, your throughput in one direction will need to be on the order of 44100 samples/sec x 2 bytes per channel /sample x 2 channels = 176,400 bytes per second. Usually, clock rate will need to be significantly higher than the throughput unless your design is heavily pipelined (pipelining is something most of you will learn in ECE437 & isn't realistically expected this semester).

The pin count and the area constraint are based on the size of chip and package that we are usually able to fabricate at no charge through the MOSIS Service - a silicon fabrication broker located as the University of Southern California. MOSIS receives funding and silicon space from industry for

fabrication of student projects. Even though most of your projects will not be fabricated, meeting these area and pin count targets is good practice and it increases the chances of being able to fabricate more student designs in the future.

3. Initial Design (2 to 4 pages)

3.1. Design Architecture

You a required to have an architectural block diagram of your chip completed with the proposal. The level of detail of the architectural block diagram should be such that it consists of high-level functional blocks, i.e. a DVI interface, USB transceiver, Master Control Module, Memory Arbiter, etc. Draw arrows with labels to identify any essential data that has to flow from one block to another. External inputs and outputs should be consistent with the descriptions in the operational characteristics section.

3.2. Functional Block Diagrams

You a required to have a separate block level diagram for each function block in your architectural diagram completed with the proposal. The level of detail of these block diagrams should be similar to the block diagrams you were given for labs 5 and 6. Each block in the diagram needs to be something that be reasonably implemented in hardware - such as a state machine, counter, memory, arithmetic calculation, etc. Draw arrows with labels to identify any essential data that has to flow from one block to another. External inputs and outputs should be consistent with the descriptions in the operational characteristics section. Include a short (one or two sentence) description of each block and how it relates the functions described in section 2. Later, for the design review, you will need to refine the block diagram to explicitly show each register and combinational logic block (i.e., at the RTL level)

4. Projected Timeline and Division of Tasks (1/2 page)

This section of the proposal should be a projected timeline for your progress on the project. Given the short duration of this project, your schedule will be mostly determined by project related deadlines, but it is still wise to think about what you need to get done each week. So, tell us what you expect to have accomplished each week. This is to help us measure your progress and help you finish on time. Give specific goals each week. Example goals: week 1: enter VHDL code for input and display blocks, week 2: test input and display blocks together,..., week 3: prepare documents for midterm design review, week 4: layout and route chip.

Fixed milestones are as follows:

Week 1	Proposal submitted
Week 2	Documents for design review: detailed RTL drawings, data sheets, relevant standards, and timing and area budgets
Week 3	Design review
Week 7	Final Presentation, demonstration, report

Along with your timeline, specify which team members will be responsible for each task, for each major piece of the design, and for each major portion of testing. List the team members. For each

member, list the tasks accepted by that person. Identify one person to be responsible for monitoring progress and negotiating task distribution..

The task assignments may change as you work on your project, but it is important to make sure that every task has someone who will take responsibility for it. No matter what, every team member is expected to make a tangible contribution to the design and testing of your project. All team members will be surveyed at the end of the project to find out who contributed what to the project. Failure to contribute something meaningful to both the design and testing will fail the project outcome, and therefore the entire course.

5. Success Criteria (1/2 to 1 page)

The last section of the proposal will be a list of the criteria to be used in determining whether or not you met your project objectives. Your technical accomplishment score will be based on these criteria. Some criteria will be the same for every project (such as produce a complete IC layout) and are given below. Other criteria will be project dependent and must be specified by you. However, your TA and instructor both reserve the right to modify your success criteria and point allocation at their discretion as your proposal is being graded. After the proposal is submitted, you may not change your success criteria without documented agreement of your TA or instructor.

5.1. Fixed criteria: (total 12 points)

1. (2 points) Test benches exist for all top level components and the entire design. The test benches for the entire design can be demonstrated or documented to cover all of the functional requirements given in the design specific success criteria.
2. (4 points) Entire design synthesizes completely, without any inferred latches, timing arcs, and, sensitivity list warnings.
3. (2 points) Source and mapped version of the complete design behave the same for all test cases. The mapped version simulates without timing errors except at time zero.
4. (2 points) A complete IC layout is produced that passes all geometry and connectivity checks.
5. (2 points) Your total area, including I/O pads, is no more than 3mm x 3mm and your required pin count (including power and ground) is no more than 40. For half credit on these criteria, your constraints are 10mm x 10mm and 100 pins.

5.2. Design specific criteria (total 8 points)

Up to 6 design specific criteria and no less than 3. Allocate a total of 8 points to these criteria. Each criterion must be state in the form: “Demonstrate by simulation of VHDL test benches that the complete design is able to...” For example, criteria for an I2C bus design could include:

- Demonstrate by simulation of a VHDL test bench that the I2C interface ignores start commands followed by an invalid address.
- Demonstrate by simulation of a VHDL test bench that data transmitted serially on the I2C bus matches the data originally written into the transmit FIFO.

You may use one success criteria to cover some unique feature that you plan to incorporate into your test bench or other software used to facilitate demonstration of your design.

Note: at the end of the semester, project difficulty will be added to your technical accomplishment score as follows:

+2 points - substantially more complex than what we would expect of an ECE337 project

+0 points - appropriate difficulty for the size of team (approximately equal in complexity to lab 6 per person)

-2 points - unusually low complexity

-10 points - trivial

In the past, most projects have been categorized in the 0 point, appropriate difficulty category.

Comments and advice (not a section of the report)

It is recommended that the students preparing the proposal use the proposal grade sheet as a guide to the amount of work put forth in each section. Keep in mind that your TA will use the grade sheet when scoring your document.

Extra points may be deducted and the TA may refuse grading if the grammar and spelling contained in any formal documentation for this course is extremely poor.

Format, and method of submission

Format: single spaced, 12 point fonts for text, 14 point for section labels. Margins no more than 1 inch on each side.

Length: minimum 7 pages, typical 10 pages, maximum 14 pages.

There will be a blackboard assignment for submitting your full project proposal. Submissions must be a single PDF file.