### RCB Hardware Software Interface Document

### FPGA Version

Address: 0x0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:16 | SPARE | R-O |  | Set to ‘0’ |
| 15:8 | FPGA\_MAJOR\_VER | R-O |  | Increase by one for every major change |
| 7:0 | FPGA\_REV | R-O |  | Increase by one for every change! |

### FPGA REV Data, Time

Address: 0x1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31-24 | FPGA\_REV\_YEAR | R-O | Unsigned, Decimal | Rev year in Decimal format |
| 23-16 | FPGA\_REV\_MONTH | R-O | Unsigned, Decimal | Rev Day in decimal format |
| 15:8 | FPGA\_REV\_DAY | R-O | Unsigned, Decimal | Rev Month in decimal format |
| 7:0 | FPGA\_REV\_HOUR | R-O | Unsigned, Decimal | Rev Time (Hour) in decimal format |

### FPGA Power Diagnostic

Address: 0x2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:2 | SPARE | R-O |  | Set to ‘0’ |
| 1 | Power OK from Power supply Sticky | R-W | 1-Power OK  0-Power Fail | Sticky Power OK signal, set by PS Error, cleared by Write ‘1’ |
| 0 | Power OK from Power supply RT | R-O | 1-Power OK  0-Power Fail | Real time Power O.K signal |

### FPGA buttons

Address: 0x3

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:8 | SPARE | R-W |  | Set to ‘0’ |
| 3 | RIGHT\_TOOL\_EXCHANGE\_BUTTON\_NC | R-O | 1-PRESSED |  |
| 2 | RIGHT\_TOOL\_EXCHANGE\_BUTTON\_NO | R-O | 1-PRESSED |  |
| 1 | LEFT\_TOOL\_EXCHANGE\_BUTTON\_NC | R-O | 1-PRESSED |  |
| 0 | LEFT\_TOOL\_EXCHANGE\_BUTTON\_NO | R-O | 1-PRESSED |  |

### FPGA Drape switch state

Address: 0x4

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:2 | SPARE | R-W |  | Set to ‘0’ |
| 1 | RIGHT\_DRAPE\_SWITCH | R-O | 1-PRESSED |  |
| 0 | LEFT\_DRAPE\_SWITCH | R-O | 1-PRESSED |  |

### FPGA Drape electromagnet state

Address: 0x5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:2 | SPARE | R-W |  | Set to ‘0’ |
| 1 | LEFT DRAPE\_ELECTROMAGNET\_STATE | R-O | 1-RELEASED |  |
| 0 | LEFT DRAPE\_ELECTROMAGNET\_STATE | R-O | 1-RELEASED |  |

### FPGA Drape electromagnet S.W approval

Address: 0x6

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:9 | SPARE | R-W |  | Set to ‘0’ |
| 8 | RIGHT\_DRAPE\_ELECTROMAGNET\_OPEN | R-W | 1-OPEN DRAPE |  |
| 7-1 | SPARE | R-W |  | Set to ‘0’ |
| 0 | LEFT\_DRAPE\_ELECTROMAGNET\_OPEN | R-W | 1-OPEN DRAPE |  |

### FPGA Drape Sensors

Address: 0x7

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:14 | SPARE | R-W |  | Set to ‘0’ |
| 13 | RIGHT DRAPE CLOSE 2 NC STATE | R-O | 1-PRESSED |  |
| 12 | RIGHT DRAPE CLOSE 2 NO STATE | R-O | 1-PRESSED |  |
| 11 | RIGHT DRAPE CLOSE 1 NC STATE | R-O | 1-PRESSED |  |
| 10 | RIGHT DRAPE CLOSE 1 NO STATE | R-O | 1-PRESSED |  |
| 9 | RIGHT DRAPE OPEN NC STATE | R-O | 1-PRESSED |  |
| 8 | RIGHT DRAPE OPEN NO STATE | R-O | 1-PRESSED |  |
| 7:6 | SPARE | R-W |  | Set to ‘0’ |
| 5 | LEFT DRAPE CLOSE 2 NC STATE | R-O | 1-PRESSED |  |
| 4 | LEFT DRAPE CLOSE 2 NO STATE | R-O | 1-PRESSED |  |
| 3 | LEFT DRAPE CLOSE 1 NC STATE | R-O | 1-PRESSED |  |
| 2 | LEFT DRAPE CLOSE 1 NO STATE | R-O | 1-PRESSED |  |
| 1 | LEFT DRAPE OPEN NC STATE | R-O | 1-PRESSED |  |
| 0 | LEFT DRAPE OPEN NO STATE | R-O | 1-PRESSED |  |

### FPGA Wheel driver out

Address: 0x8

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:8 | SPARE | R-W |  | Set to ‘0’ |
| 7 | WHEEL DI7 | R-W |  | Output to driver |
| 6 | WHEEL DI6 | R-W |  | Output to driver |
| 5 | WHEEL DI5 | R-W |  | Output to driver |
| 4 | WHEEL DI4 | R-W |  | Output to driver |
| 3 | WHEEL DI3 | R-W |  | Output to driver |
| 2 | WHEEL DI2 | R-W |  | Output to driver |
| 1 | WHEEL DI1 | R-W |  | Output to driver |
| 0 | WHEEL DI0 | R-W |  | Output to driver |

### FPGA Wheel driver ELO (Currently in FPGA 3.2 ELO is not used)

Address: 0x9

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:1 | SPARE | R-W |  | Set to ‘0’ |
| 0 | WHEEL DRIVER ELO | R-W |  | ELO line to driver |

### FPGA Wheel driver in

Address: 0xA

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:4 | SPARE | R-W |  | Set to ‘0’ |
| 3 | WHEEL DO3 | R-W |  | Input from driver |
| 2 | WHEEL DO2 | R-W |  | Input from driver |
| 1 | WHEEL DO1 | R-W |  | Input from driver |
| 0 | WHEEL DO0 | R-W |  | Input from driver |

### FPGA Wheel driver ABRT\RST(Currently in FPGA 3.2 ELO is not used)

Address: 0xB

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:2 | SPARE | R-W |  | Set to ‘0’ |
| 1 | WHEEL RST | R-W |  | RST line to driver |
| 0 | WHEEL ABRT | R-W |  | ABRT line to driver |

### FPGA WHEEL sensors status

Address: 0xC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:24 | SPARE | R-W |  | Set to ‘0’ |
| 23 | WHEEL D SENSOR 3 IN 2 | R-O |  |  |
| 22 | WHEEL D SENSOR 3 IN 1 | R-O |  |  |
| 21 | WHEEL D SENSOR 2 IN 2 | R-O |  |  |
| 20 | WHEEL D SENSOR 2 IN 1 | R-O |  |  |
| 19 | WHEEL D SENSOR 1 IN 2 | R-O |  |  |
| 18 | WHEEL D SENSOR 1 IN 1 | R-O |  |  |
| 17 | WHEEL C SENSOR 3 IN 2 | R-O |  |  |
| 16 | WHEEL C SENSOR 3 IN 1 | R-O |  |  |
| 15 | WHEEL C SENSOR 2 IN 2 | R-O |  |  |
| 14 | WHEEL C SENSOR 2 IN 1 | R-O |  |  |
| 13 | WHEEL C SENSOR 1 IN 2 | R-O |  |  |
| 12 | WHEEL C SENSOR 1 IN 1 | R-O |  |  |
| 11 | WHEEL B SENSOR 3 IN 2 | R-O |  |  |
| 10 | WHEEL B SENSOR 3 IN 1 | R-O |  |  |
| 9 | WHEEL B SENSOR 2 IN 2 | R-O |  |  |
| 8 | WHEEL B SENSOR 2 IN 1 | R-O |  |  |
| 7 | WHEEL B SENSOR 1 IN 2 | R-O |  |  |
| 6 | WHEEL B SENSOR 1 IN 1 | R-O |  |  |
| 5 | WHEEL A SENSOR 3 IN 2 | R-O |  |  |
| 4 | WHEEL A SENSOR 3 IN 1 | R-O |  |  |
| 3 | WHEEL A SENSOR 2 IN 2 | R-O |  |  |
| 2 | WHEEL A SENSOR 2 IN 1 | R-O |  |  |
| 1 | WHEEL A SENSOR 1 IN 2 | R-O |  |  |
| 0 | WHEEL A SENSOR 1 IN 1 | R-O |  |  |

### FPGA Buttons LED

Address: 0xD

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 0:2 | LED MUX blabla | R-W |  | 00-L TOOL EX,  01-L LED Strip,  10-R Tool Ex,  11-R LED Stirp,  100-WS LED Strip,  101-Robot ESTOP LED |

### FPGA ESTOP Status

Address: 0xE

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:8 | SPARE | R-W |  | Set to ‘0’ |
| 7 | ESTOP Btn2 (Robotic ws) STATUS (from NC push button) - Sticky | R-W |  | Sticky bit, set to ‘1’ by Button, can be cleared by S.W |
| 6 | ESTOP Btn2 (Robotic ws) STATUS (from NO push button) -Stick | R-W |  | Sticky bit, set to ‘1’ by Button, can be cleared by S.W |
| 5 | ESTOP Btn2 (Robotic ws) STATUS (from NC push button) | R-0 |  |  |
| 4 | ESTOP Btn2 (Robotic ws) STATUS (from NO push button) | R-O |  |  |
| 3 | ESTOP Btn1 (Robotic ws) STATUS (from NC push button) - Sticky | R-W |  | Sticky bit, set to ‘1’ by Button, can be cleared by S.W |
| 2 | ESTOP Btn1 (Robotic ws) STATUS (from NO push button) -Stick | R-W |  | Sticky bit, set to ‘1’ by Button, can be cleared by S.W |
| 1 | ESTOP Btn1 (Robotic ws) STATUS (from NC push button) | R-0 |  |  |
| 0 | ESTOP Btn1 (Robotic ws) STATUS (from NO push button) | R-O |  |  |

### FPGA ESTOP Activation

Address: 0xF

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31 | BYPASS ESTOP DIAG | R-W |  |  |
| 30:1 | SPARE | R-W |  | Set to ‘0’ |
| 0 | ESTOP Activation | R-W |  | Once set – only active for 0.1Sec. |

### FPGA ESTOP DIAGNOSTIC

Address: 0x10

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 30:16 | SPARE | R-W |  | Set to ‘0’ |
| 15:0 | ESTOP DIAGNOSTIC Activation | R-W |  | Set to 0xABCD for Closing Estop in Diagnostic mode ( along with bit 31 in ESTOP Activation register. |

### FPGA ESTOP OPEN

Address: 0x11

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:1 | SPARE | R-W |  | Set to ‘0’ |
| 0 | ESTOP OPEN | R-W |  | Set to ‘1’ to open. |

### FPGA DIAGNOSTIC LEDS

Address: 0x12

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:8 | SPARE | R-W |  | Set to ‘0’ |
| 7:0 | Diagnostic LEDs | R-W |  |  |

### FPGA Spare IO connector

Address: 0x13

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:22 | SPARE | R-W |  | Set to ‘0’ |
| 21 | SPARE 1 CONN SINGLE END 3 | R-W |  |  |
| 20 | SPARE 1 CONN SINGLE END 2 | R-W |  |  |
| 19 | SPARE 1 CONN SINGLE END 1 | R-W |  |  |
| 18 | SPARE 1 CONN SINGLE END 0 | R-W |  |  |
| 17 | SPARE 1 CONN ANALOG SW 2 | R-W |  |  |
| 16 | SPARE 1 CONN ANALOG SW 1 | R-W |  |  |
| 15 | SPARE 1 CONN ANALOG SW 0 | R-W |  |  |
| 14 | SPARE 1 CONN DIFF 3 | R-W |  |  |
| 13 | SPARE 1 CONN DIFF 2 | R-W |  |  |
| 12 | SPARE 1 CONN DIFF 1 | R-W |  |  |
| 11 | SPARE 1 CONN DIFF 0 | R-W |  |  |
| 10 | SPARE 1 CONN SINGLE END 3 | R-W |  |  |
| 9 | SPARE 1 CONN SINGLE END 2 | R-W |  |  |
| 8 | SPARE 1 CONN SINGLE END 1 | R-W |  |  |
| 7 | SPARE 1 CONN SINGLE END 0 | R-W |  |  |
| 6 | SPARE 1 CONN ANALOG SW 2 | R-W |  |  |
| 5 | SPARE 1 CONN ANALOG SW 1 | R-W |  |  |
| 4 | SPARE 1 CONN ANALOG SW 0 | R-W |  |  |
| 3 | SPARE 1 CONN DIFF 3 | R-W |  |  |
| 2 | SPARE 1 CONN DIFF 2 | R-W |  |  |
| 1 | SPARE 1 CONN DIFF 1 | R-W |  |  |
| 0 | SPARE 1 CONN DIFF 0 | R-W |  |  |



### FPGA Wheel Rod sensor

Address: 0x15

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:4 | SPARE | R-W |  | Set to ‘0’ |
| 3 | WHEEL ROD SENSOR 1 NC STATE | R-O | 1-PRESSED |  |
| 2 | WHEEL ROD SENSOR 1 NO STATE | R-O | 1-PRESSED |  |
| 1 | WHEEL ROD SENSOR 1 NC STATE | R-O | 1-PRESSED |  |
| 0 | WHEEL ROD SENSOR 1 NO STATE | R-O | 1-PRESSED |  |

### FPGA FAN 1 Tacho

Address: 0x16

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:14 | SPARE | R-W |  | Set to ‘0’ |
| 23:16 | FAN 1 READ NUMBER | R-O |  | Updated +1 at Fan tacho update |
| 15:0 | FAN 1 TACHO | R-O |  | Measured pulses per 0.2 Sec. |

Tacho input pulses are counter per 0.2Sec. register is updated every 0.2Sec, read number is update +1 for any Tacho update

### FPGA FAN 1 PWM

Address: 0x17

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:8 | SPARE | R-W |  | Set to ‘0’ |
| 7:0 | FAN 1 PWM | R-W |  | PWM Freq=1KHz |

PWM is 0-255 (0 = no PWM, 255=Full PWM 100%).

### FPGA FAN 2 Tacho

Address: 0x18

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:14 | SPARE | R-W |  | Set to ‘0’ |
| 23:16 | FAN 2 READ NUMBER | R-O |  | Updated +1 at Fan tacho update |
| 15:0 | FAN 2 TACHO | R-O |  | Measured pulses per 0.2 Sec. |

Tacho input pulses are counter per 0.2Sec. register is updated every 0.2Sec, read number is update +1 for any Tacho update

### FPGA FAN 2 PWM

Address: 0x19

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:8 | SPARE | R-W |  | Set to ‘0’ |
| 7:0 | FAN 2 PWM | R-W |  | PWM Freq=1KHz |

PWM is 0-255 (0 = no PWM, 255=Full PWM 100%).

### FPGA SYNC DELAY TIME

Address: 0x1A

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:16 | SPARE | R-W |  | Set to ‘0’ |
| 15:0 | FPGA\_SYNC\_DELAY\_TIME | R-W |  | Sync signal delay in uSec |

### FPGA SYNC TIME

Address: 0x1B

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Field | Type | Encoding\reset | Description |
| 31:16 | SPARE | R-W |  | Set to ‘0’ |
| 15:0 | FPGA\_SYNC\_TIME | R-W |  | Length of sync signal in uSec |