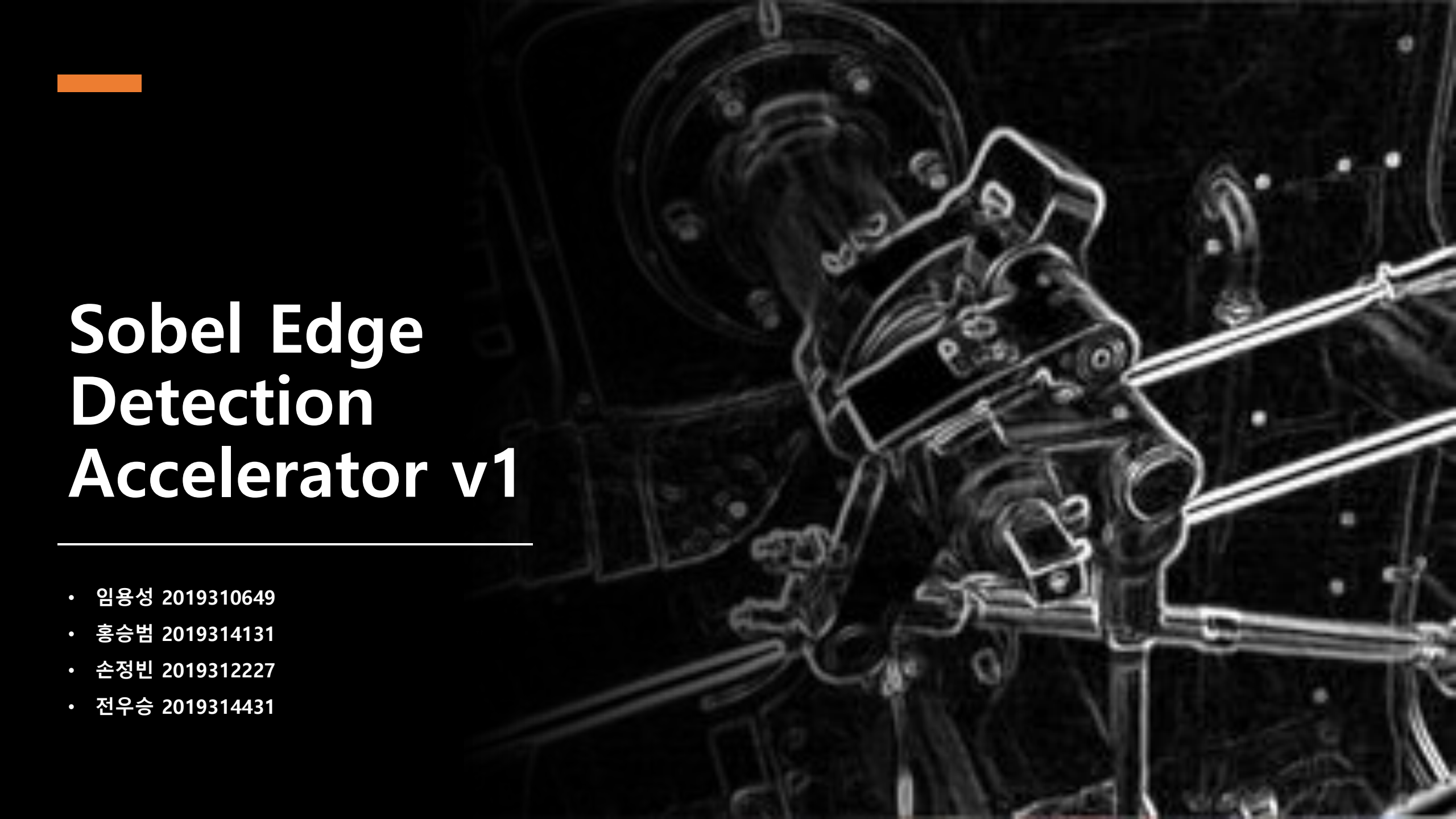
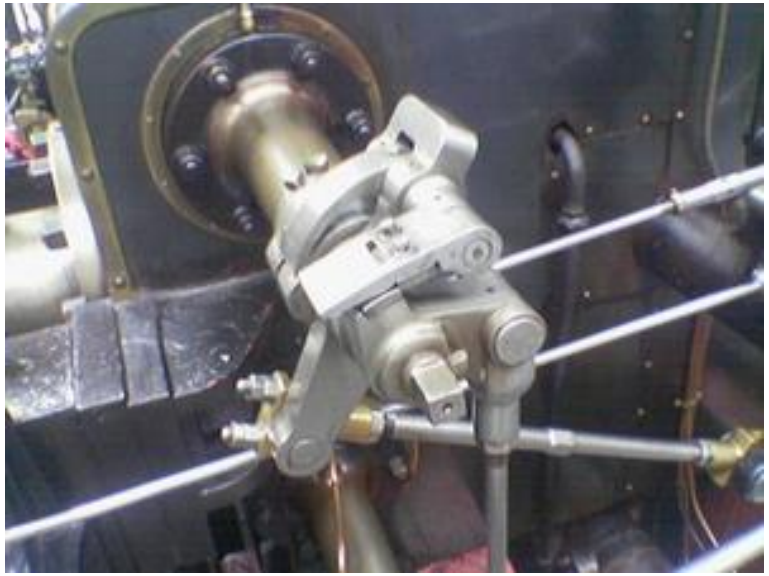
Sobel Edge Detection Accelerator v1



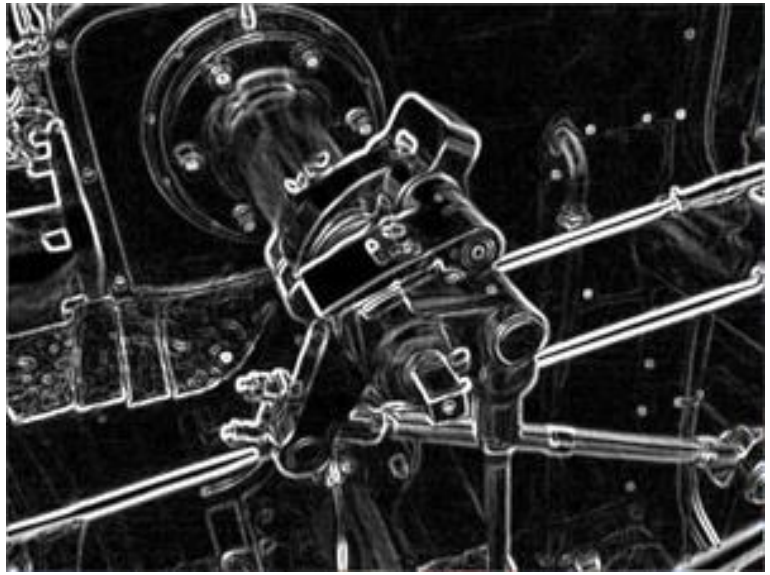
- 임용성 2019310649
- 홍승범 2019314131
- 손정빈 2019312227
- 전우승 2019314431

What is Sobel Edge Detection?



RGB

Matrix Operation

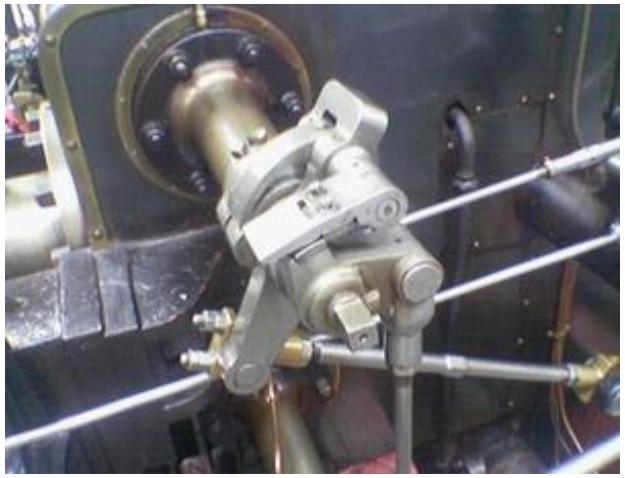


SOBEL

CORE

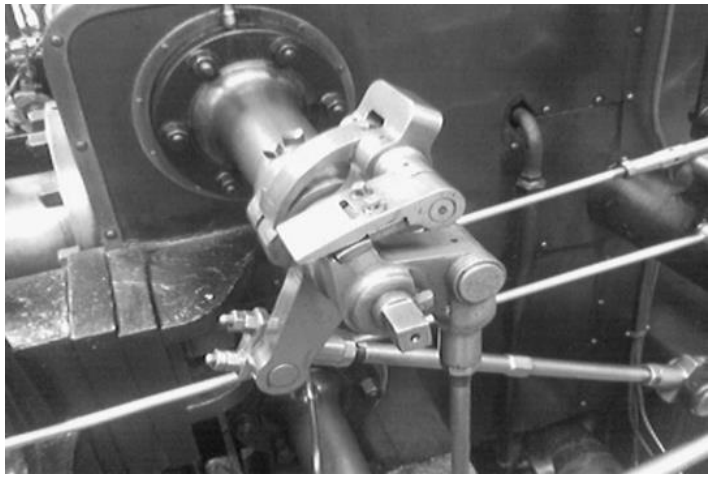
$$\mathbf{G}_x = \begin{bmatrix} +1 & 0 & -1 \\ +2 & 0 & -2 \\ +1 & 0 & -1 \end{bmatrix} * \mathbf{A} \quad \text{and} \quad \mathbf{G}_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix} * \mathbf{A}$$

How we Challenging this Problem?



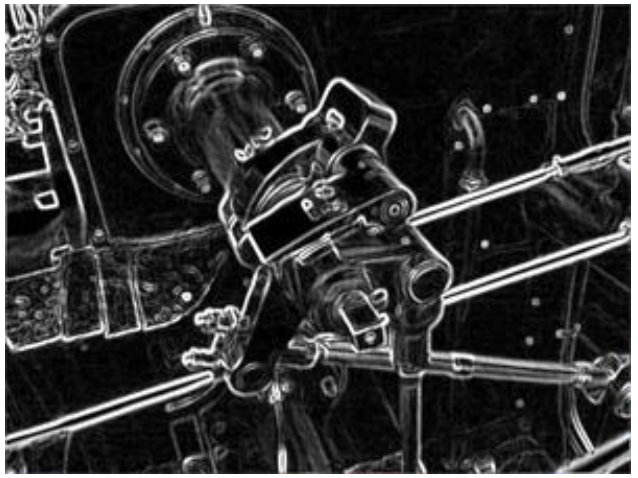
540 x 360 x 3(RGB) x 8bit
= 4,665,600 bits

SW



540 x 360 x 1(mono) x 8bit
= 1,555,200 bits

HW



540 x 360 x 8bit
= 1,555,200 bits

■ SW

SW 전처리를 통해
RGB → MONO로 바꿈으로써
연산량을 3배 줄임
→ Speed UP !

■ HW

FPGA를 사용하여 행렬 연산을 가속

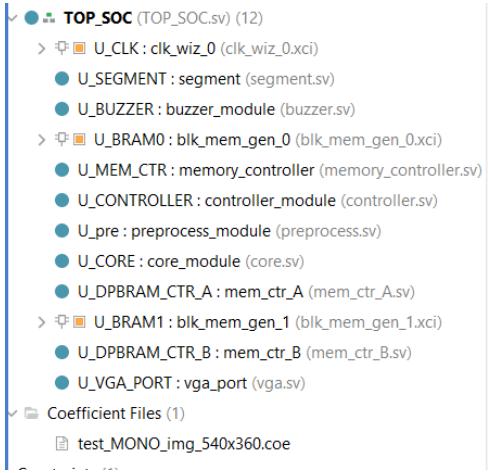
→ $\mathbf{G}_x = \begin{bmatrix} +1 & 0 & -1 \\ +2 & 0 & -2 \\ +1 & 0 & -1 \end{bmatrix} * \mathbf{A}$ and $\mathbf{G}_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix} * \mathbf{A}$

Brief Summary

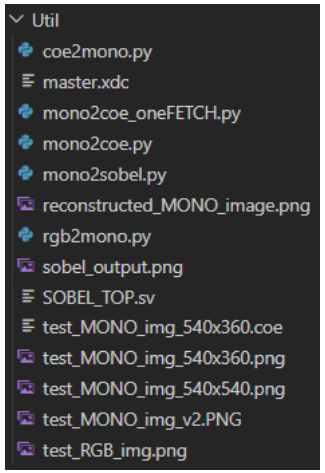
- **Hardware Using (Mandatory)**
  - LED
  - 7-Segment
  - Push Switch & DIP SW
  - Reset SW
  - Piezo Buzzer

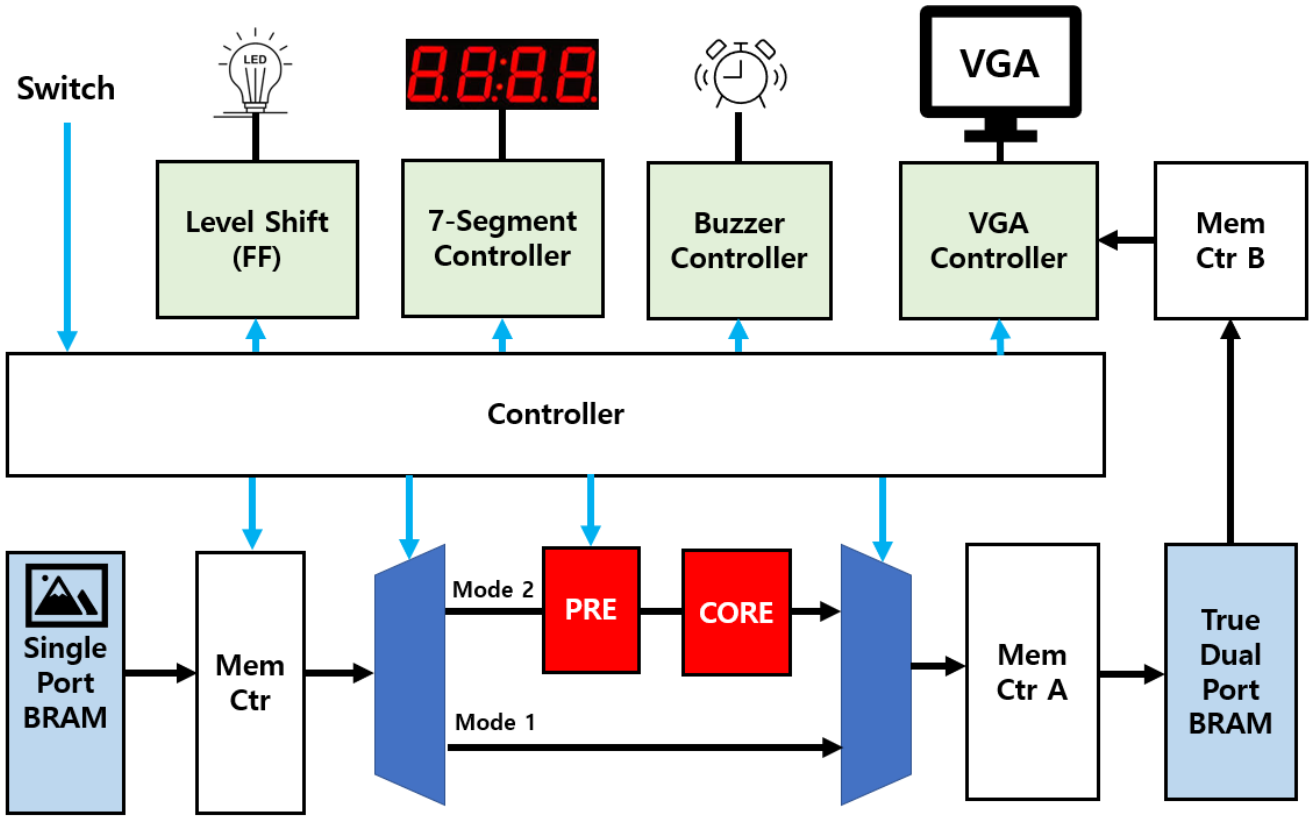
  (Additional)
  - VGA
  - BRAM
  - Clock Wizard

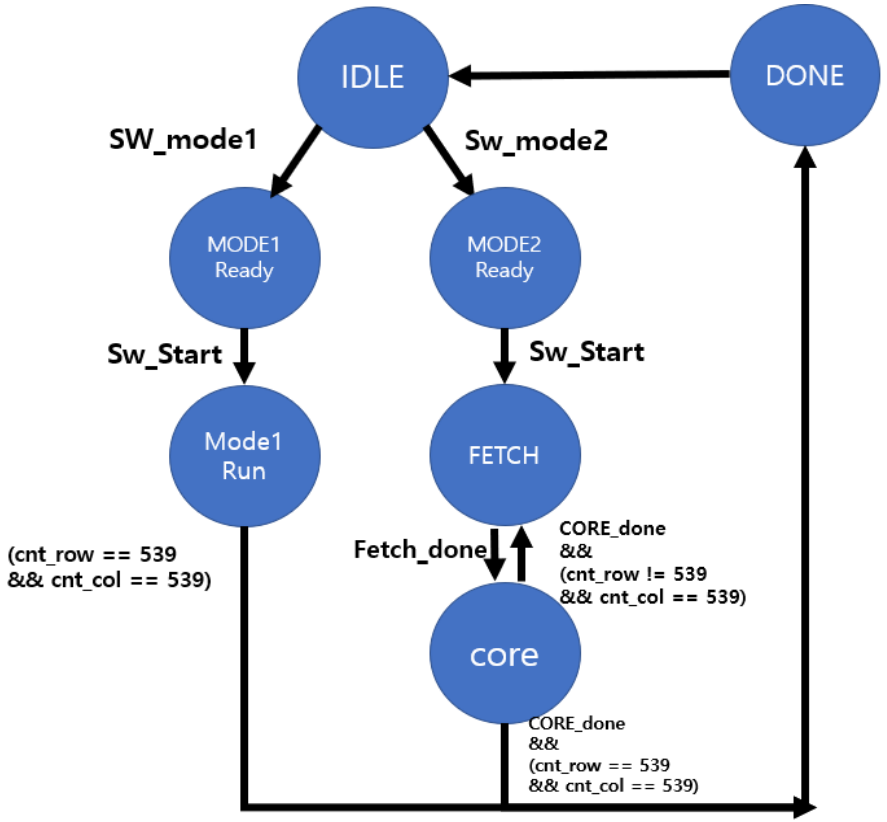
RTL & IP



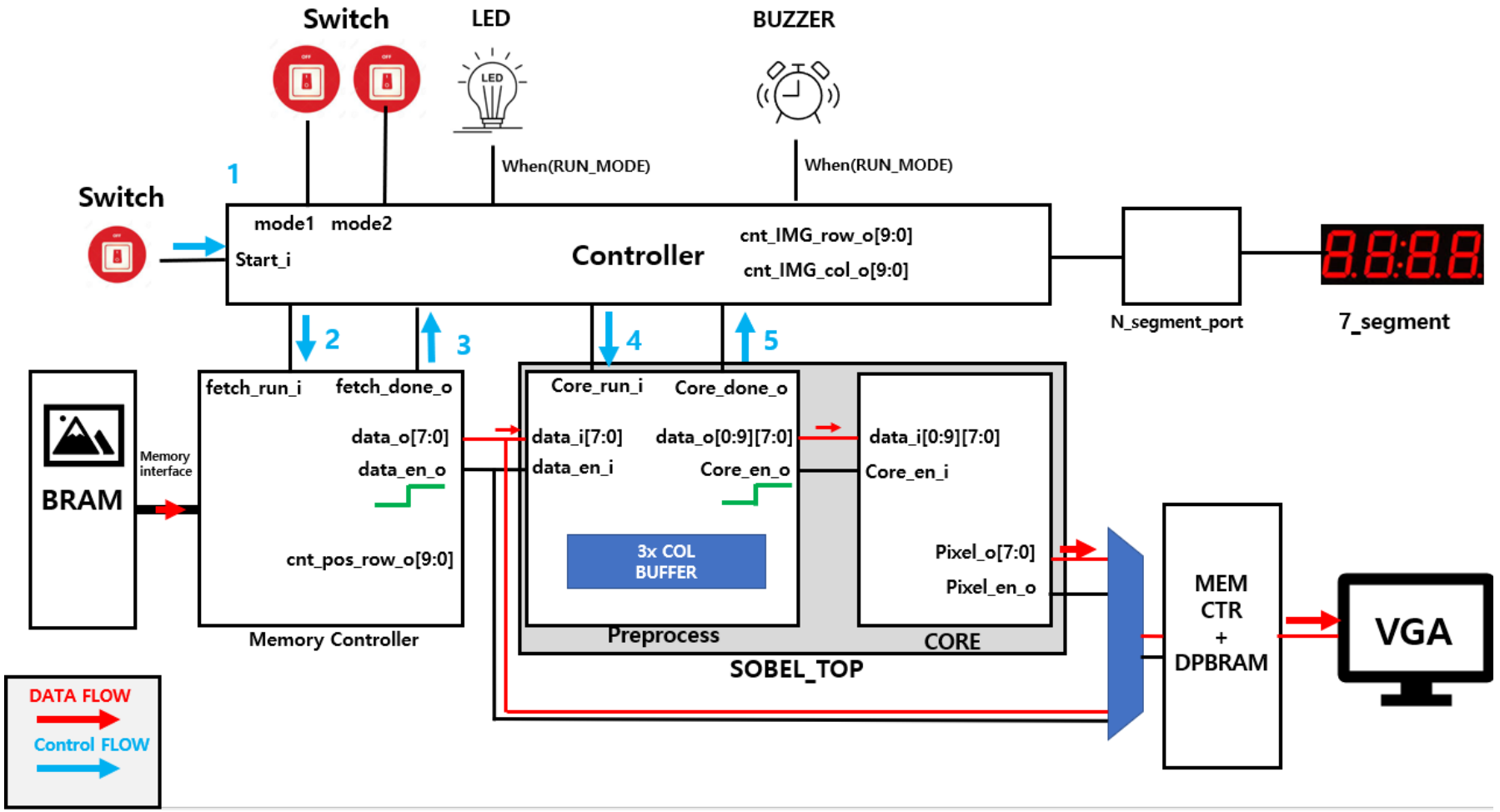
SW

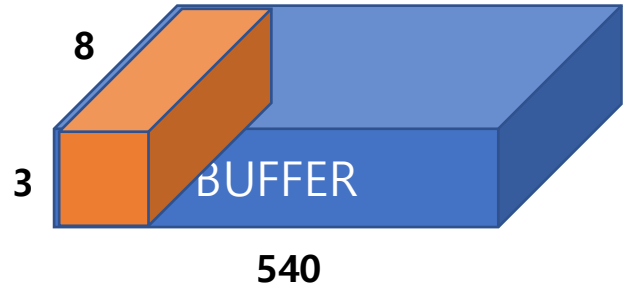


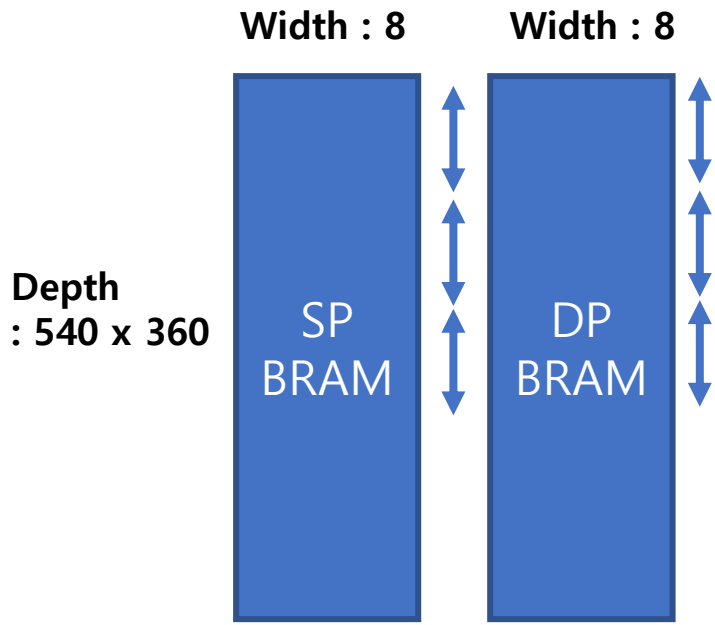




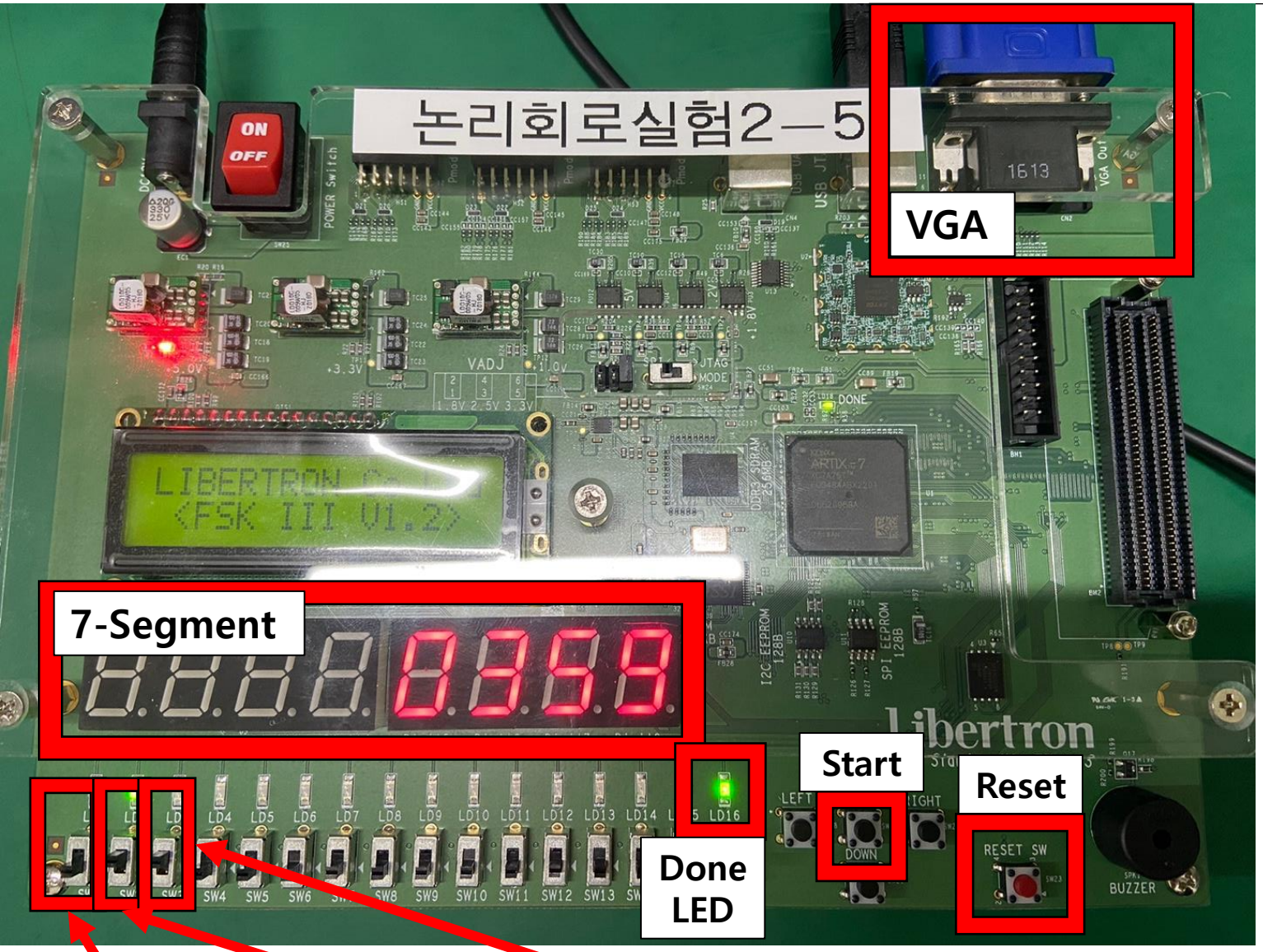
Key Point & Dataflow





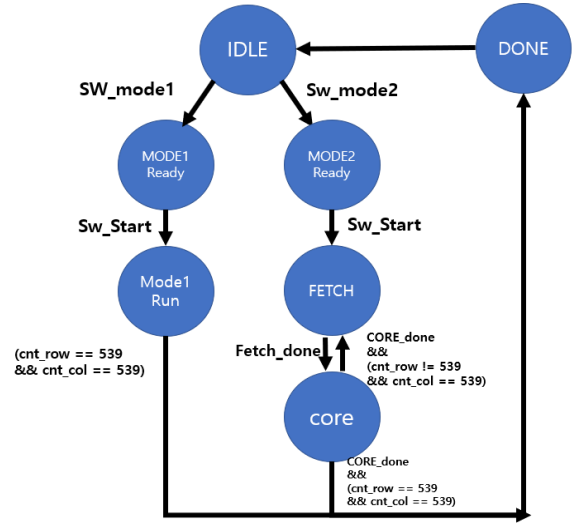


Brief Summary - Function



◆ **Function**

1. Switch 1(DIP) → Mode1 (Raw)
2. Switch 2(DIP) → Mode2 (Sobel)
3. Switch 3(DIP) → Buzzer Mode
4. Button (MID) → Start Signal
5. Reset SW → System Reset
6. DONE LED → At Done State
7. 7-Segment → # of Row which is processed
8. Buzzer → Up Tone at row up



Result – Area

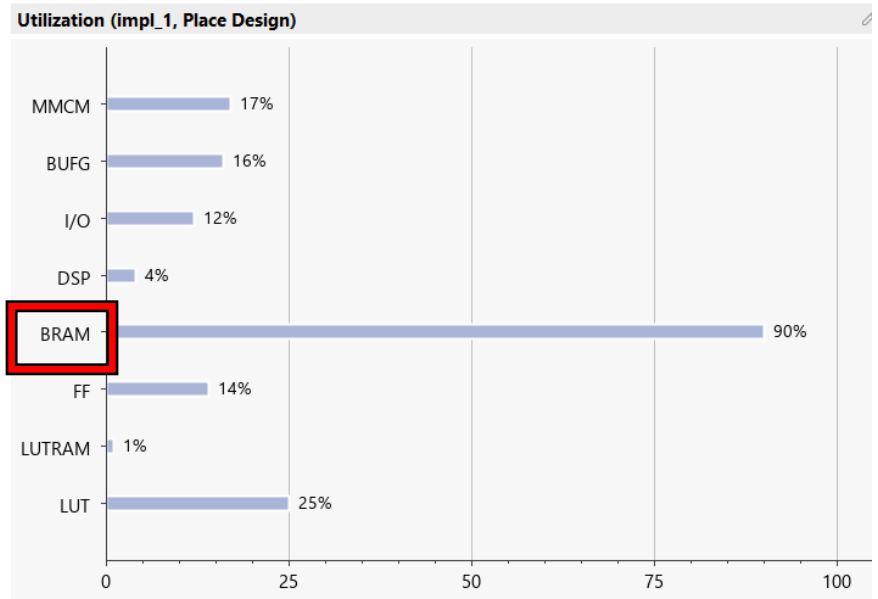
◆ **Board Name**
- xc7a75tfgg484-1

◆ **Board Resource Limit**
- Logic Cell : 75.520
- BRAM : 105KB

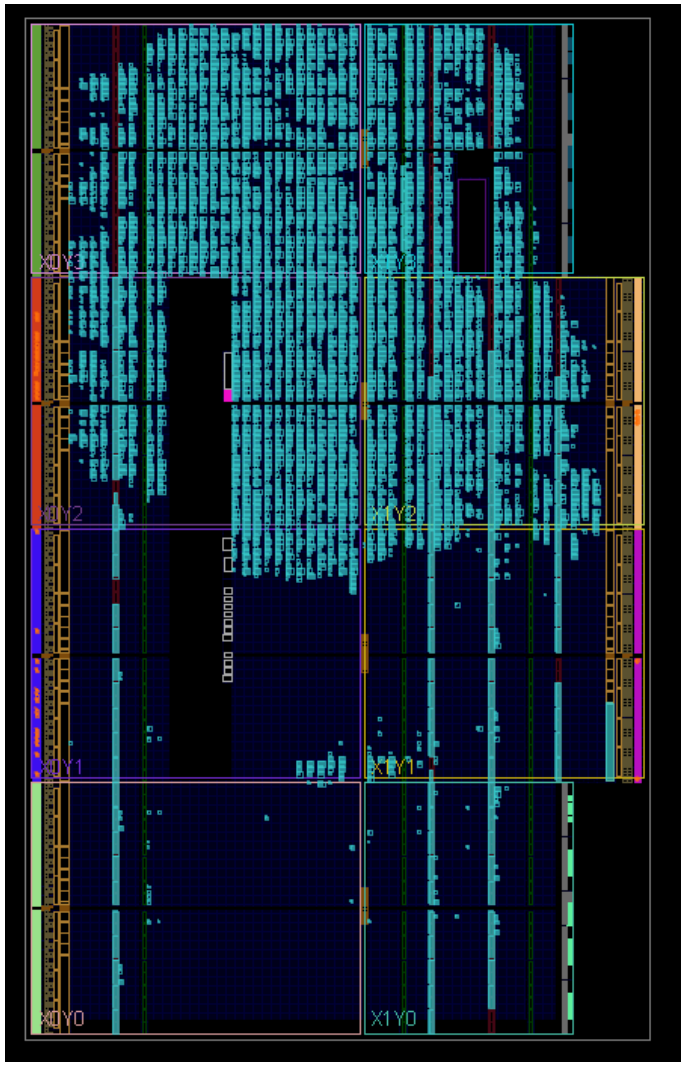
◆ **Utilization**
- BRAM : 90%
- LUT : 25.28%
- FF : 14.33%

◆ **Resource**

Resource	Utilization	Available	Utilization %
LUT	11934	47200	25.28
LUTRAM	3	19000	0.02
FF	13532	94400	14.33
BRAM	95	105	90.48
DSP	7	180	3.89
IO	35	285	12.28
BUFG	5	32	15.63
MMCM	1	6	16.67

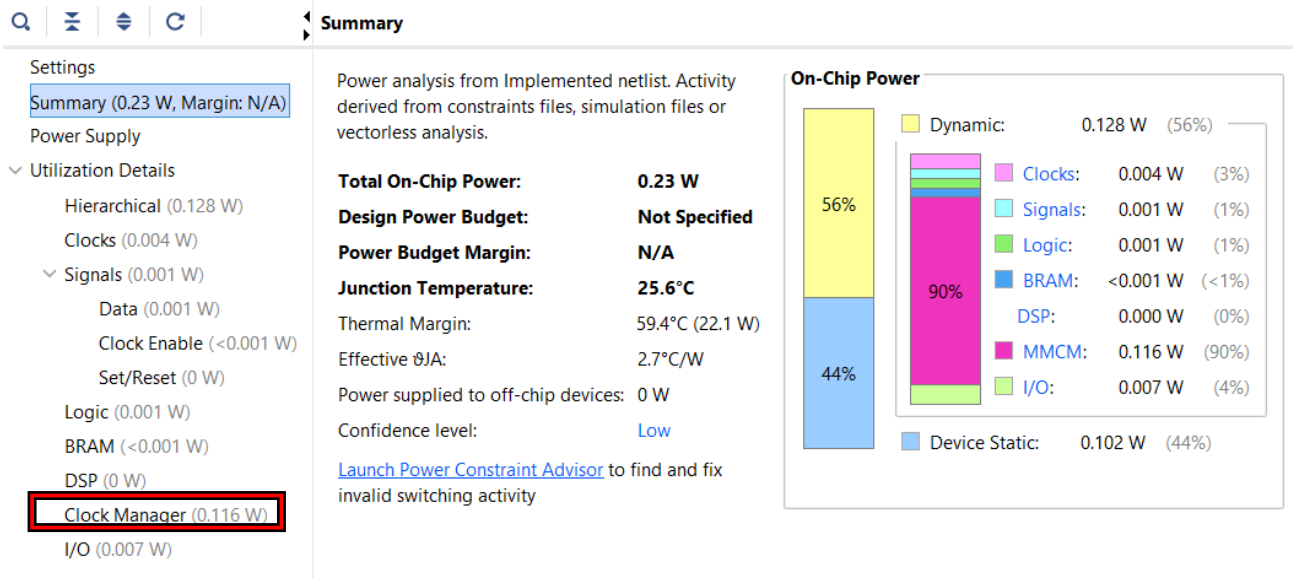


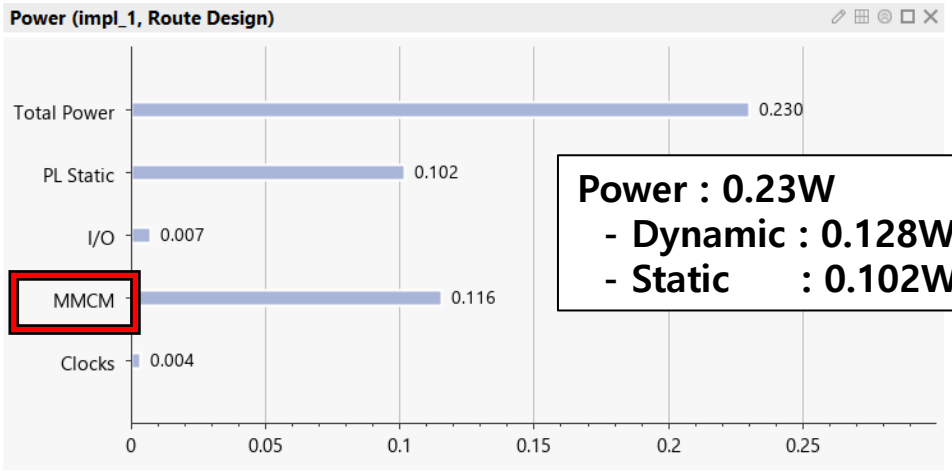
◆ **Area**



Result – Power & Timing

◆ Power





Power : 0.23W
- **Dynamic : 0.128W (56%)**
- **Static : 0.102W (44%)**

◆ Timing

There is no Slack!

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.066 ns	Worst Hold Slack (WHS):	0.112 ns	Worst Pulse Width Slack (WPWS):	3.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1057	Total Number of Endpoints:	1057	Total Number of Endpoints:	251

All user specified timing constraints are met.

Result

Mode 1

Mode 2

◆ **Comment**

저희 팀의 주 목표는 Sobel Edge Operator 가속기를 설계하는 것이었습니다.
가시성을 위해서 Mode1을 후반부에 추가하였고, 5월 27일 이전까지 Mode1의 동작이 성공적으로 동작함을 확인하였으나, Version Update를 하면서, mode1이 오동작하는 문제가 발생했습니다.
하지만, 본래 목적인 Sobel 가속기 설계를 성공적으로 하였으므로, 이번 TermProject를 성공적으로 수행완료했습니다.

Thank you ☺

Q & A

◆ 역할 및 참여 내용

- 임용성
  1. Mem Ctr & Mem Ctr A & BRAM
  2. Preprocess
  3. TOP (Mode 1 , Mode 2)

- 홍승범
  1. 7-Segment
  2. Preprocess
  3. CORE

- 손정빈 :
  1. VGA Controller
  2. CORE
  3. Mem Ctr B

- 전우승 :
  1. Buzzer Controller
  2. Mem Ctr