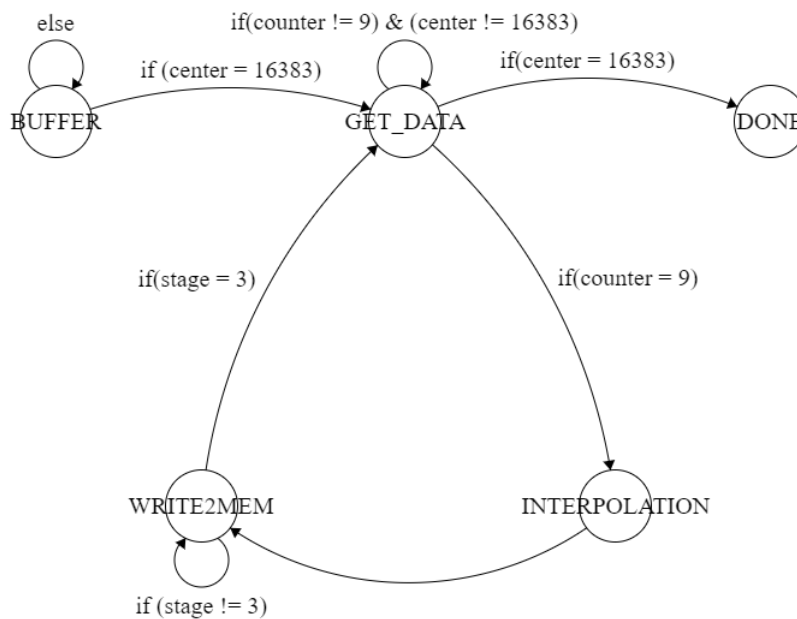
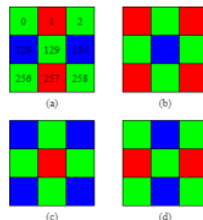


2023 Digital IC Design Homework 5

NAME	蘇勇達		
Student ID	N96114603		
Simulation Result			
Functional simulation	Completed	Gate-level simulation	Completed
<pre>VSIM 7> restart # ** Note: (vsim-12125) Error and warning message counts have been # Loading work.testfixture # Loading work.demosaic VSIM 8> run -all ***** # ** Simulation Start # ** ***** # ** Simulation completed successfully! # ** ***** # ** Note: \$finish : D:/DICdesign/HW5/file/testfixture.v(148) # Time: 10201500 ns Iteration: 1 Instance: /testfixture # 1 # Break in Module testfixture at D:/DICdesign/HW5/file/testfixture. VSIM 9> restart VSIM 10> run -all ***** # ** Simulation Start # ** ***** # ** Simulation completed successfully! # ** ***** # ** Note: \$finish : D:/DICdesign/HW5/file/testfixture.v(148) # Time: 10201500 ns Iteration: 1 Instance: /testfixture # 1 # Break in Module testfixture at D:/DICdesign/HW5/file/testfixture. VSIM 11> restart # Compile of demosaic.v was successful with warnings. # Compile of testfixture.v was successful. # 2 compiles, 0 failed with no errors. restart # ** Note: (vsim-12125) Error and warning message counts have been # Loading work.testfixture # Loading work.demosaic VSIM 12> run -all</pre>		<pre>ak key hit ak in Module testfixture at D:/DICdesign/HW5/file/testfixtur pile of testfixture.v was successful. pile of demosaic.vo was successful. ompile, 0 failed with no errors. 0> restart Note: (vsim-12125) Error and warning message counts have bee ding work.testfixture ding work.demosaic ding work.hard_block ` 2020.1 Compiler 2020.02 Feb 28 2020 ding instances from D:/DICdesign/HW5/file/demosaic_v.sdc ding instances from demosaic_v.sdo ding timing data from D:/DICdesign/HW5/file/demosaic_v.sdo ding timing data from demosaic_v.sdo Note: (vsim-3587) SDF Backannotation Successfully Completed. Time: 0 ps Iteration: 0 Instance: /testfixture File: D:/DI 1> run -all ***** # ** Simulation Start # ** ***** # ** Simulation completed successfully! # ** ***** # ** Note: \$finish : D:/DICdesign/HW5/file/testfixture.v(148) # Time: 10201500 ns Iteration: 1 Instance: /testfixture ak in Module testfixture at D:/DICdesign/HW5/file/testfixtur 2></pre>	
Evaluation Results			
test1.png	25.32	test2.png	24.82
test3.png	29.12	test4.png	20.95
test5.png	21.94	test6.png	25.21
Description of your design			



以上是這次作業所使用的 FSM 狀態，在一開始的 BUFFER，我將 data_in 的資料分別存入 R、G、B 三個 memory，儲存完資料後再進行資料的運算。在 GET_DATA 中，我要把要運算的資料讀出來才能做運算，所以這裡會花費掉較多的時間，而因為此次不需要處理邊界，所以我遇到邊界的 pixel 就會跳過。拿取完資料之後，我就進入 INTERPOLATION 做運算，按照題目說明，此次只會有四種狀況產生：



所以在這邊我就分成四種狀況來做運算。在完成運算之後，我就把運算完的 pixel R、G、B 寫回 memory 裡面，之後回到 GET_DATA 的狀態。假如全部的資料都運算完成，跳到 DONE 狀態，程式結束。

Scoring = average PSNR of the six test images

*** PSNR of all interpolation results should meet at least the baseline.**