Hardware Realization of a MASH-111 $\Delta\Sigma$ Modulator

Group 14 — **Members:** Yanghonghui Chen, Xuancheng Liu

Design Performance & Architecture

The design was synthesized using the TSMC 16nm CMOS library. A multi-corner strategy (SS/125°C for Setup, FF/-40°C for Hold) ensures robustness. Power is verified via PrimeTime sign-off.

Metric	Value
Clock Freq.	500 MHz (2.0 ns)
Total Area	176.62 μm^2
Power (DC)	0.192 mW
Power (PT)	**0.178 mW**
Hold Slack	0.00 ns (MET)
Setup Slack	1.16 ns (MET)

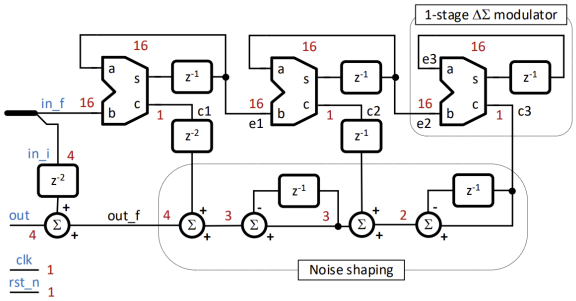

Figure 1: MASH-111 Top-Level Diagram.

Key Features of the Design

- **MASH-1-1-1 Architecture:** Implemented a Multi-stAge noise SHaping modulator by cascading three 1st-order accumulators. This structure effectively randomizes quantization noise while maintaining unconditional stability.
- **Robust Noise Shaping Logic:** Utilized a cascaded differentiation network ($(1-z^{-1})^3$) to push quantization noise to high frequencies. The logic handles 1-bit carry signals using signed arithmetic with bit-extension to accommodate the dynamic range of -3 to +4.
- **High-Speed Pipelining:** Designed with critical path alignment using z^{-1} and z^{-2} registers to strictly meet the 500 MHz constraint. The large Setup Time slack (1.16 ns) indicates a highly efficient datapath capable of exceeding the target frequency.
- **Multi-Corner Optimization:** Validated against extreme corners. The synthesis flow successfully closed timing in the Slow-Slow corner (worst-case delay) while preventing hold violations in the Fast-Fast corner.
- **Automated Hold Fixing:** To address the fast signal propagation inherent in the 16nm process, the synthesis tool automatically inserted 94 buffer/inverter cells, achieving a passing Hold Slack of 0.00 ns without compromising system performance.