Principles and Design of IoT Systems (2022-23)

December 8, 2023

Abstract

Human Activity Recognition is a complex field of study focusing upon recognising human motion. This paper outlines the creation of a wearable sensor-based approach the Human Activity Recognition problem. Multiple machine learning models capable of distinguishing between 14 different kinds of ambulation activities are created with a quantitative analysis being conducted to evaluate the most successful model. The design process behind the creation of an accompanying Android mobile application is discussed. A reflection on the quality of the system is provided alongside suggestions for improvements to similar systems in the future.

Contents

1 Glossary

BOM Bill of Material.
CIFB Cascaded Integrator with Feedback Paths.
CIFF Cascaded Integrator with Feedforward Paths.
CRFB Cascaded Resonator with Feedback Paths.
CRFF Cascaded Resonator with Feedforward Paths.
DAC Digital to Analogue Converter.
DWA Data Weighted Averaging.
FFT Fast Fourier Transform.
MASH Multi-stage Noise Shaping.
MSA Maximum Stable Input Amplitude.
NTF Noise Transfer Function.
OSR Oversampling Ratio.
PSD Power Spectral Density.
S-MASH Sturdy Multi-stage Noise Shaping.
SQNR Signal to Quantization Noise Ratio.
THD Total Harmonic Distortion.
Chapter 1

2 Introduction

2.1 Project Overview

This project aims to design a delta-sigma analogue to digital converters to realize the specific design requirements. The design specifications of the delta-sigma modulator are decided to achieve good performance for an audio product. At the start stage, a Cascade Integrator with Feedforward Path(CIFF) modulator is used to find the most suitable modulator parameters, such as modulator Order, Oversampling Ratio(OSR) and Quantizer bits. Then discussions among different modulator architectures are presented. The modulator design specifications are achieved by using different design techniques, such as Noise Transfer Function(NTF optimization, Dynamic Element Matching(DEM), adding dither and so on. After finishing the design work, comprehensive verification notes are presented to check the modulator performance at different conditions(finite integrator gain, coefficient mismatch, DAC nonlinearity and so on).

2.2 Report Outline

This report starts by describing the design considerations on choosing the modulator parameters and the trade-offs between them in Chapter 2. The following chapter presents the modulator verification notes. A detailed verification matrix that includes all the extreme simulation conditions are given to justify the modulator has a robust performance. Chapter 4 presents the potential advantages of the Sturdy multi-stage noise shaping S-MASH modulator and the practical implementation challenges. The final chapter summarizes the project achievement and future development.
Chapter 2

3 Modulator Design Consideration

3.1 Design Specifications and Initial Assumption

Design an audio band ADC with the following specifications over 20 Hz to 20KHz.
- Maximum stable input amplitude at least $\pm 0.85 for a full-scale input range \pm 1$.
- Signal to quantisation noise ratio at MSA at least 105 dB.
- Total harmonic distortion at input level 1dB below MSA less than -90 dB.
- No audio band limit cycles or tones exceeding the quantisation noise power.

To start with the design, the first task is to choose appropriate modulator parameters, such as modulator order, oversampling ratio and quantizer bit to achieve the design specifications. The theoretically estimated peak SQNR equation can be used at the start point.

$$SQNR = 6.02N + 1.76 + (20L+10)\log_{10}(OSR) - 10\log_{10}\left(\frac{\pi^{2L}}{2L+1}\right) 1$$

where L is modulator order OSR is the oversampling ratio, N is the bits number of the quantizer.

By using Equation 2.1 and SQNR estimation graphs[1] in the Appendix, initial assumptions could be made and checked. The detail justifications on the initial parameters choosing are presented in Table 2.1

3.2 Modulator Parameters Selection

There are five most common modulator architectures for designing a delta-sigma analogue to digital converter.

- Cascade Integrators with Feedback Path(CIFB)
- Cascade Integrators with Feedforward Path(CIFF)
- Cascade Resonators with Feedback Path(CRFB)
- Cascade Resonators with Feedforward Path(CRFF)
- $2+1$ Multi-stage Noise Shaping (MASH) converters

The CIFB and CIFF modulators only use delaying integrator for all the stages, while CRFB and CRFF modulators use both delaying and non-delaying integrators. To realise a non-delaying integrator, the design requirement of an amplifier in the analogue domain is much higher than a delaying integrator. Because the amplifier of a non-delaying integrator needs higher SlewRate and Bandwidth. [2] Therefore, CIFB and CIFF modulators are considered to reduce the complexity of integrator design. Besides, $2+1$ MASH modulator is also considered as one of the potential design solution.

3.2.1 Modulator Order and Oversampling Ratio(OSR)

To achieve a high SQNR (105dB) at MSA it is prefered to use a high order modulator L $= 2, 3$ or 4 without using an extremely high OSR High OSR improves the performance of SQNR but the power consumption also increases. Therefore, the trade-off between OSR and power consumption needs to be taken into consideration. Similarly, a high-order modulator means more complicated circuit design and more area consumption. Hence, a modulator with order L $= 2$ or 3 or 4 and OSR $= 64$ or 128 are considered in this project.

3.2.2 Quantizer Bits

The modulator quantizer bits determine the maximum stable input range(MSA) and peak SQNR A modulator with multi-bits feedback could achieve a high peak SQNR as the loop is stable for larger input signals. Besides, the design requirement of the input op-amp of the loop filter is eased as the loop error reduced. However, a multi-bits feedback loop requires the same number bits DAC, hence the non-linearity of DAC is a potential issue. Therefore, a modulator with quantizer bits N $= 2$ or 3 is considered in this project.

3.2.3 Simulation Set-up

For choosing the input signal frequency, it is noticed that the frequency corresponds exactly to one of the frequency points in the calculated FFT spectrum is necessary to obtain an accurate result.

For instance, choosing OSR $= 128$ to obtain a sampling frequency fs $= 128 \times 2 \times 24$kHz $= 6.144$MHz.

$$f_{sine} = \frac{N \times f_{sampling}}{N_S} 3$$

where N is an arbitrary integer, f_{sine} is the test frequency, N_S is the number of samples used in the FFT. In order to check the modulator output spectral density at 20 Hz, a big $N_S = 65536$ is chosen. If choose N $= 40$, then $f_{sine} = 3750$ Hz.

Table 2.1 takes CIFF modulator as an example to test the most suitable modulator parameters.

Table 2.1: CIFF modulator parameters justification table.

Modulator Order	MSA	SQNR at MSA	THD	Tones in audio band
2	0.89	84.5	-91.52	Yes
3	0.89	127.6	-137.67	Yes
4	0.89	147.4	-146.27	Yes
![](https://cdn.mathpix.com/cropped/2023_04_02_7dfea647590134309876g-08.jpg?height=62&width=1612&top_lef				
OSR	MSA	SQNR at MSA	THD	Harmonics in audio band
64	0.89	105.9	-114.77	Yes
128	0.89	127.6	-137.67	Yes
CIFF modulator performance at different Quantizer bits when Order = 3, OSR = 128				
Quantizer Bits	MSA	SQNR at MSA	THD	Harmonics in audio band
2	0.89	107	-112.47	Yes
3	0.89	127.6	-137.67	Yes
CIFF modulator performance with/without dither when Order = 3, OSR = 128, Quantizer bits =				
Dither	MSA	SQNR at MSA	THD	Harmonics in audio band
0.1	0.89	123.2	-148.21	No tones
0.2	0.89	121.3	-149.16	No tones

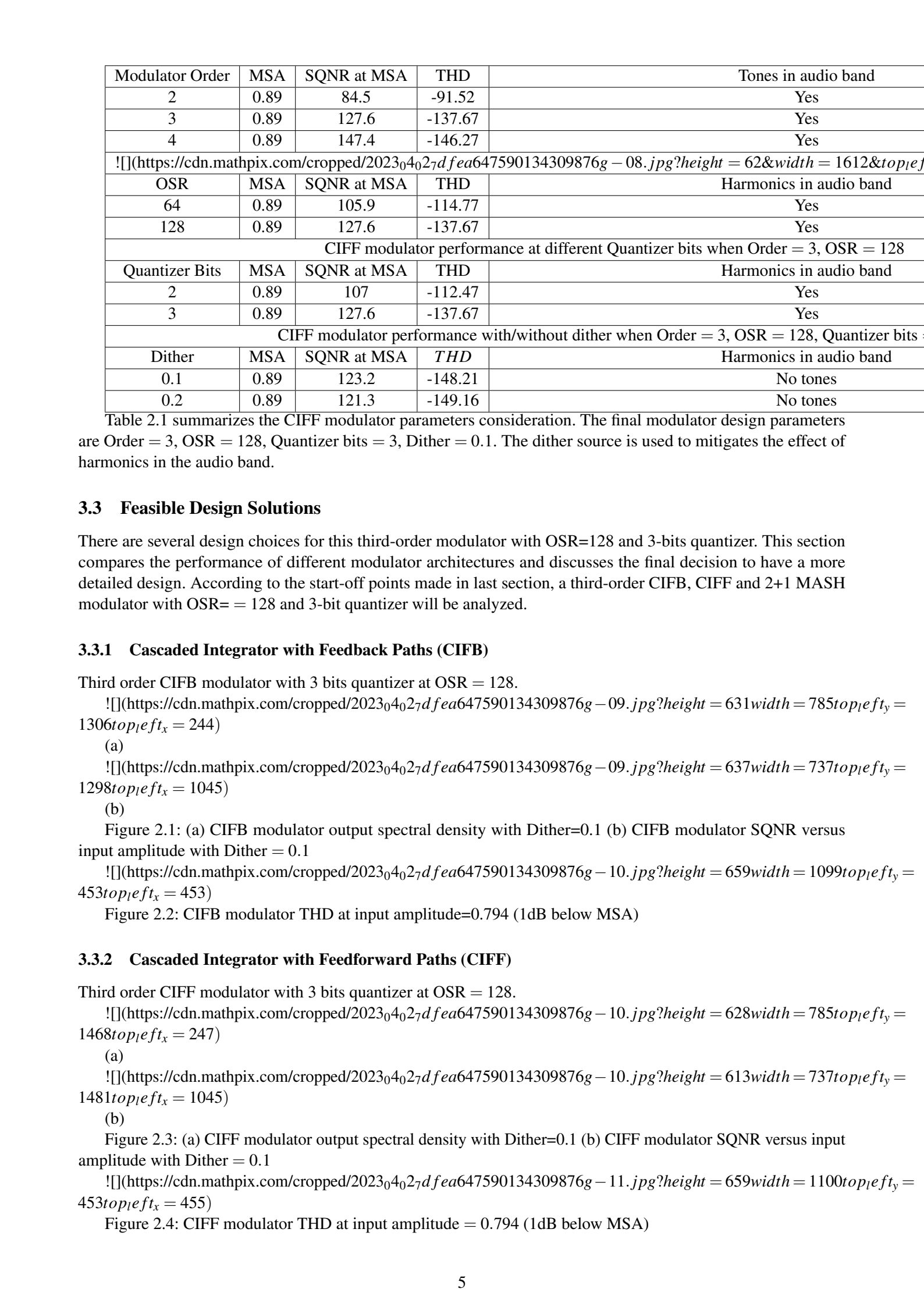
Table 2.1 summarizes the CIFF modulator parameters consideration. The final modulator design parameters are Order = 3, OSR = 128, Quantizer bits = 3, Dither = 0.1. The dither source is used to mitigates the effect of harmonics in the audio band.

3.3 Feasible Design Solutions

There are several design choices for this third-order modulator with OSR=128 and 3-bits quantizer. This section compares the performance of different modulator architectures and discusses the final decision to have a more detailed design. According to the start-off points made in last section, a third-order CIFB, CIFF and 2+1 MASH modulator with OSR= = 128 and 3-bit quantizer will be analyzed.

3.3.1 Cascaded Integrator with Feedback Paths (CIFB)

Third order CIFB modulator with 3 bits quantizer at OSR = 128.



(a)

(b)

Figure 2.1: (a) CIFB modulator output spectral density with Dither=0.1 (b) CIFB modulator SQNR versus input amplitude with Dither = 0.1

Figure 2.2: CIFB modulator THD at input amplitude=0.794 (1dB below MSA)

3.3.2 Cascaded Integrator with Feedforward Paths (CIFF)

Third order CIFF modulator with 3 bits quantizer at OSR = 128.

(a)

(b)

Figure 2.3: (a) CIFF modulator output spectral density with Dither=0.1 (b) CIFF modulator SQNR versus input amplitude with Dither = 0.1

Figure 2.4: CIFF modulator THD at input amplitude = 0.794 (1dB below MSA)

3.3.3 2+1 Multi-stage Noise Shaping(MASH) Converters

(a)

(b)

Figure 2.5: (a) 2+1 MASH modulator output spectral density with Dither=0.1 (b) 2+1 MASH modulator SQNR versus input amplitude with Dither $= 0.1$

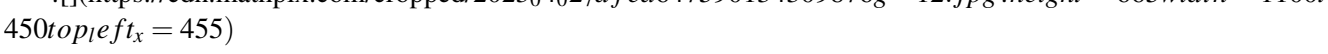


Figure 2.6: $2+1$ MASH modulator THD at input amplitude=0.794 (1dB below MSA)

3.4 Modulator Architecture Comparison

Last section shows the simulation results of three types of modulator. Table 2.2 summarizes their performance in terms of the design specifications.

Table 2.2: Modulator architecture comparison according to design specifications

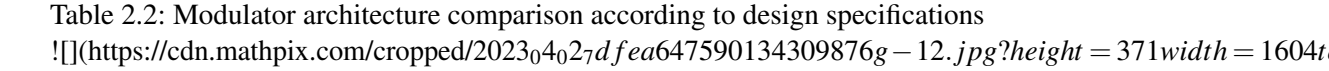


Table 2.2 indicates that all three modulators can achieve the main design specifications. The $2+1$ MASH modulator has a higher design requirement on the analogue building blocks to mitigate the effect of path mismatch between the NTF and STF. Digital filter in MASH modulator could be very difficult to design because it needs to match with the complex analogue transfer functions. Besides, the quantisation noise in the preceding loop has a possible leak to the output directly. (H_1 in Figure A.4 in Appendix.) Therefore, to relax the constrain of digital filter design, this project is not going to use a MASH modulator. Compare to CIFB, CIFF has the advantage of using only one feedback DAC, Also, CIFF is known as a low-distortion architecture [2], as the summing amplifier (shown in Figure 2.7) sums the input signal and all the integrators output to the quantizer. However, needing this extra amplifier is also one of the drawback of CIFF modulator. Overall, CIFF modulator is chosen for this project.

3.5 CIFF Modulator Schematic

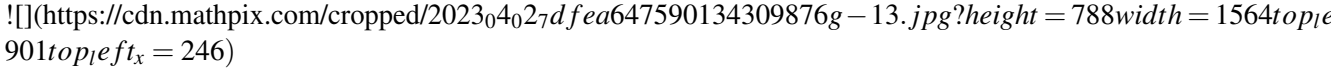


Figure 2.7: Third order CIFF modulator schematic.

3.6 Conclusion

This chapter starts by calculating the appropriate modulator parameters, such as Order, OSR and quantizer bits. Then a set of simulations for CIFF modulator are run to check the modulator performance at different design parameters. A third-order modulator with OSR $= 128$ and quantizer bits N $= 3$ are chosen to realize all the design requirements. After obtaining the design parameters, three modulator architectures(CIFB, CIFF and 2+1 MASH) are checked to find the most suitable one for this project in terms of all the design trade-offs. The project finally decides to use a third-order CIFF modulator with OSR $= 128$ and quantizer bits N $= 3$.

4 Chapter 3

5 CIFF Modulator Implementation

Chapter 2 discussed the possible design solutions for this audio band analogue to digital converter. A CIFF modulator is selected to achieve the design tasks. This chapter will describe the design details and the verification notes of CIFF modulator. The key design parameter will be justified in each section and a full verification notes is given at the end.

5.1 NTF Zeros Optimization

The modulator NTF transfer function could be optimized by using the delta-sigma toolbox. The new modulator NTF expression is shown below.

$$NTF = \frac{(z-1)\left(z^2-2z+1\right)}{(z-0.6693)\left(z^2-1.531z+0.6638\right)}$$

Figure 3.1 shows the modulator pole-zero plot with NTF optimization and the Bode plots comparison with and without using NTF optimization. An estimation of zero frequencies is shown below. The estimated zero frequency is aligned with the notch point from the modulator PSD spectrum(as shown in Figure 2.3(a)).

$$Theta(\theta) = \arctan\frac{0.0190103}{0.999819} = 1.0893^{\circ} f_{Zero} = \frac{\theta}{180} \times \frac{fs}{2} = \frac{1.0893}{180} \times \frac{6.144 \times 10^6}{2} = 15.98kHz$$

(a)

(b)

Figure 3.1: (a)Modulator Pole-Zero plot with NTF optimization. (b)Modulator Bode plots comparison with and without NTF optimization.

5.2 Modulator Verification

This section will give a detailed verification notes on the modulator performance at different simulation conditions. Table 3.1 gives the MSA value of this modulator.

Table 3.1: CIFF modulator test with different input signal amplitude.

Sine-wave amplitude(sinamp)	0.89	0.91	0.93(MSA)	0.95	Pass/Fail
SQNR	123.2	122.9	122.3	106.5	Pass
THD at 1dB below sinamp	-148.21	-135.02	-131.72	-119.97	Pass

5.2.1 Tolerance of Finite DC Integrator Gain

In the real analogue world, the integrator amplifier gain is not infinite. The finite amplifier DC gain will bring some non-ideal effect on the modulator performance. Table 3.2 shows the dead zone, SQNR and THD behaviours at finite DC integrator gain. Table 3.2: CIFF modulator dead zone, SQNR and THD performance with different finite integrator DC gain. Each integrator in this modulator has the same DC gain.

Finite DC integrator gain					
DC Gain(Gain of each integrator)	Infinite	100	50	25	10
Dead zone width	no	no	no	no	no
SQNR at MSA	123.2	113.2	106.3	94.4	76
THD at 1dB below MSA	-148.21	-134.16	-123.15	-107.4	-93.668

There is no dead zone for this modulator unless the integrator gain is smaller than 5, which typically won't happen in the real circuit design. Figure 3.2 shows the CIFF modulator output spectrum at different integrator gain.

Figure 3.2: CIFF modulator output spectrum at different integrator gain.

Amplifier finite gain causes a shift in the NTF zeros from z = 1 to a point inside the unit circle. [4] The noise floor increases when the integrator gain is not high enough.(as shown in Figure 3.2). The integrator with finite gain behaves like a low-pass filter and limits the modulator noise-shaping capability at low frequency. An integrator with a gain of 100 is normally easy to achieve in the analogue domain. So for the rest of the modulator verification work, the gain of each integrator is set to 100. For a real circuit design, the amplifier open-loop gain should be[4]

$$A_0 >> \frac{OSR}{\pi} - 2 >> \frac{128}{\pi} - 2 >> 38.74$$

5.2.2 Tonal Behaviour for Sweeping DC Input

Modulator behaviour with DC input is justified by checking the output spectrum and quantization noise power versus full range DC input level.

(a)

(b)

Figure 3.3: (a)Modulator output spectrum with rational DC inputs (b)Modulator output spectrum with irrational DC inputs

(a)

(b)

Figure 3.4: (a)Modulator in-band quantization noise power versus full range DC input level. (b)Modulator in-band quantization noise power versus DC input level within MSA. Figure 3.3 shows the modulator output spectrum with rational and irrational DC inputs. There are no spurious tones appear when testing different DC input level. Figure 3.4 presents the modulator in-band quantization noise power versus full range DC input level. There are no tones when DC input level smaller than 0.93. The base band power increases when the DC input is higher than the maximum stable input range.

5.2.3 Integrator Outputs Dynamic Range Scaling

The integrator output dynamic range scaling is tested by applying a sine signal with amplitude $= 0.9$. Figure 3.5 indicates that the modulator internal signals are all scaled in the range of ± 1 V

Figure 3.5: Modulator internal signals plots in time domain.

5.2.4 Coefficient Mismatch and Variation

The coefficients for different building blocks of the CIFF modulator is calculated by the Delta Sigma Toolbox. The values of all the coefficients are listed below. Coefficients refer back to Figure 2.7(CIFF modulator schematic)

- a represents feedforward summation coefficients. $\mathrm{a}(1) = 2.0686, \mathrm{a}(2) = 1.5509, \mathrm{a}(3) = 0.99521$.
- b represents feedforward path coefficients from input to the integrators.

$b(1) = 0.38669, b(2) = 0, b(3) = 0, b(4) = 1$ - c represents forward path coefficients between integrators.

$c(1) = 0.38669, c(2) = 48004, c(3) = 0.23665$

- g represents resonator coefficients. $\mathrm{g}(1) = 0.0015271$

The variation of $\mathbf{a}, \mathbf{b}$ and $\mathbf{c}$ in a real design could up to 2%, while $\mathbf{g}$ could vary up to 50% as the absolute value of it is very small.

Table 3.3: Modulator coefficient mismatch/variation effect on SQNR and THD.

Variation of **a**				
Coefficient variation	$0.5\%/-0.5\%$	$1\%/-1\%$	$2\%/-2\%$	Pass/Fail
SQNR at MSA	$123.6/123.1$	$124.1/122.4$	$124.7/121.7$	Pass
THD at 1 dB below MSA	$-140.8/-140.5$	$-141.7/-141.5$	$-141.4/-141.3$	Pass
Variation of **b**				
Coefficient variation	$0.5\%/-0.5\%$	$1\%/-1\%$	$2\%/-2\%$	Pass/Fail
SQNR at MSA	$122.4/123.2$	$121.6/122.3$	$122.1/121.8$	Pass
THD at 1 dB below MSA	$-142.8/-143.5$	$-143.4/-144.1$	$-141.4/-141.4$	Pass
Variation of **c**				
Coefficient variation	$0.5\%/-0.5\%$	$1\%/-1\%$	$2\%/-2\%$	Pass/Fail
SQNR at MSA	123.9/121.7	$124.2/122.3$	$125.4/123.4$	Pass
THD at 1 dB below MSA	$-140.3/-140.9$	$-143.7/-143.2$	$-148/-147.3$	Pass
Variation of g				.
Coefficient variation	$5\%/-5\%$	$20\%/-20\%$	$50\%/-50\%$	Pass/Fail
SQNR at MSA	$122.8/109.8$	$122.6/108.7$	$119.6/107.5$	Pass
THD at 1 dB below MSA	$-142.1/-142.3$	$-141.8/-141.3$	$-134.5/-138.4$	Pass

5.2.5 DAC Element Mismatch

The effect of DAC nonlinearity could seriously affect the modulator output. Both the signal and shaped noise distorted in this situation(poor noise shaping and more harmonic tones in the bandwidth of interest). The signals intermodulation also has a bad effect on the modulator output PSD spectrum. Table 3.4 presents the effect of DAC element mismatch on modulator SQNR and THD performance. Table 3.4: Practical DAC element mismatch summarization.

DAC element mismatch					
Mismatch level	0%	$\pm 0.25\%$	$\pm 0.5\%$	$\pm 1\%$	Pass/Fail
SQNR at MSA	123.2	118.5	113.2	111.3	Pass
THD at 1dB below MSA	-148.21	-133.4	-129.8	-123.6	Pass

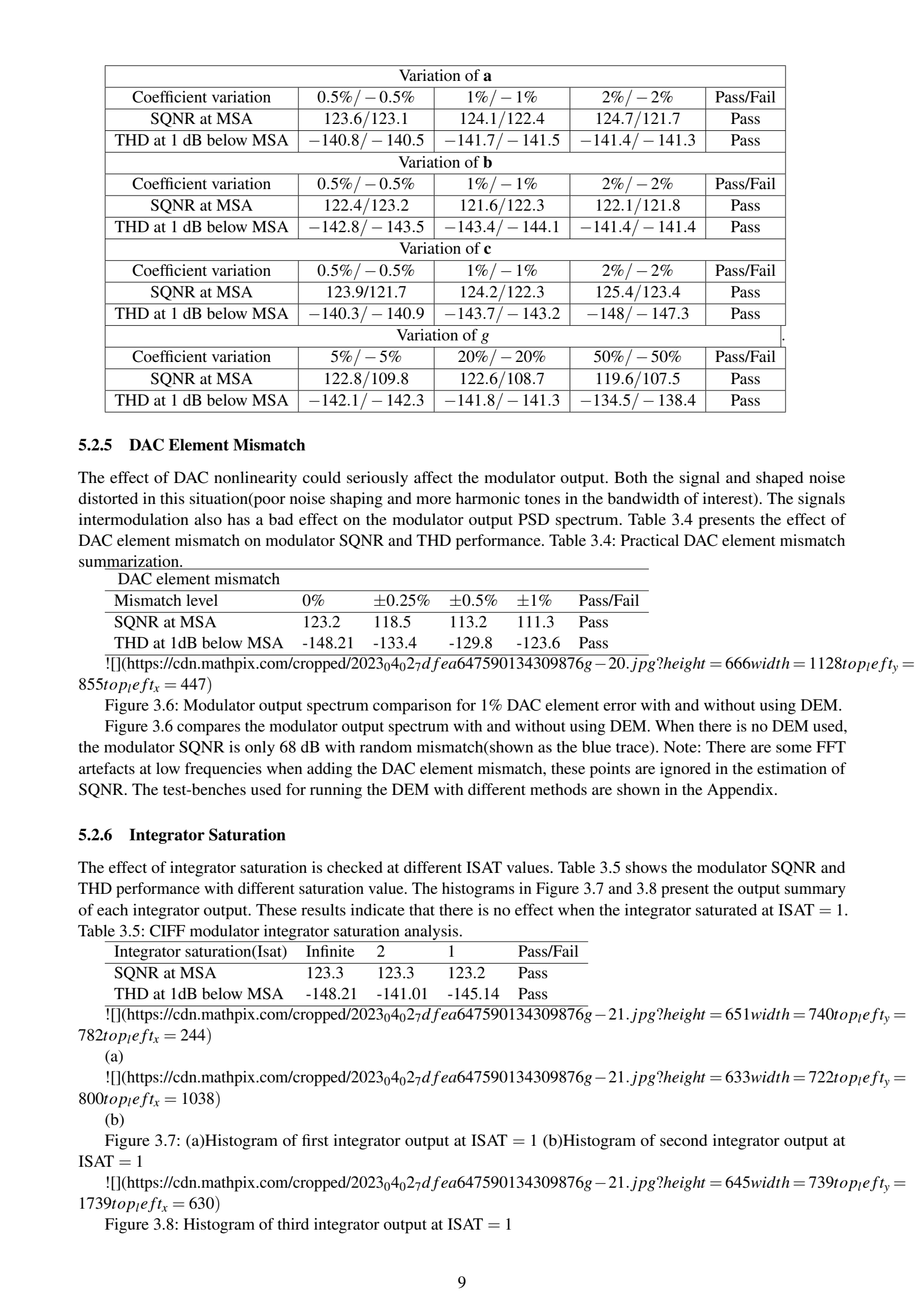


Figure 3.6: Modulator output spectrum comparison for 1% DAC element error with and without using DEM.

Figure 3.6 compares the modulator output spectrum with and without using DEM. When there is no DEM used, the modulator SQNR is only 68 dB with random mismatch(shown as the blue trace). Note: There are some FFT artefacts at low frequencies when adding the DAC element mismatch, these points are ignored in the estimation of SQNR. The test-benches used for running the DEM with different methods are shown in the Appendix.

5.2.6 Integrator Saturation

The effect of integrator saturation is checked at different ISAT values. Table 3.5 shows the modulator SQNR and THD performance with different saturation value. The histograms in Figure 3.7 and 3.8 present the output summary of each integrator output. These results indicate that there is no effect when the integrator saturated at ISAT $= 1$. Table 3.5: CIFF modulator integrator saturation analysis.

Integrator saturation(Isat)	Infinite	2	1	Pass/Fail
SQNR at MSA	123.3	123.3	123.2	Pass
THD at 1dB below MSA	-148.21	-141.01	-145.14	Pass

(a)

(b)

Figure 3.7: (a)Histogram of first integrator output at ISAT $= 1$ (b)Histogram of second integrator output at ISAT $= 1$

Figure 3.8: Histogram of third integrator output at ISAT $= 1$

5.2.7 Stability and Absence of Limit Cycle Tones

The modulator stability is verified by testing different types of input signal at different amplitude. The NTF optimization and multi-bits quantizer help to stabilize the modulator. Figure 3.9 presents the modulator output spectrum at different sine-wave frequencies. Figure 3.10 and 3.11 shows the modulator internal signals time domain behaviour with step and ramp input.

Figure 3.9: Modulator output spectrum with different frequencies sine-wave inputs. The amplitude of sine-wave is at MSA.

Figure 3.10: Modulator stability measurement with step signal input. The step is from 0 to 0.9 . ![](https://cdn.mathpix.com/cr
23.jpg?height=670&width=1262&top_left_y=438&top_left_x=403)

Figure 3.11: Modulator stability measurement with ramp signal input. The ramp is from 0 to 0.9 with a slope parameter of 18 .

5.2.8 Power and Area considerations

The design parameters trade-offs of a modulator are primarily depending on the specific applications. Some applications have more budget on burning power, while others might have more budget on consuming the silicon area.

For those applications that are keening on low power consumption, a high order modulator with low OSR is a good choice. However, the design complexity and stability of a high order modular are needed to take into consideration. For the applications that are focus on using a small footprint, a less complicated modulator will be a good choice. The area consumption of a modulator typically includes integrators, DACs, summing amplifiers and quantizer. For example, if the integrator is realised by using a Sample/Hold circuit, then the integrator size will primarily determined by the capacitors. In the real world, having a small physical footprint makes the design more competitive in terms of the bill of material(BOM).

For this project, there are multiple choices to achieve the modulator specifications. Trade-offs among modulator performance, area and power consumption need to be carefully balanced to use this project in a specific application.

5.3 Design Summary

Table 3.6: Modulator design summary.

Modulator parameters				
Modulator Type	Order	OSR	Quantizer Bits	Dither
CIFF	3	128	3	Yes (dither gain $1 = 0.1$)

Table 3.7: Modulator Specification compliance. The parameters show the extreme simulation conditions.

Modulator behaviour under different test conditions.					
Parameters	MSA	SQNR at MSA	THD(1 dB ($below$MSA)	*Tonesin audioband*	*Pass/− Fail*
Finite DC gain = 50	0.93	106.3	-123.15	No tones	Pass
Coefficient mismatch					
a varies 2%	0.93	121.7	-141.4	No tones	Pass
b varies 2%	0.93	121.8	-141.4	No tones	Pass
c varies 2%	0.93	123.4	-147.3	No tones	Pass
g varies 50%	0.93	107.5	-134.5	No tones	Pass
DAC elements vary 1%	0.93	111.3	-123.6	No tones	Pass
Integrator saturation = 1	0.93	123.3	-145.14	No tones	Pass
$Nostabilityandabsenceoflimitcycletones.Checkedwithdifferentinput conditions(dc,sine,stepandrampsignals)$					Pass
Integrator outputs dynamic range scaling.					

5.4 Conclusion

This chapter concludes with a comprehensive verification note on the designed modulator. The simulation results under extreme conditions justified that the modulator is able to work properly in different scenarios. Extensive simulations are run to check the effect of elements mismatch on modulator performance and design feasibility.

6 Chapter 4

7 S-MASH ^{2} Modulator Exploration

The proposed $2+2+1$ S$-MASH^2$ modulator has a great potential to be implemented in this project as it has good performance on SQNR, MSA and power consumption. The proposed S-MASH ^{2} modulator combines the advantages of both MASH and SMASH structures without facing those common issues, such as stability, modulator saturation and sensitivity of finite integrator gain.[5]

7.1 Potential Advantages of S-MASH ^{2} Modulator

Several advantages of this architecture are observed and summarized below.

- Very low OSR. The proposed fifth-order $2+2+1$ S-MASH ^{2} modulator only uses OSR=12 to achieve a good SQNR, which significantly reduce the power consumption compare with the third-order CIFF that uses OSR=128. Therefore, it is a great choice if this project is going to use in a low power application.[5]

- High dynamic range. The proposed implementation can convert full-scale input signal to digital output. This is a big advantage than using third-order CIFF modulator which achieves 0.93 for a full-scale inpur range of ± 1.

- Less sensitive to the integrator DC gain. The CIFF, CIFB and MASH modulator suffer from the finite integrator DC gain, while the proposed architecture has the immunity on the finite gain effect. This will greatly reduce the requirement on the amplifier circuit design. If the amplifier is using S$/$H circuit, the area consumption of capacitors will be smaller so that reduce the product size. - Relaxed constrains on digital filter. This S-MASH ^{2} architecture eases the requirement on accurate path matching for the digital filter.

- All quantization errors are shaped by the modulator order.

7.2 Practical Implementation Challenges

Two drawbacks of this proposed modulator are explained below.

- Extra DAC at the input stage and a slight increase of integrators swing.

- 4-bits quantizer in the first and third loop. 4-bits quantizer in the two loops means any DAC element mismatch will degrade the modulator performance a lot.

8 Chapter 5

9 Conclusion

9.1 Project Achievement

This project achieved the design of a third-order CIFF modulator with OSR=128 and 3bits quantizer. The extensive simulations justify that the modulator achieved all the design specifications. An exploration of the fifth-order S-MASH ^{2} modulator is discussed.

10 5.2 Future Development

There are more simulations that could be run to check the ADC properties. The small footprint of BOM and low power consumption are the key parameters for an audio product to be competitive in the market. Hence, knowing the details in the physical circuit design will help the designer to choose the most appropriate parameters(Order, OSR, and Quantizer bit) for the modulator.

The circuit implementation work could be done to take this project forward. Detail simulations for measuring the exact power and area consumption of the modulator can help to decide either using high order modulator with

low OSR or low order modulator with high OSR. The proposed fifth-order S-MASH ^{2} modulator in Chapter 4 only uses OSR=12 to achieve a good SQNR, which significantly reduce the power consumption. The area consumption for high order modulator is not a big issue if the product is manufactured with advanced process technology. However, the trade-off with manufacturing cost also needs to be taken into account.

11 References

[1] Richard Schreier, G. C.: 'Understanding delta-sigma data converters', in: (Wiley-IEEE Press, 2005), pp. 1-464.

[2] L.Young, B.: 'ECE 627 Project: Design of a High-Speed Delta-Sigma A/D Converter', in:

[3] Gyongy, I.: 'Data Converter Design in Simulink 5 lectures', in: (The University of Edinburgh, 2021).

[4] F.Maloberti, in: Data converters. (Netherlands: Springer, 2008).

[5] Maghari, N. and Un-Ku Moon: 'Multi-loop efficient sturdy MASH delta-sigma modulators', in: 2008 IEEE International Symposium on Circuits and Systems, pp. 1216-1219, DoI: 10.1109/ ISCAS. 2008.4541643

12 Appendix A

13 Appendix

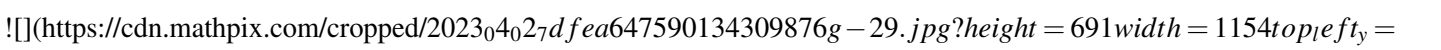


Figure A.1: SQNR estimation with 1-bit quantiser.

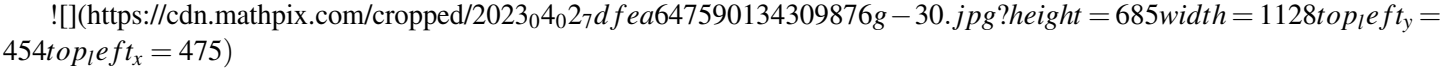


Figure A.2: SQNR estimation with 2-bits quantiser.

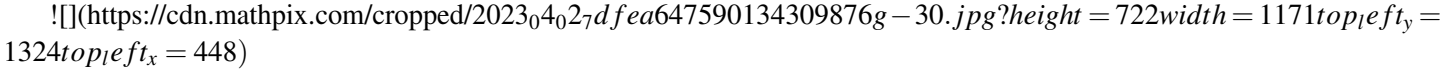


Figure A.3: SQNR estimation with 3-bits quantiser.

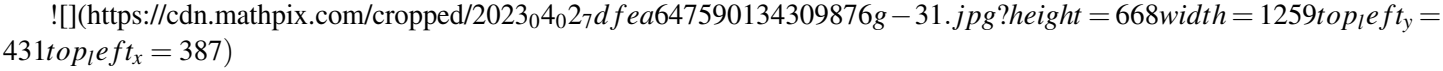


Figure A.4: $2+1$ MASH modulator schematic.

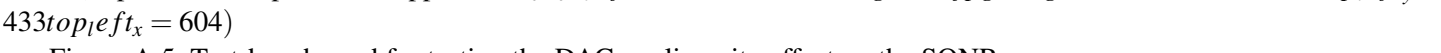


Figure A.5: Test-bench used for testing the DAC nonlinearity effect on the SQNR.

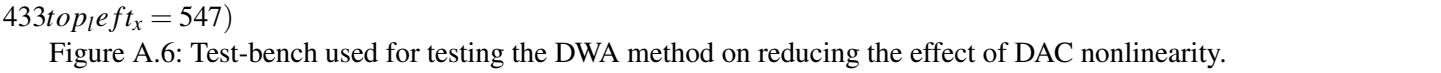


Figure A.6: Test-bench used for testing the DWA method on reducing the effect of DAC nonlinearity.

References

A Class Labels

```
#### Define Lables ####
class_labels = {
  "Climbing stairs": 0,
  "Descending stairs": 1,
  "Desk work": 2,
  "Lying down left": 3,
  "Lying down on back": 4,
  "Lying down on stomach": 5,
  "Lying down right": 6,
  "Movement": 7,
  "Running": 8,
  "Sitting bent backward": 9,
  "Sitting bent forward": 10,
  "_Sitting_": 11,
  "Standing": 12,
  "Walking": 13
}
```

Figure 1: Dictionary used for 14 class CNN