GDS Import Wizard V3.1 Manual

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Content

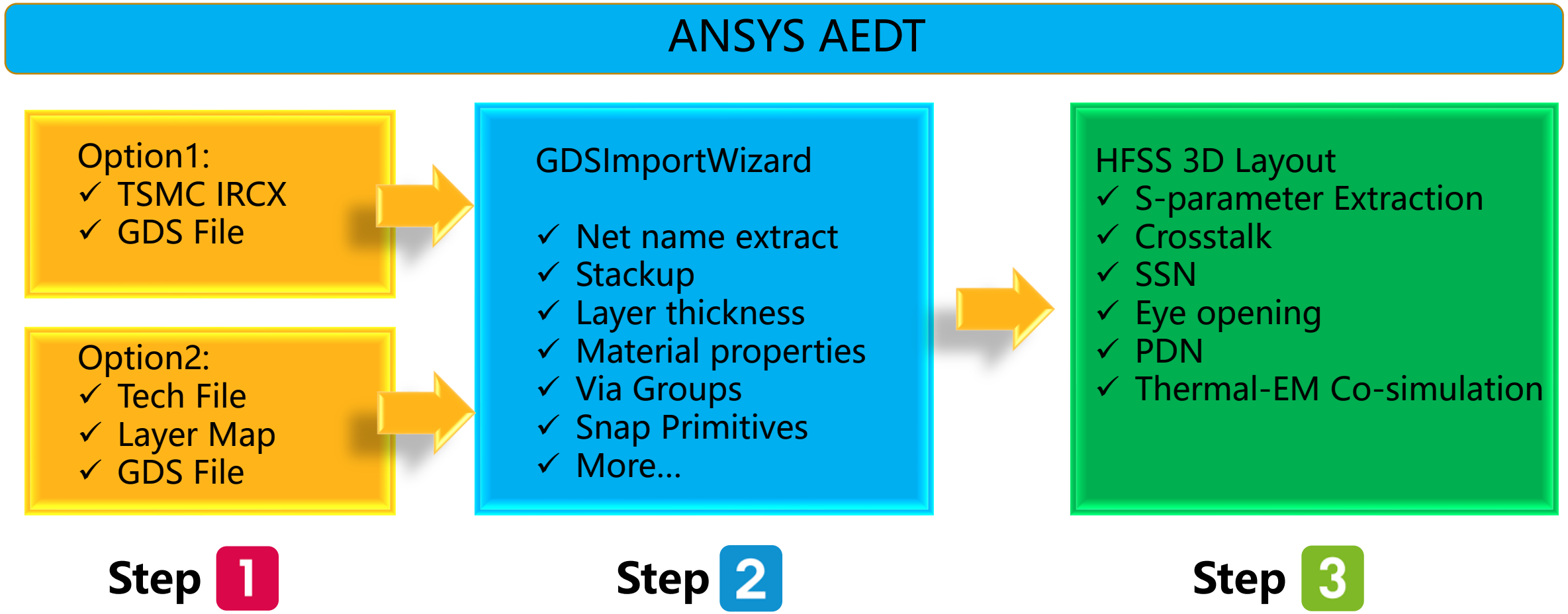
About GDS Import Wizard

A smart tool to translate GDSII to 3DLayout EDB quickly:

- Extract nets from GDS and import to EDB
- Extract accurate material property from IRCX
- Extract accurate layer thickness and stack up from IRCX
- Generate control xml for AEDT Import Module
- Support dielectric merge when importing
- Support overlapping and laminated stack up
- Automatic create Via Group and SnapViaGroups
- Generate components on top and bottom layer
- Generate TSV coating and Insulating layer
- Synchronous import to AEDT when EDB prepared

ANSYS workflow for 2.5D/3D SI Interpower Simulation

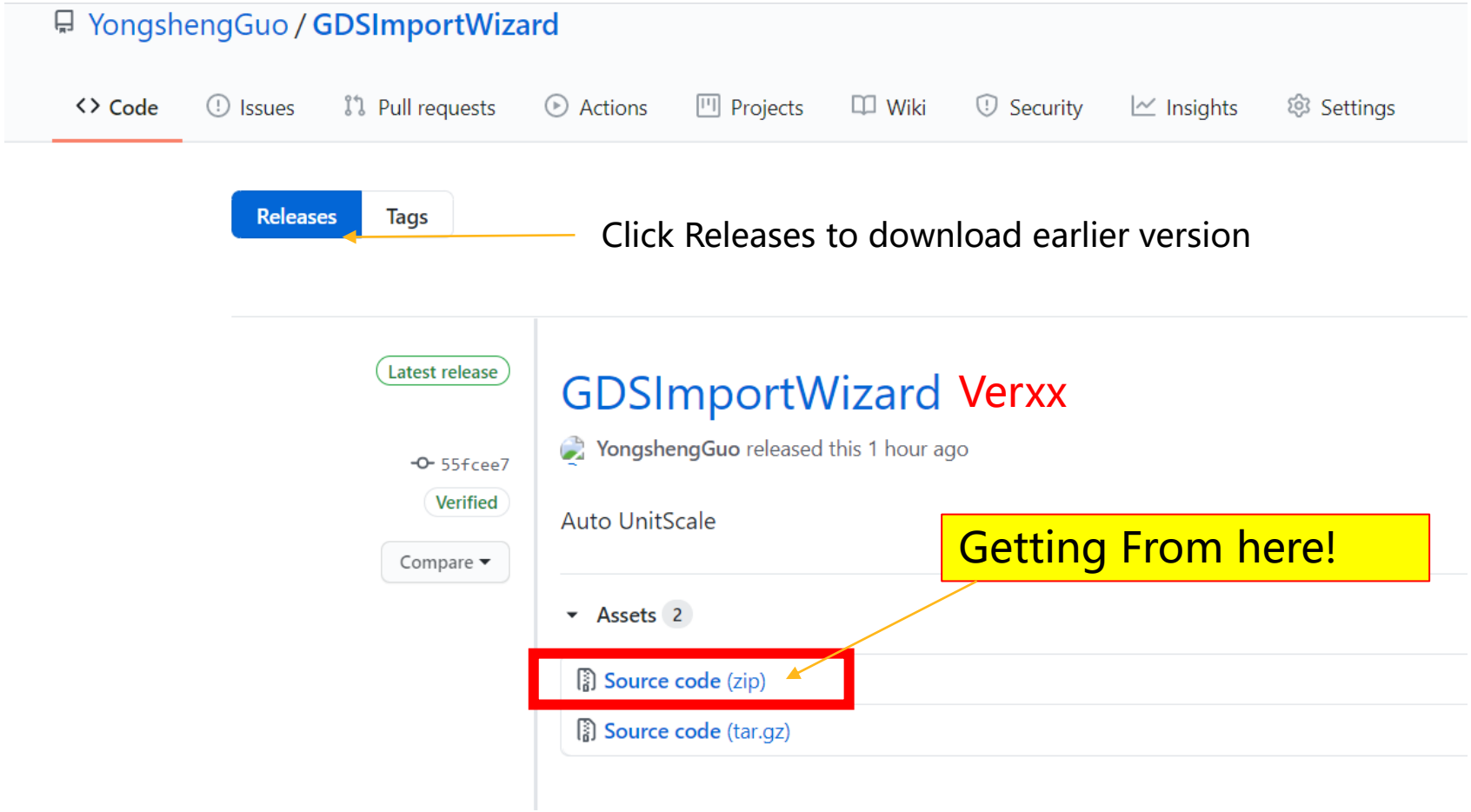
Return



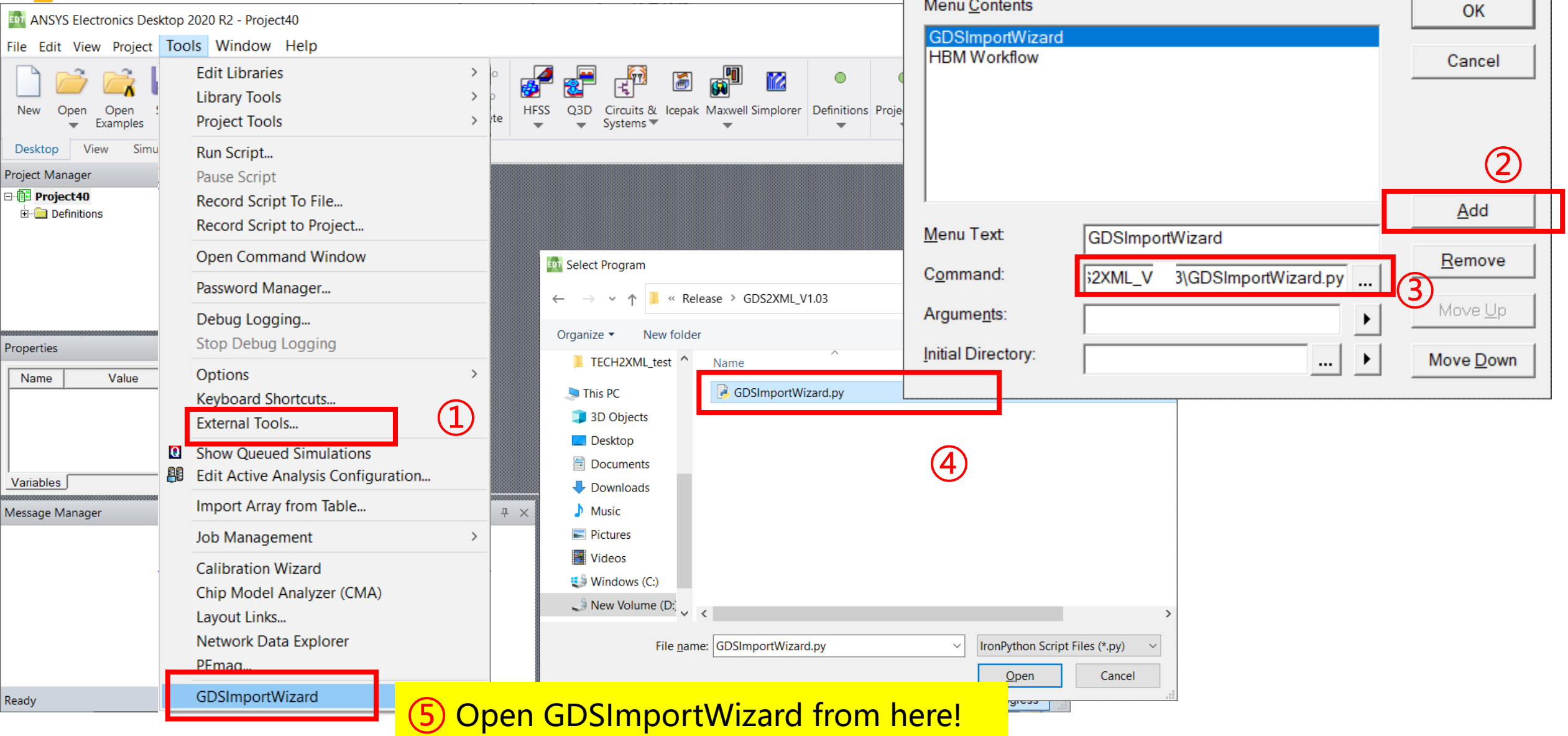
Getting the latest GDSImportWizard Tool

Return

https://github.com/YongshengGuo/GDSImportWizard/releases/latest

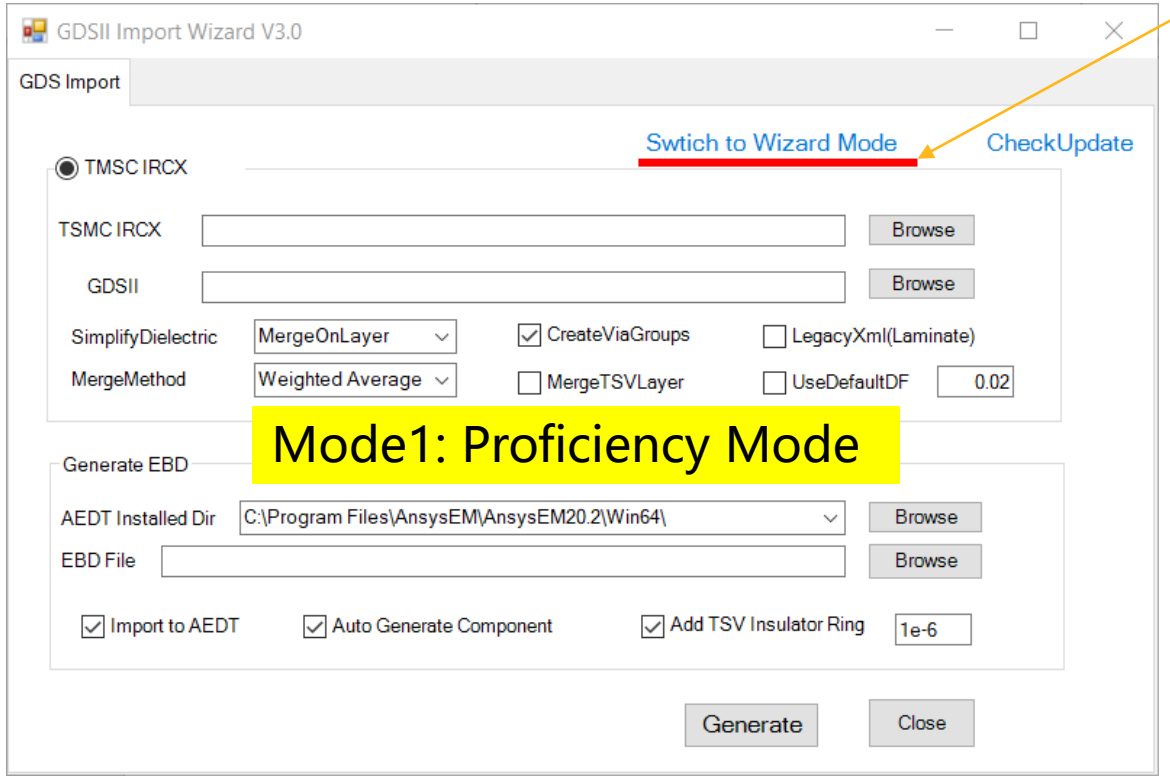


Add GDS Import Wizard to AEDT

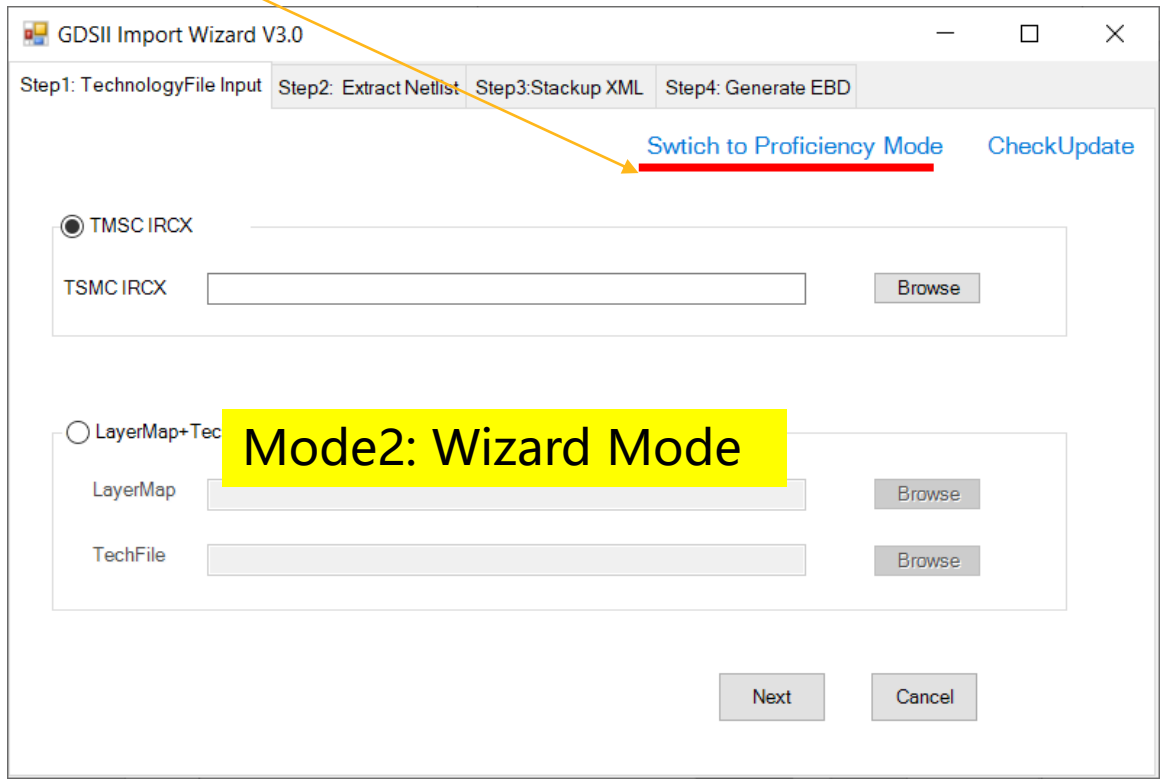


New Proficiency Mode modes in V3.0

Switching two modes by click here



Mode1: Proficiency Mode

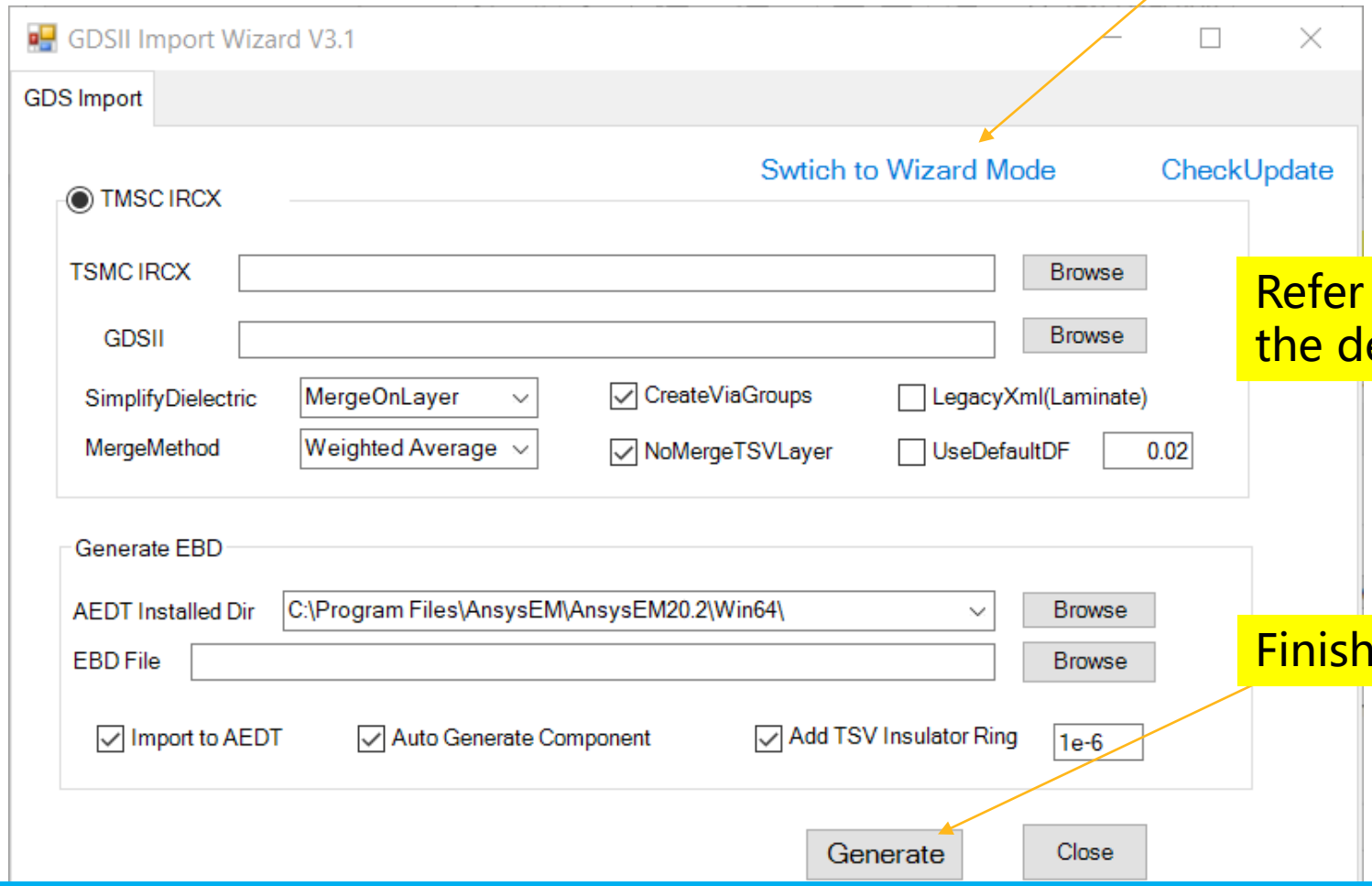


Mode2: Wizard Mode

Running in Proficiency Mode

Proficiency Mode

Switch to wizard mode from here



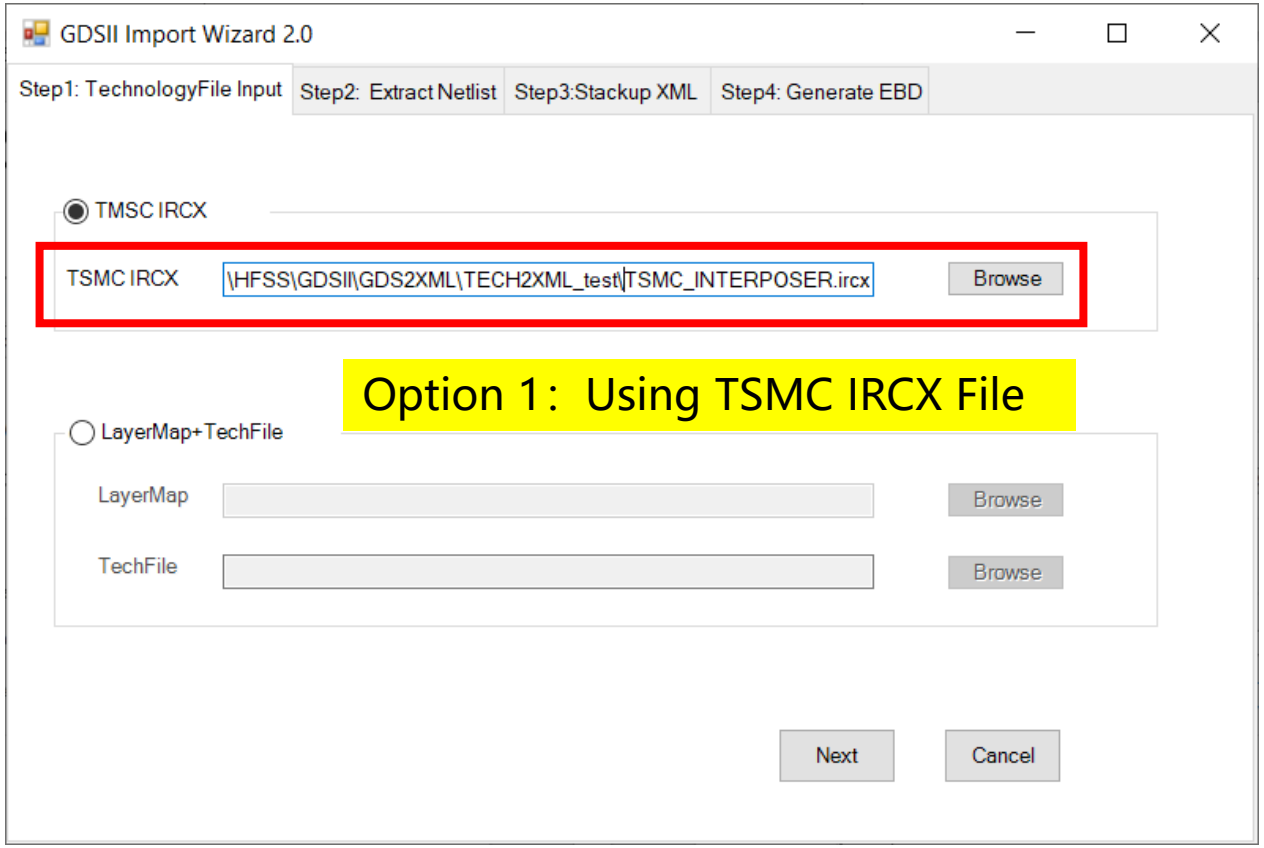
Refer to “Wizard Mode” section for the detail comments for Options.

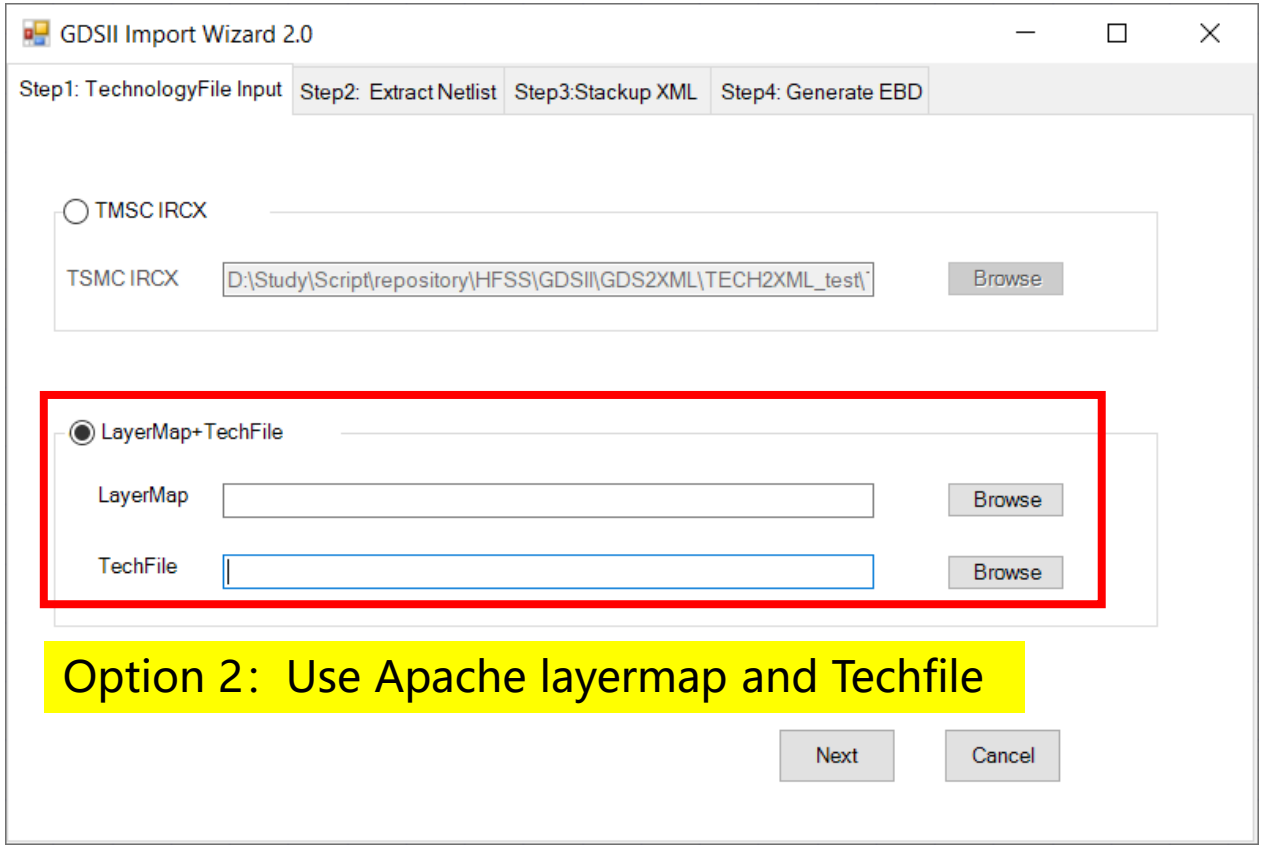
Finished whole import flow once

Note: Proficiency mode has the same options as Wizard mode.
Proficiency mode provides quick import way for users who are familiar with the workflow.
Please refer to “Wizard Mode "document for the detail comments for all Options input.

Running in Wizard Mode

Step1: Define Technology File





Option 1: Using TMSC IRCX File is suggested workflow.

What about IRCX

IRCX is an EDA data format for interconnect modeling with TSMC's 65- and 40-nm process technologies.

Include:

- ✓ Layer Mapping
- ✓ Layer Thickness
- ✓ Layer Material property

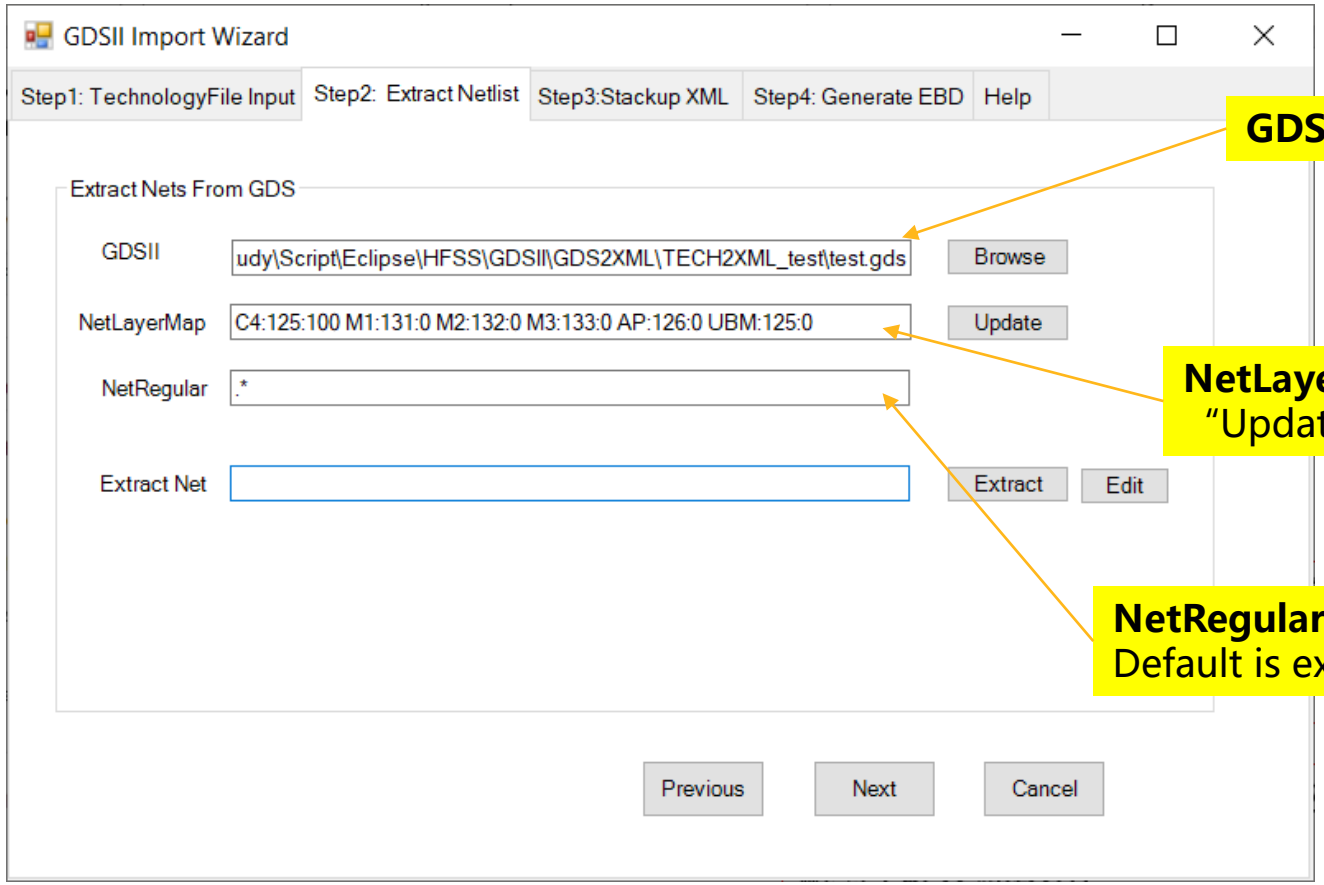
Application:

- ✓ RC parasitic extraction,
- ✓ electromigration analysis,
- ✓ power integrity analysis, and
- ✓ electromagnetic simulation

```
[RC SPICE INFORMATION]
LAYER {
* STACK 34 4 (NAME:V, MEASURED_FROM:V, HEIGHT:V, THICKNESS:V)
FIELD       MEASURED_FROM   HEIGHT  THICKNESS
NAME
ubump         UF1           142.639000  0.001000
UF1           PASS4         107.640000 35.000000
PASS4         PASS3b        107.040000  0.600000
PASS3b        PASS3a        106.640000  0.400000
PASS3a        PASS2         105.190000  1.450000
metal4        PASS2         105.190000  1.450000
PASS2         PASS1         104.490000  0.700000
PASS1         IMD3c         104.415000  0.075000
IMD3c         IMD3b         103.690000  0.725000
IMD3b         IMD3a         103.640000  0.050000
metal3        IMD3a         103.565000  0.850000
IMD3a         IMD2g         103.020000  0.620000
IMD2g         IMD2f         102.970000  0.050000
IMD2f         IMD2e         102.245000  0.725000
IMD2e         IMD2d         102.195000  0.050000
metal2        IMD2d         102.120000  0.850000
IMD2d         IMD2c         101.873000  0.322000
IMD2c         IMD2b         101.793000  0.080000
ctm           IMD2b         101.793000  0.080000
IMD2b         IMD2a         101.775000  0.018000
IMD2a         IMD1c         101.575000  0.200000
cbm           IMD1c         101.575000  0.200000
IMD1c         IMD1b         101.525000  0.050000
IMD1b         IMD1a         100.800000  0.725000
IMD1a         ILD           100.750000  0.050000
metal1        ILD           100.675000  0.850000
ILD           substrate     100.000000  0.750000
substrate     PASSB1        0.000000 100.000000
PASSB1        PASSB2b       -0.800000  0.800000
mb1           PASSB2b       -0.801000  0.001000
PASSB2b       PASSB2a       -2.800000  2.000000
PASSB2a       underFill_C   -3.200000  0.400000
underFill_C   N/A           -3.201000  0.001000
ubmb          N/A           -3.201000  0.001000
```

```
[LAYER_MAPPING]
#substate is reversed-tone NWELL
#via4 is (ubump AND metal4)
#ubump_top_pin is ubump_pin
#ubmb_top_pin is ubmb_pin
#RC      GDS LVS      DFII
ubump        170;0    ubump        UBM;drawing
metal4           74;0     metal4           AP;drawing
DUM4             74;1     DUM4             AP;dummy
metal3           33;40    metal3           M3;drawing
DUM3             33;41    DUM3             M3;dummy
metal2           32;40    metal2           M2;drawing
DUM2             32;41    DUM2             M2;dummy
metal1           31;40    metal1           M1;drawing
DUM1             31;41    DUM1             M1;dummy
mb1      31;100  MB1      M1;BSL
ubmb         170;100 UBMB         UBM;BSL
via4         86;0     via4         CB2;drawing
via3         85;0     via3             RV;drawing
via2             52;40    via2             VIA2;drawing
via1             51;40    via1             VIA1;drawing
tsv      251;0    tsv      TSV;drawing
tsv_3t       251;3    tsv_3t       TSV;dummy1
pmb      5;100    PMB      PM;dummy
ubump_pin        125;0    ubm_top_pin      UBM;pin
metal4_pin       126;0    metal4_pin       AP;pin
metal3_pin       133;0    metal3_pin       M3;pin
metal2_pin       132;0    metal2_pin       M2;pin
metal1_pin       131;0    metal1_pin       M1;pin
mb1_pin          131;100 MB1_pin          M1;BSP
ubmb_pin         125;100 UBMB_pin         UBM;test0
ctm      77;0     ctm      CTM;drawing
cbm      88;0     cbm      CBM;drawing
ctm_via      51;40    ctm_via          VIA1;drawing
cbm_via      51;40    cbm_via          VIA1;drawing
```

Step2：Extract Nets information from GDSII

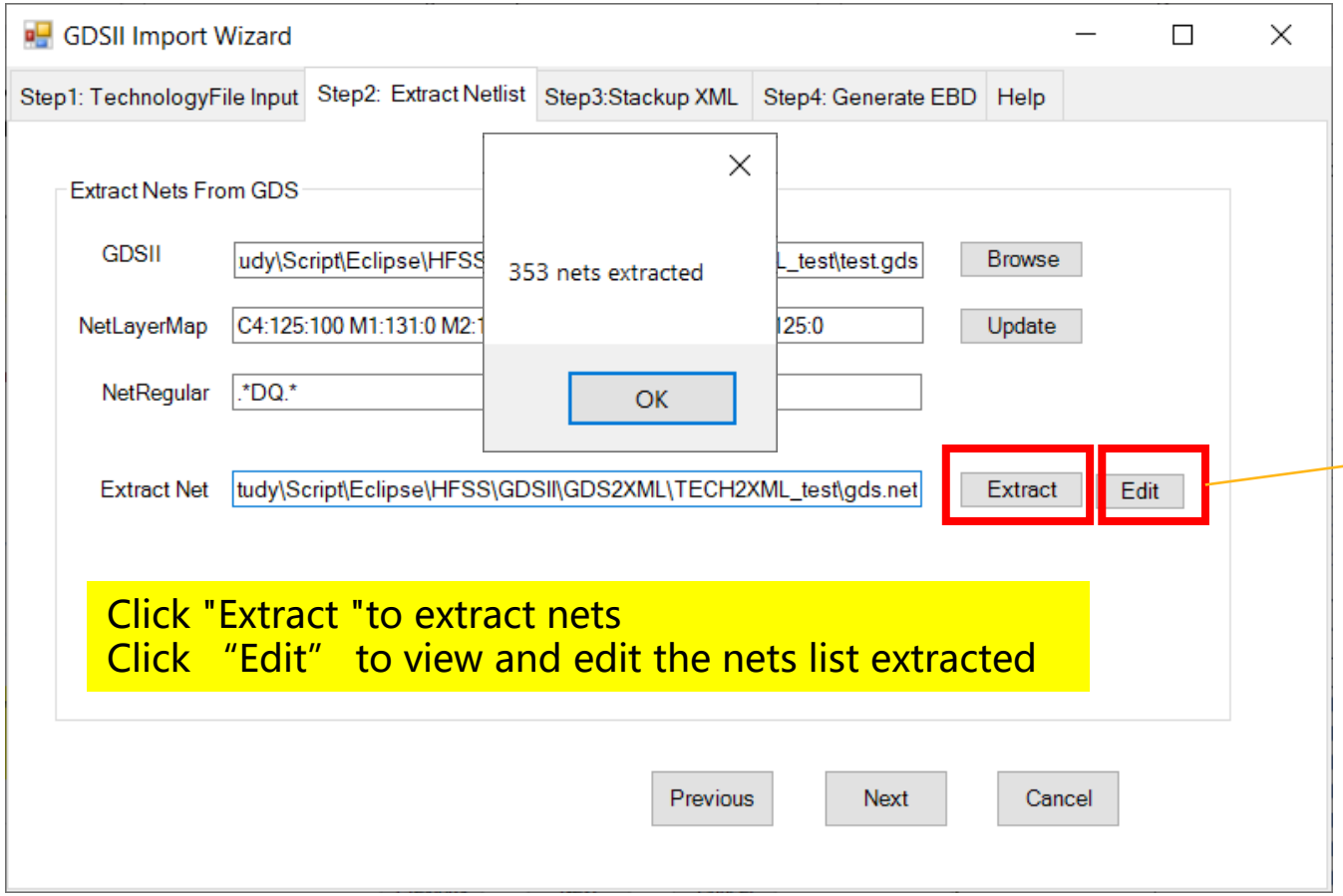


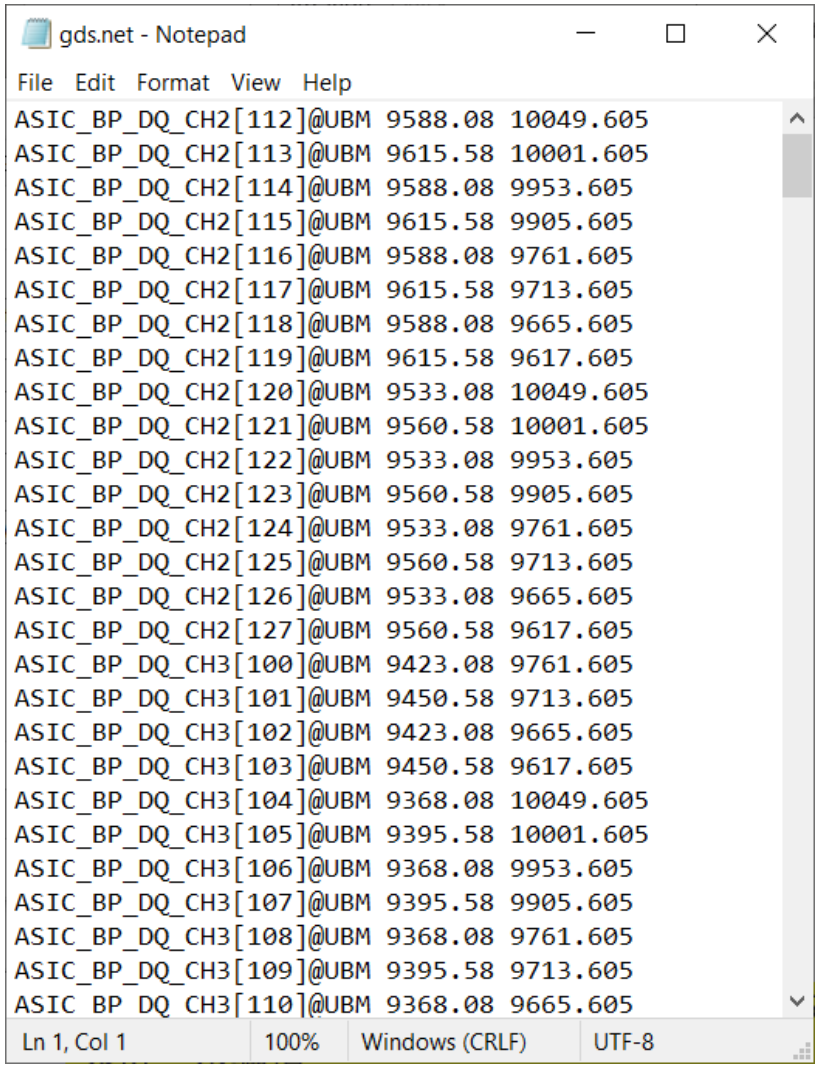
GDSII: set GDS File

NetLayerMap：GDS Layer include net information, click “Update” button to extract from layermap or IRCX.

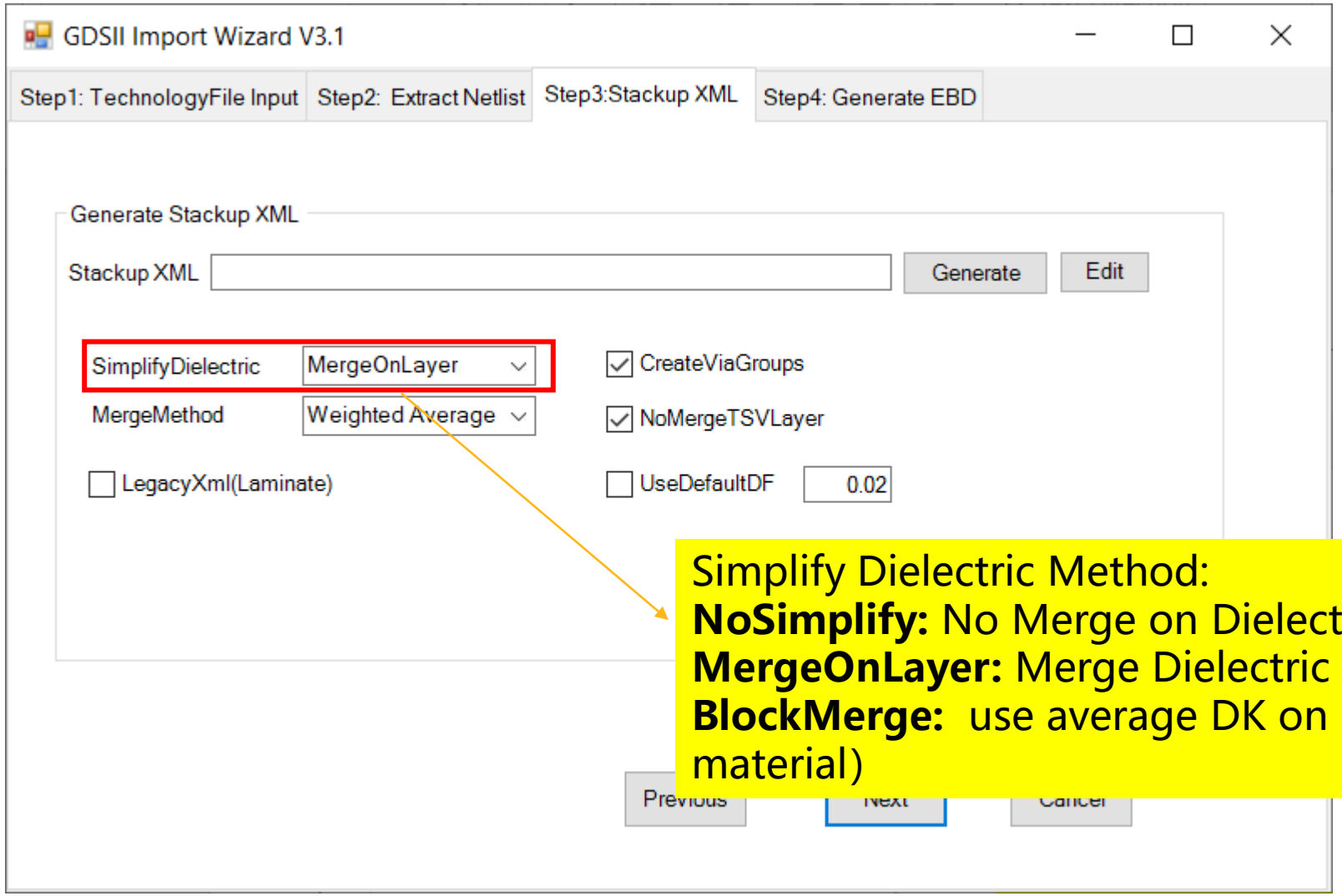
NetRegular：Using regular expressions to filter nets extracted. Default is extracted all nets.

Step2：Extract Nets information from GDSII





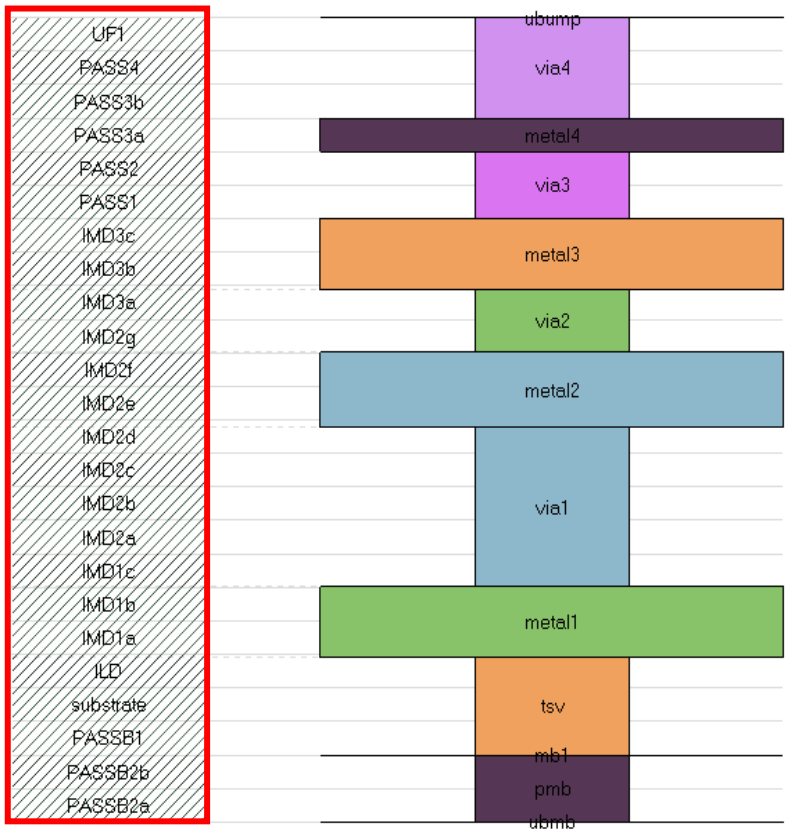
Step3：Generate Stackup XML (Control file)



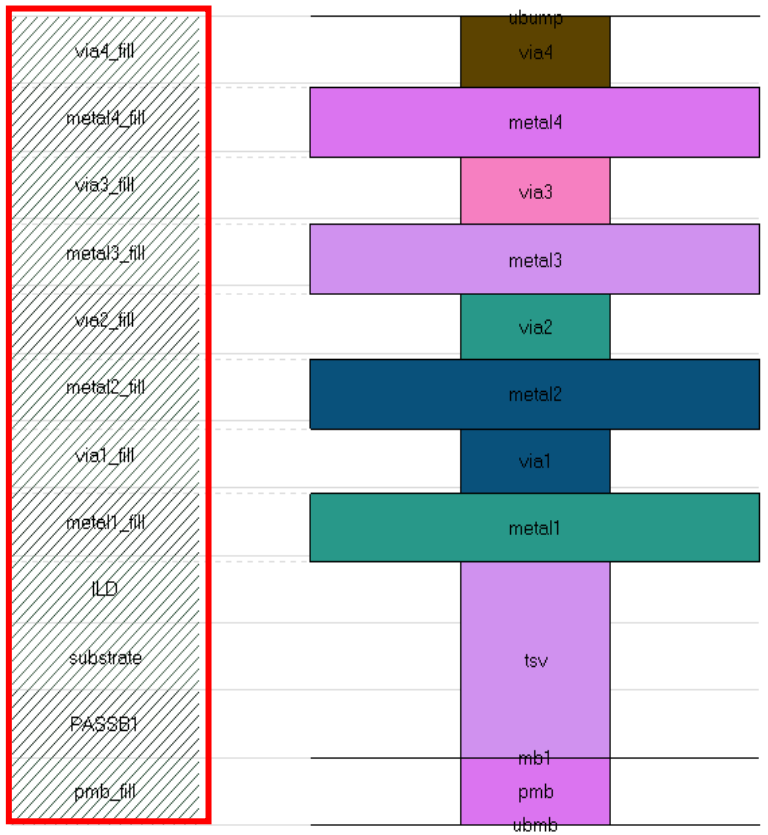
Simplify Dielectric Method:
NoSimplify: No Merge on Dielectric
MergeOnLayer: Merge Dielectric on each conduct layer
BlockMerge: use average DK on each conduct (except SI material)

Step3：Generate Stackup XML (Control file)

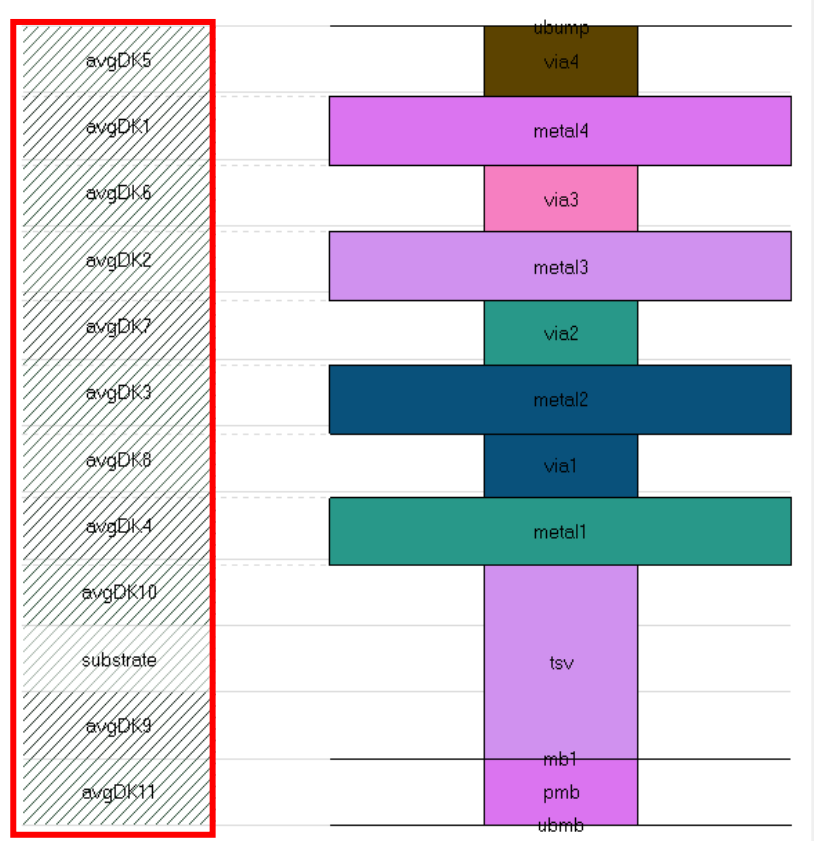
- Simplify Dielectric Method compare



NoSimplify

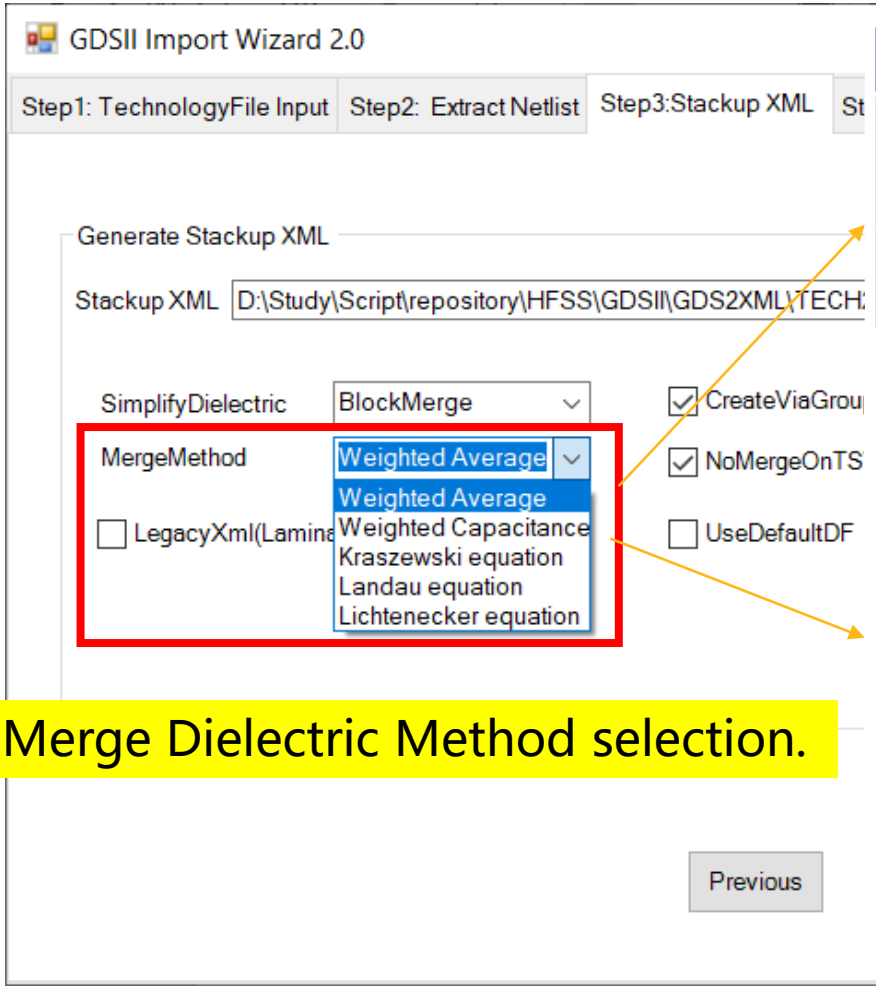


MergeOnLayer



BlockMerge

Step3： Generate Stackup XML (Control file)



Merge Dielectric Method selection.

Method	Equation
Weighted Capacitance	$\varepsilon_{r\_merged} = \frac{\sum_{i=1}^{n} h_i}{\sum_{i=1}^{n} \frac{h_i}{\varepsilon_i}}$
Weighted Average	$\varepsilon_{r\_merged} = \frac{\sum_{i=1}^{n} h_i \varepsilon_i}{\sum_{i=1}^{n} h_i}$

There are Kraszewski (Kraszewski equation)

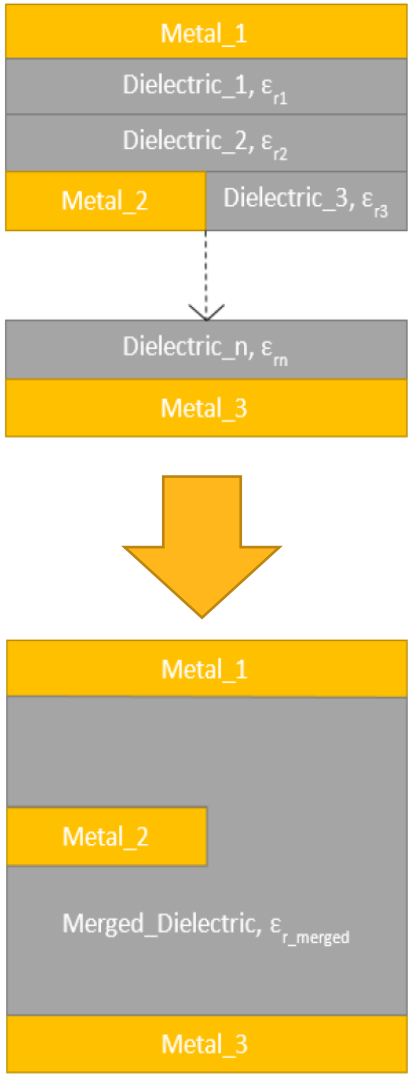
$$\sqrt{\varepsilon^*} = v_1\sqrt{\varepsilon_1} + v_2\sqrt{\varepsilon_2} + v_3\sqrt{\varepsilon_3} \quad (1)$$

Landau, Lifshitz and Looyenga, (Landau equation)

$$\sqrt[3]{\varepsilon^*} = v_1\sqrt[3]{\varepsilon_1} + v_2\sqrt[3]{\varepsilon_2} + v_3\sqrt[3]{\varepsilon_3} \quad (2)$$

Lichtenecker, (Lichtenecker equation)

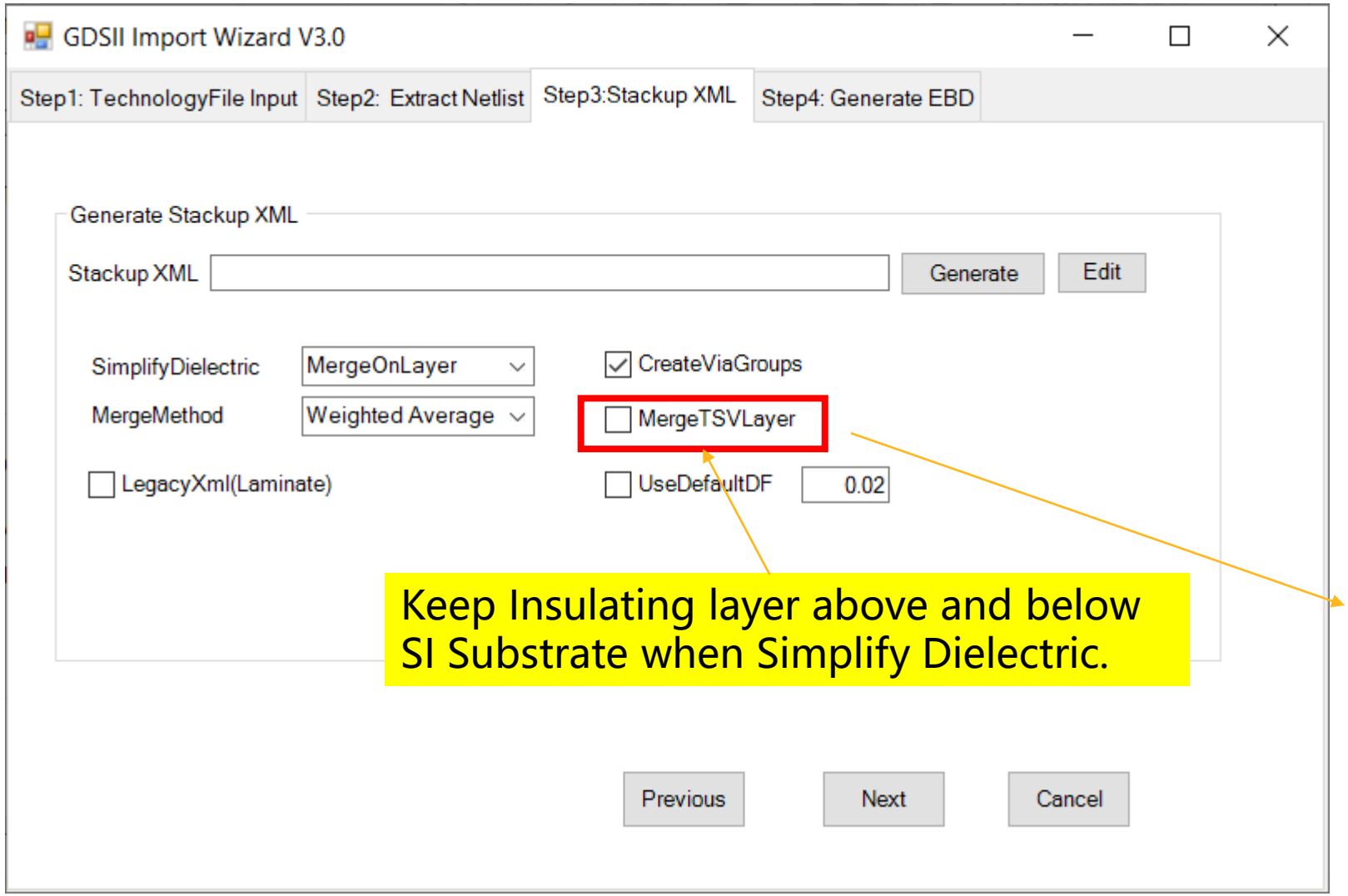
$$\ln \varepsilon^* = v_1 \ln \varepsilon_1 + v_2 \ln \varepsilon_2 + v_3 \ln \varepsilon_3 \quad (3)$$



Merge Dielectric

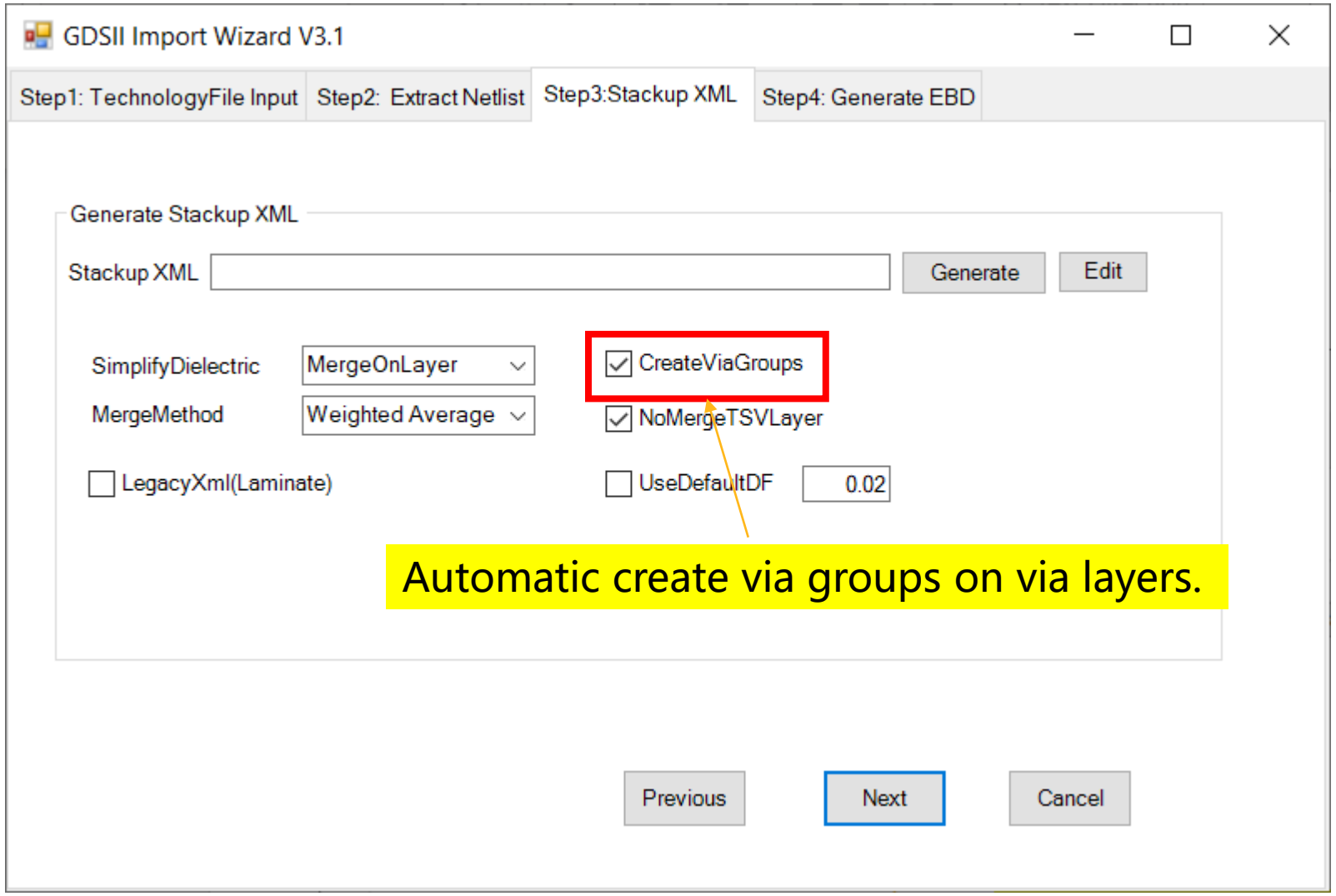
Note: Merge Dielectric also can be done in 3d Layout stackup editor.

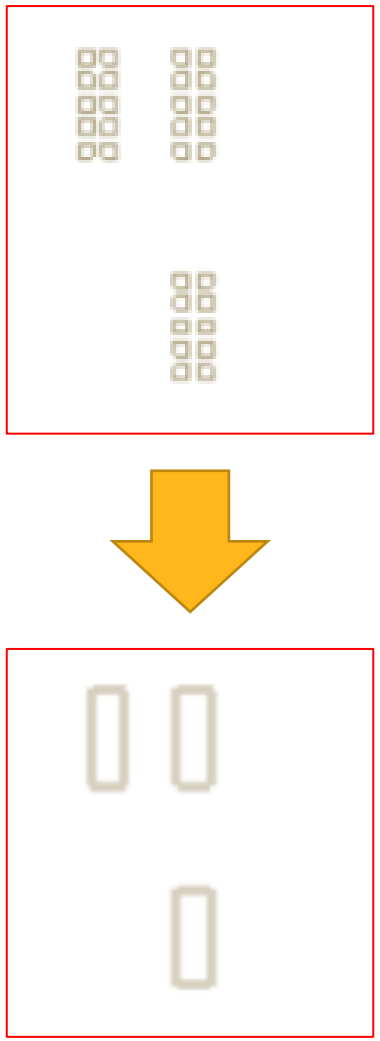
Step3：Generate Stackup XML (Control file)



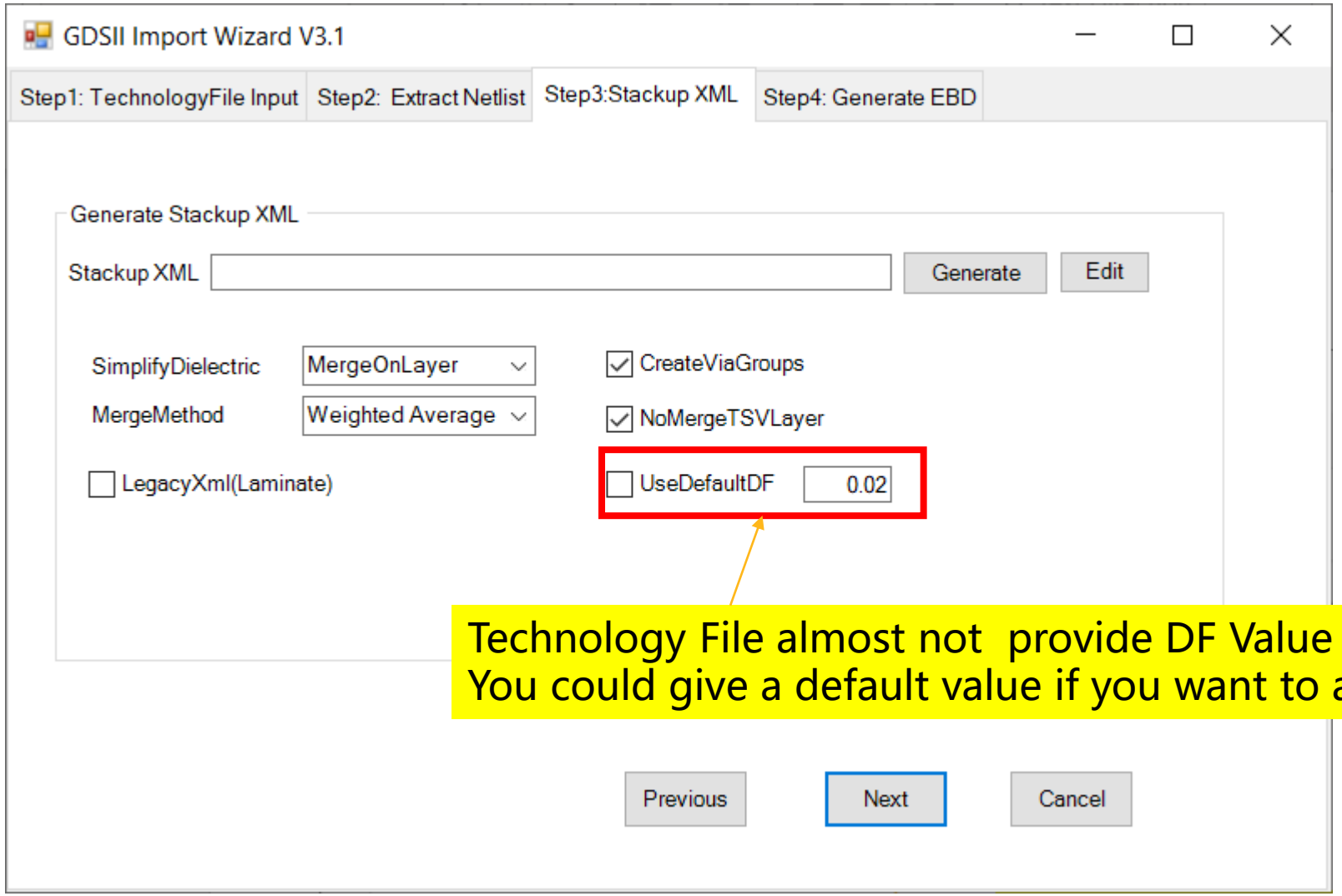
Keep Insulating layer above and below SI Substrate when Simplify Dielectric.

Step3：Generate Stackup XML (Control file)



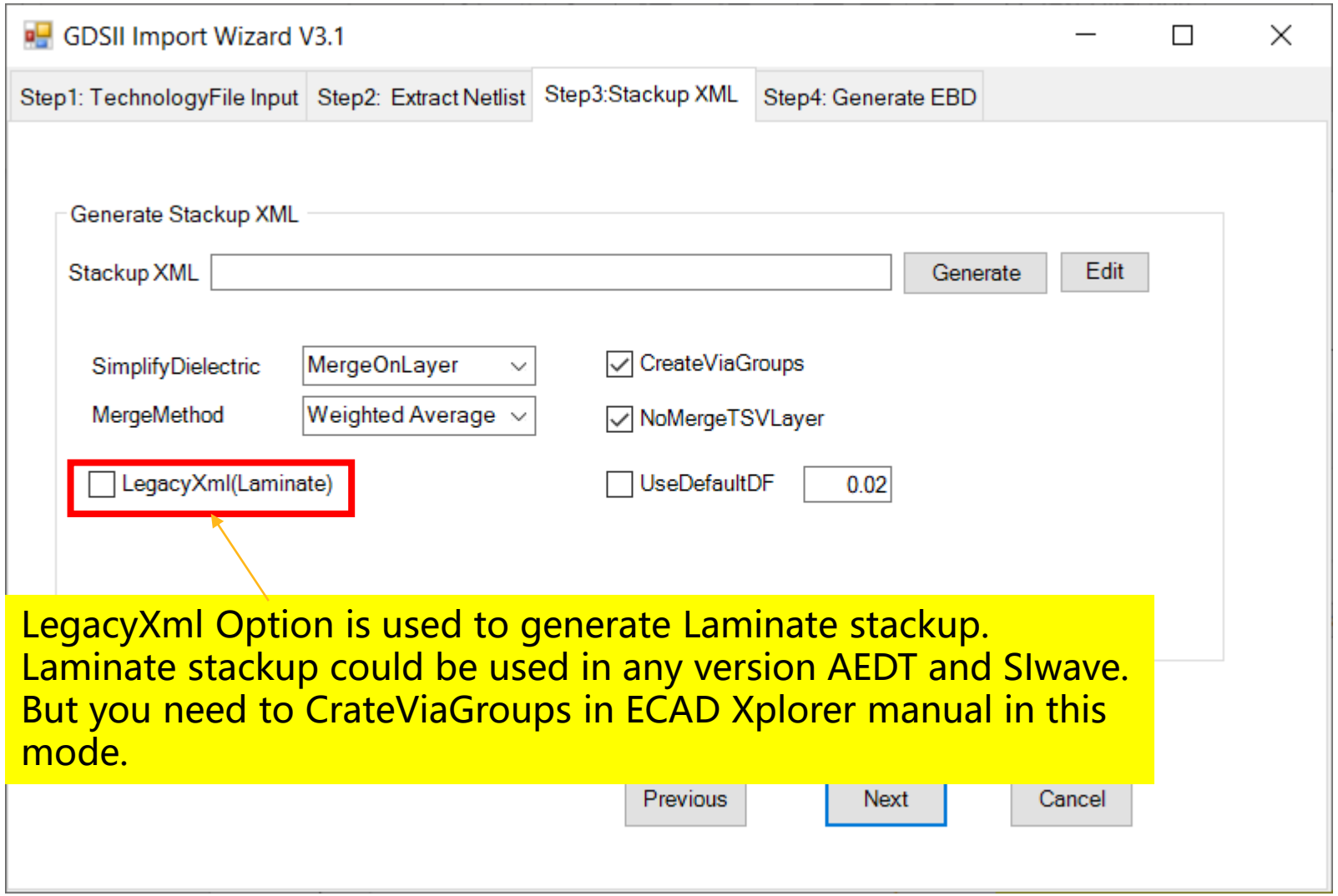


Step3：Generate Stackup XML (Control file)



Technology File almost not provide DF Value for all material.
You could give a default value if you want to at here.

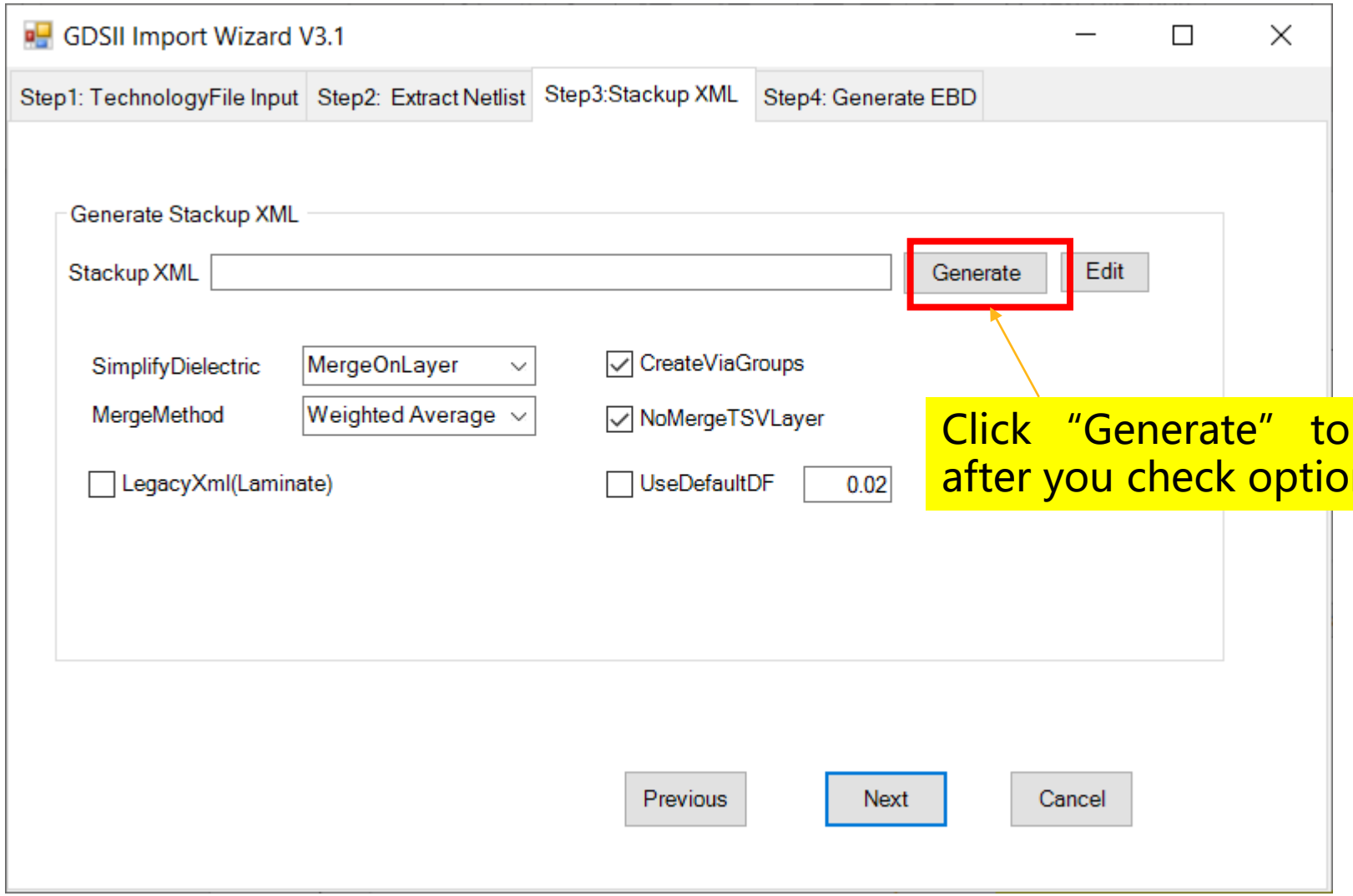
Step3：Generate Stackup XML (Control file)



LegacyXml Option is used to generate Laminate stackup. Laminate stackup could be used in any version AEDT and SIwave. But you need to CrateViaGroups in ECAD Xplorer manual in this mode.

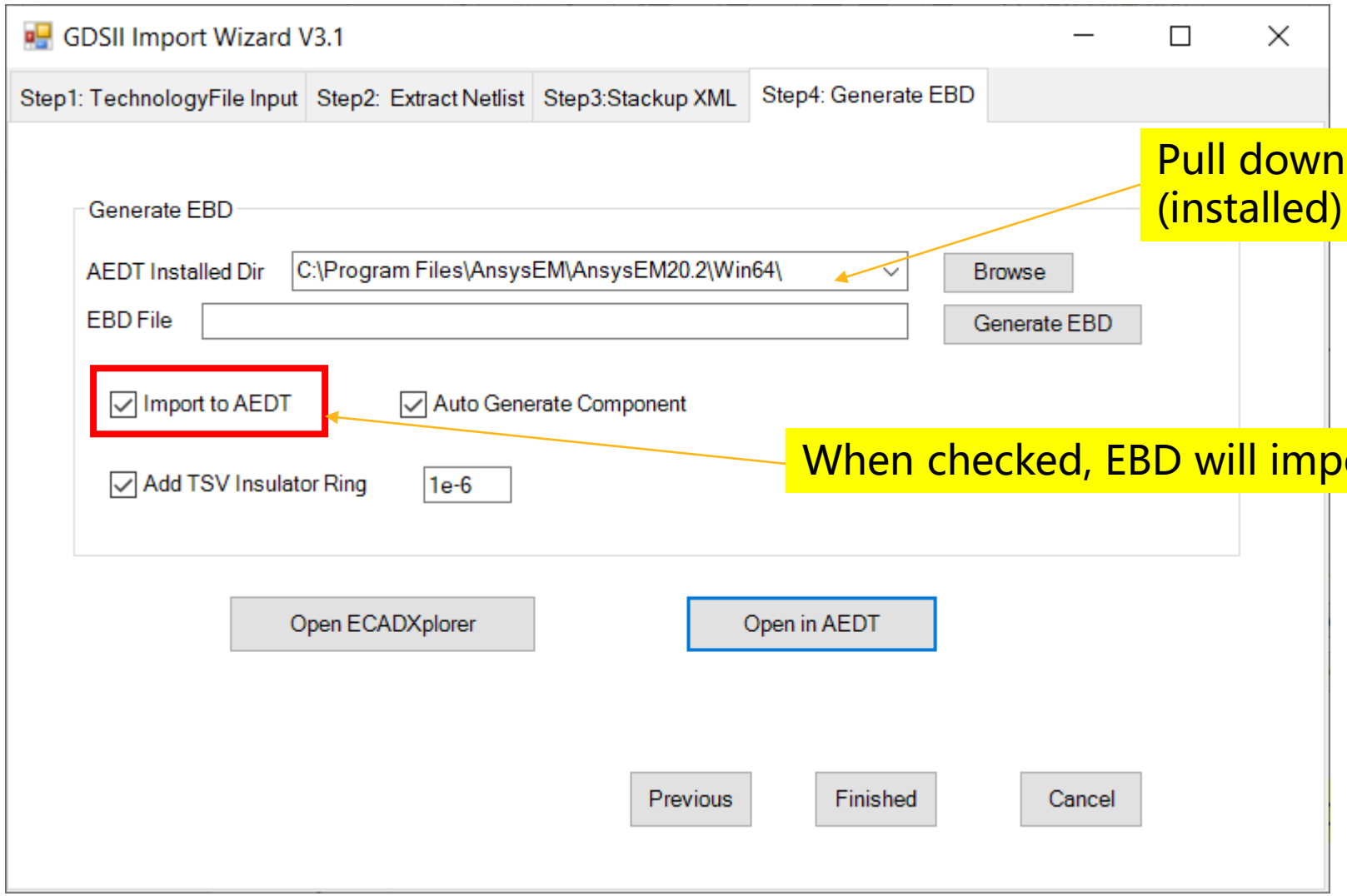
By default, GDSImportWizard generate Overlapping stackup which could create ViaGroups automatically.

Step3：Generate Stackup XML (Control file)



Click “Generate” to generate Control xml after you check options.

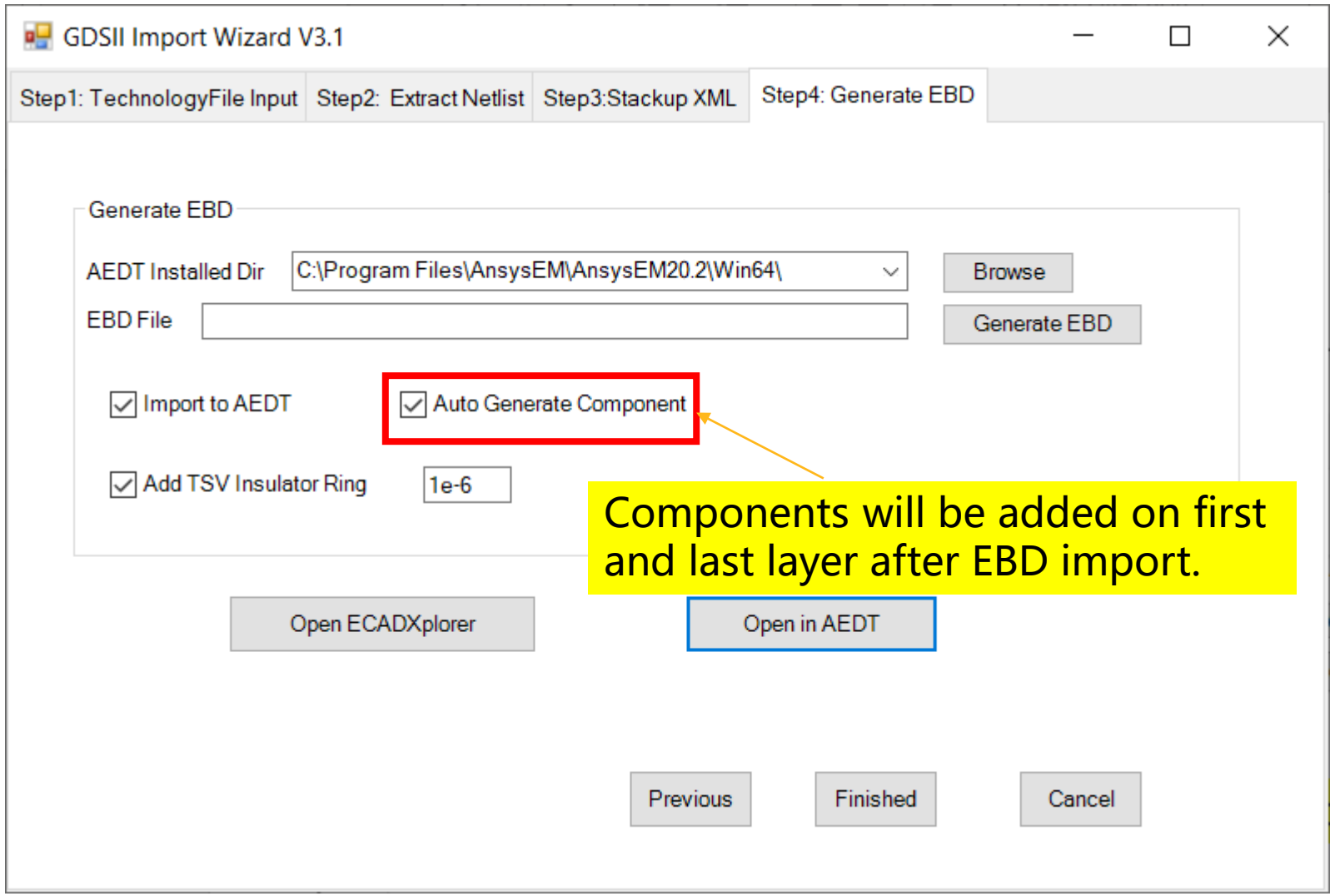
Step4：Generate EBD

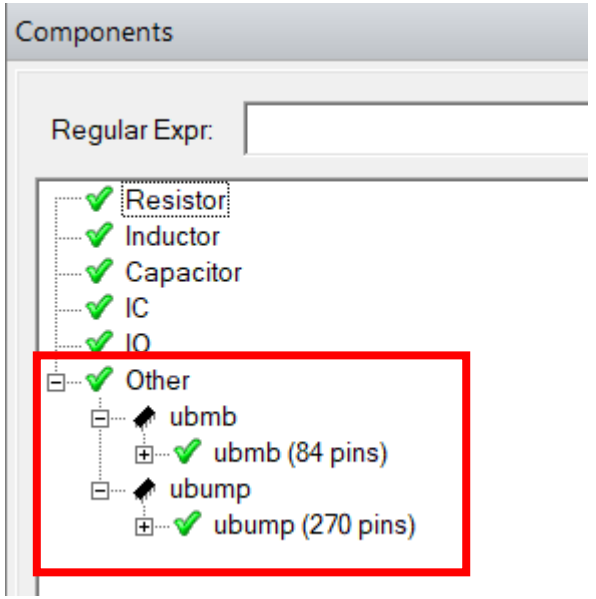


Pull down and Select AEDT version (installed)

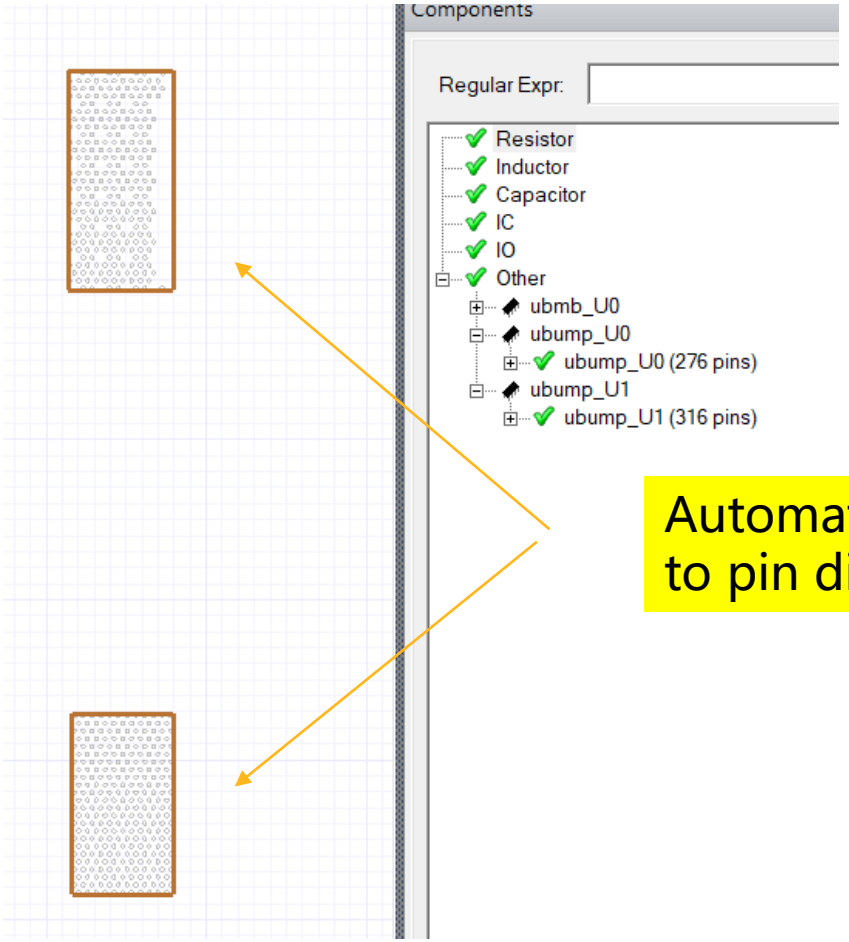
When checked, EBD will import to AEDT after generated

Step4：Generate EBD



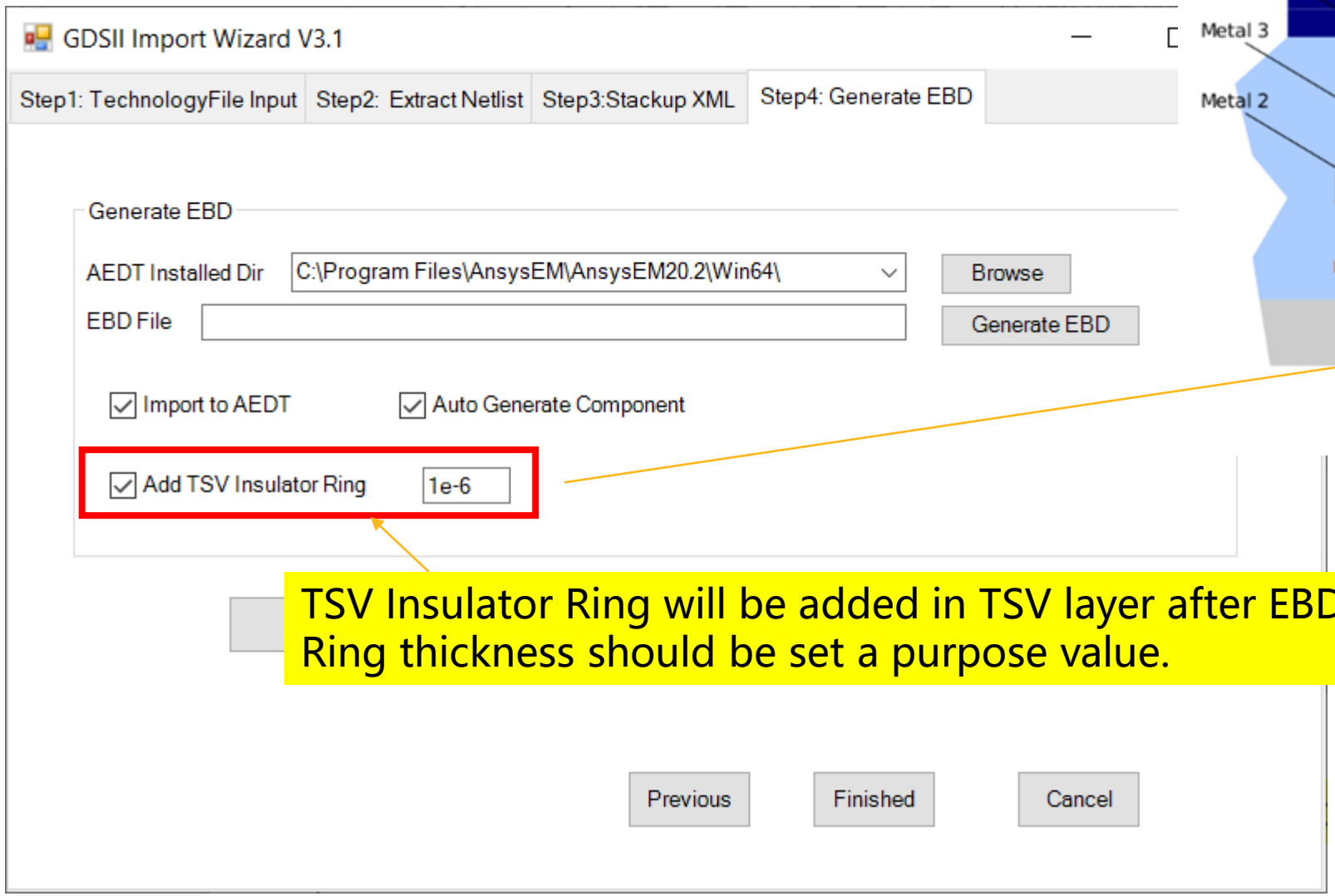


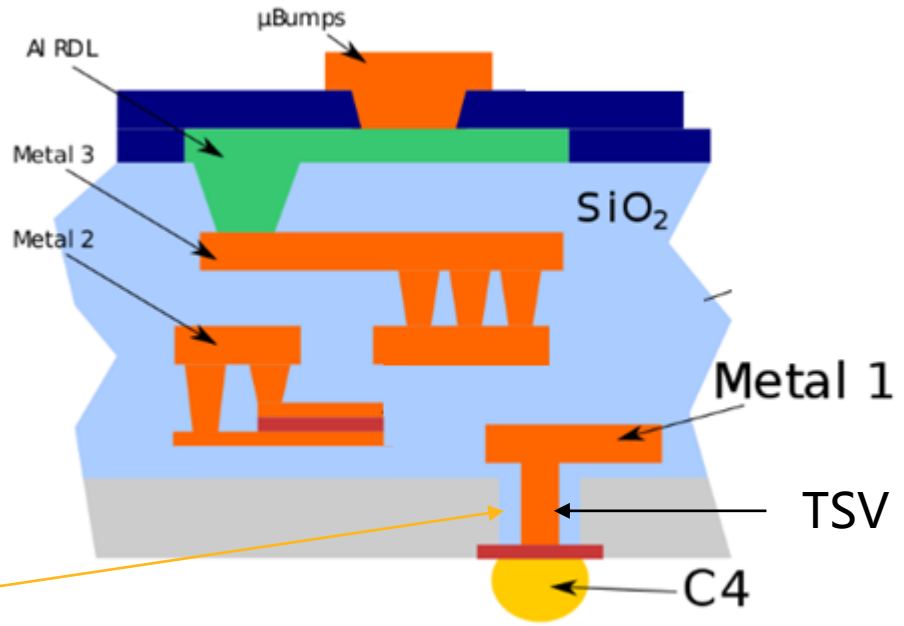
Step4：Generate EBD



Automatically generate individual components according to pin distribution and spacing. (New in V3.x)

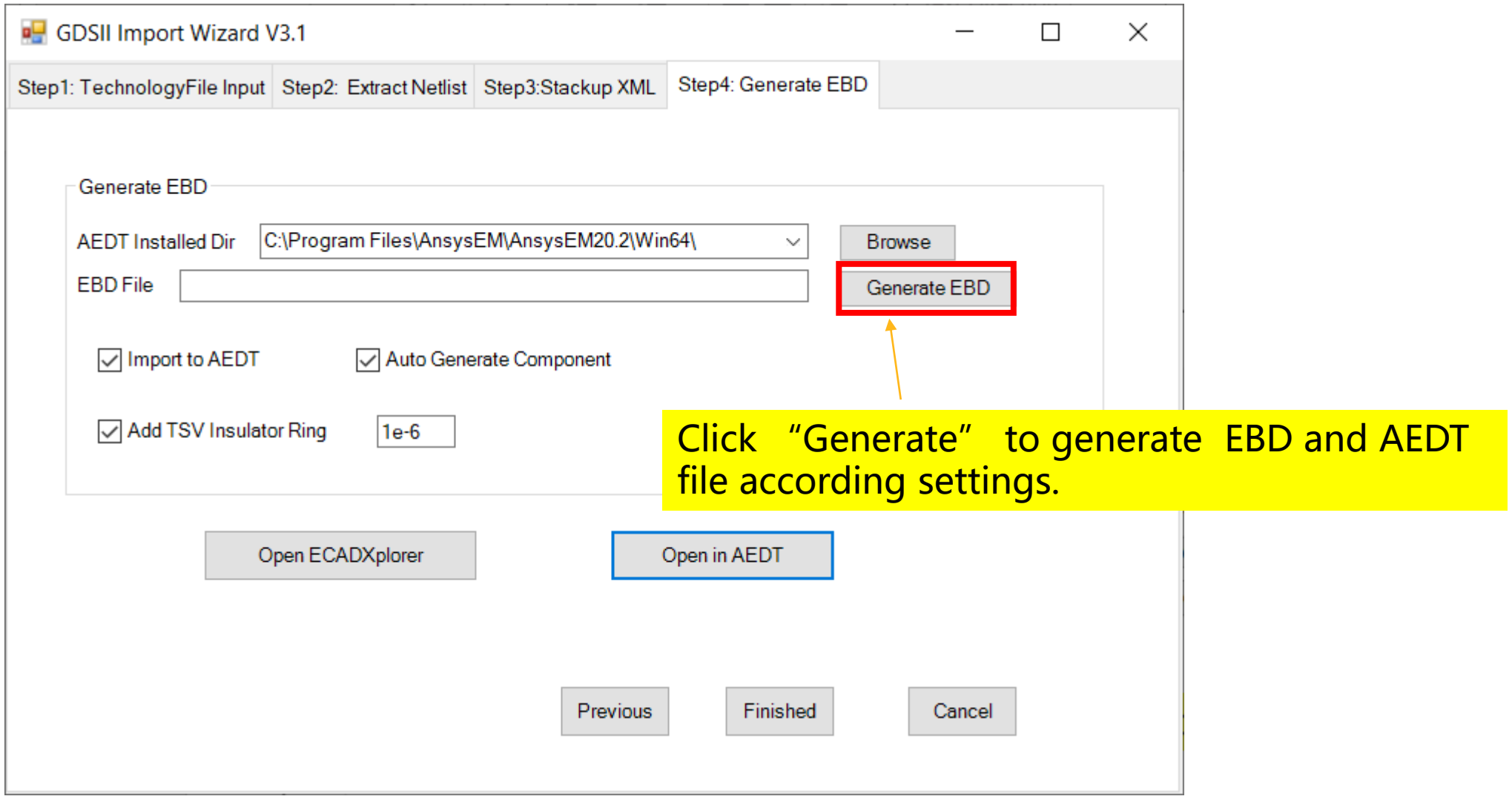
Step4：Generate EBD





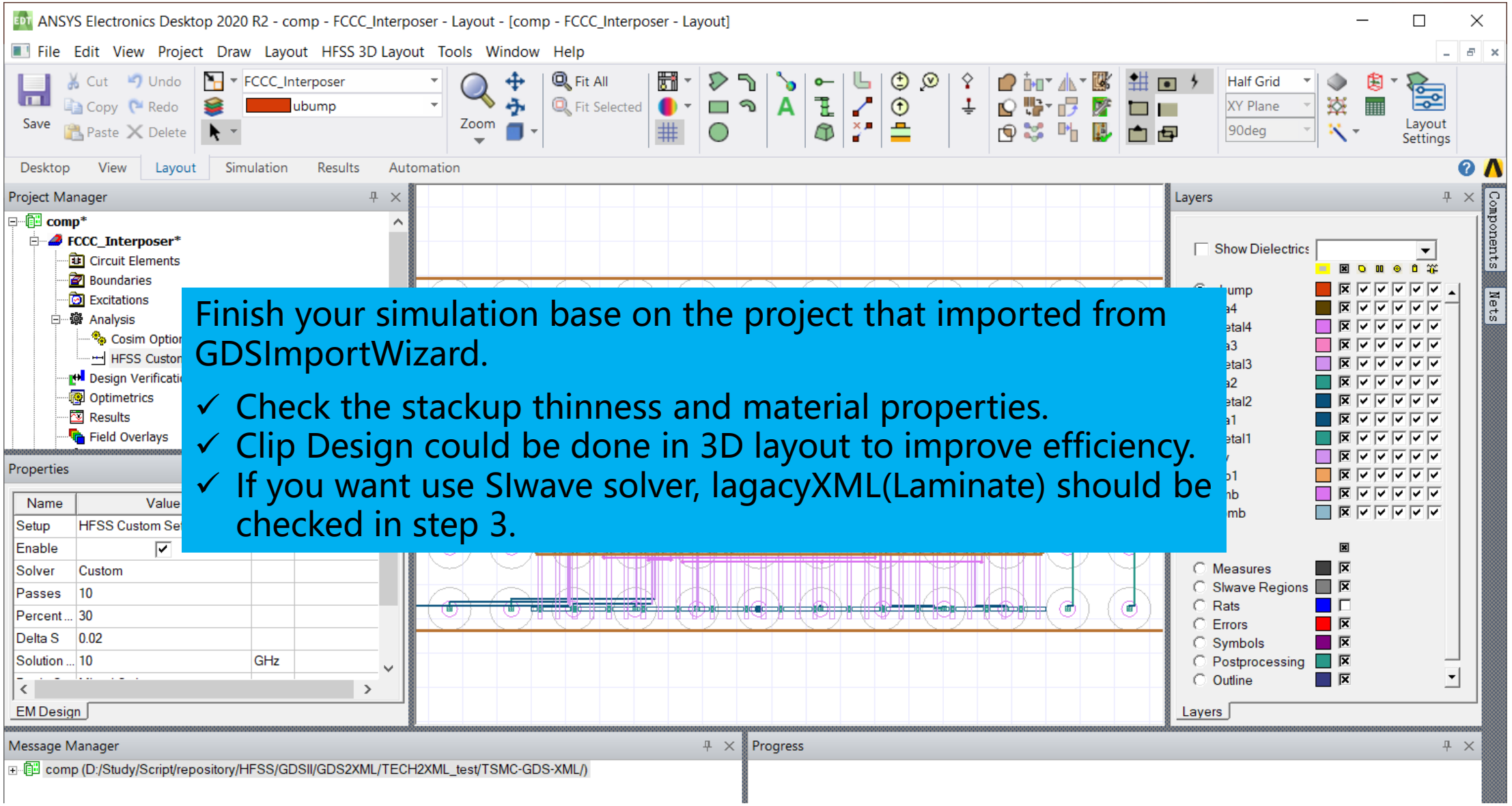
TSV Insulator Ring will be added in TSV layer after EBD imported.
Ring thickness should be set a purpose value.

Step4：Generate EBD

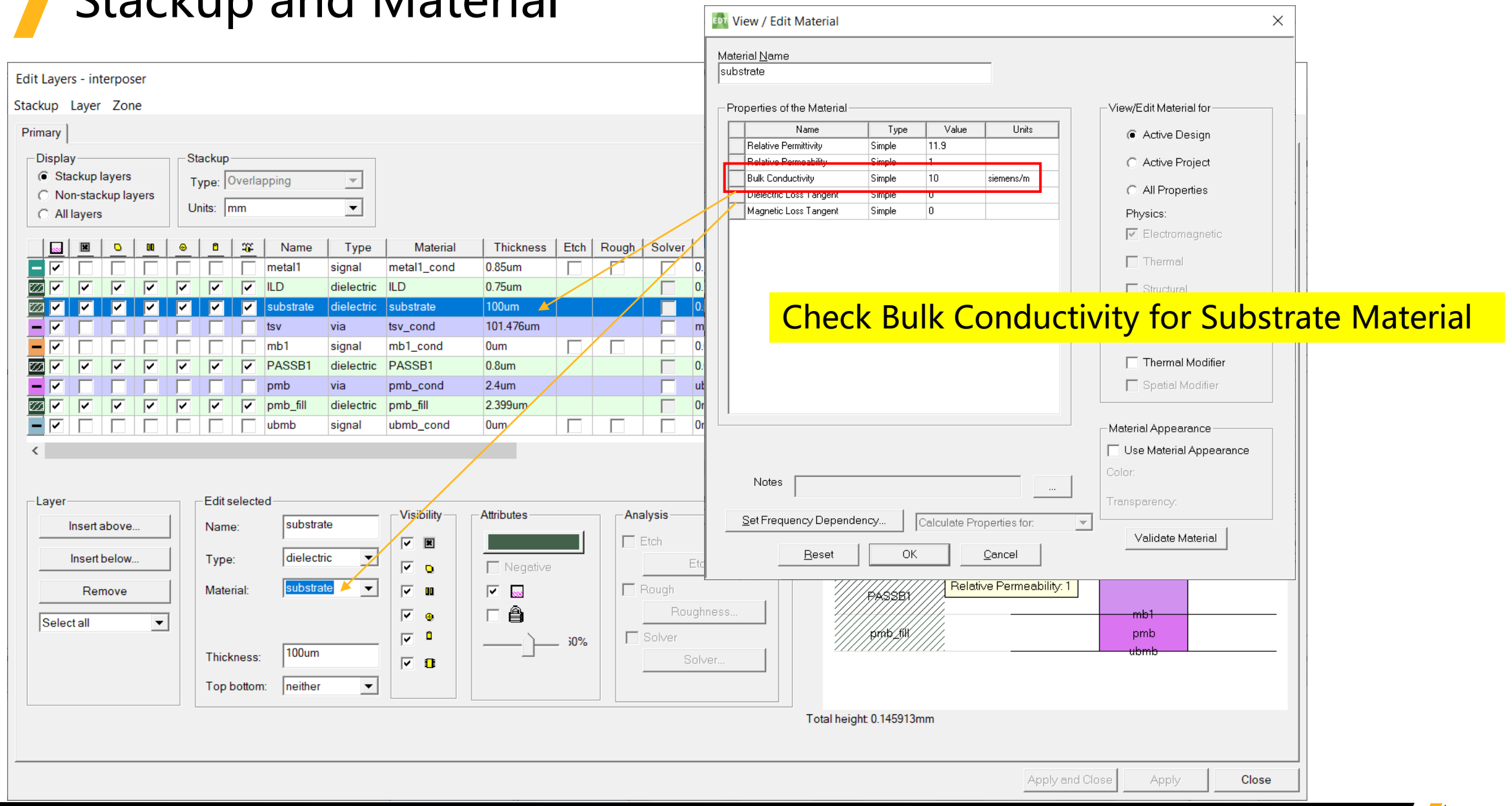


Click "Generate" to generate EBD and AEDT file according settings.

Imported Project

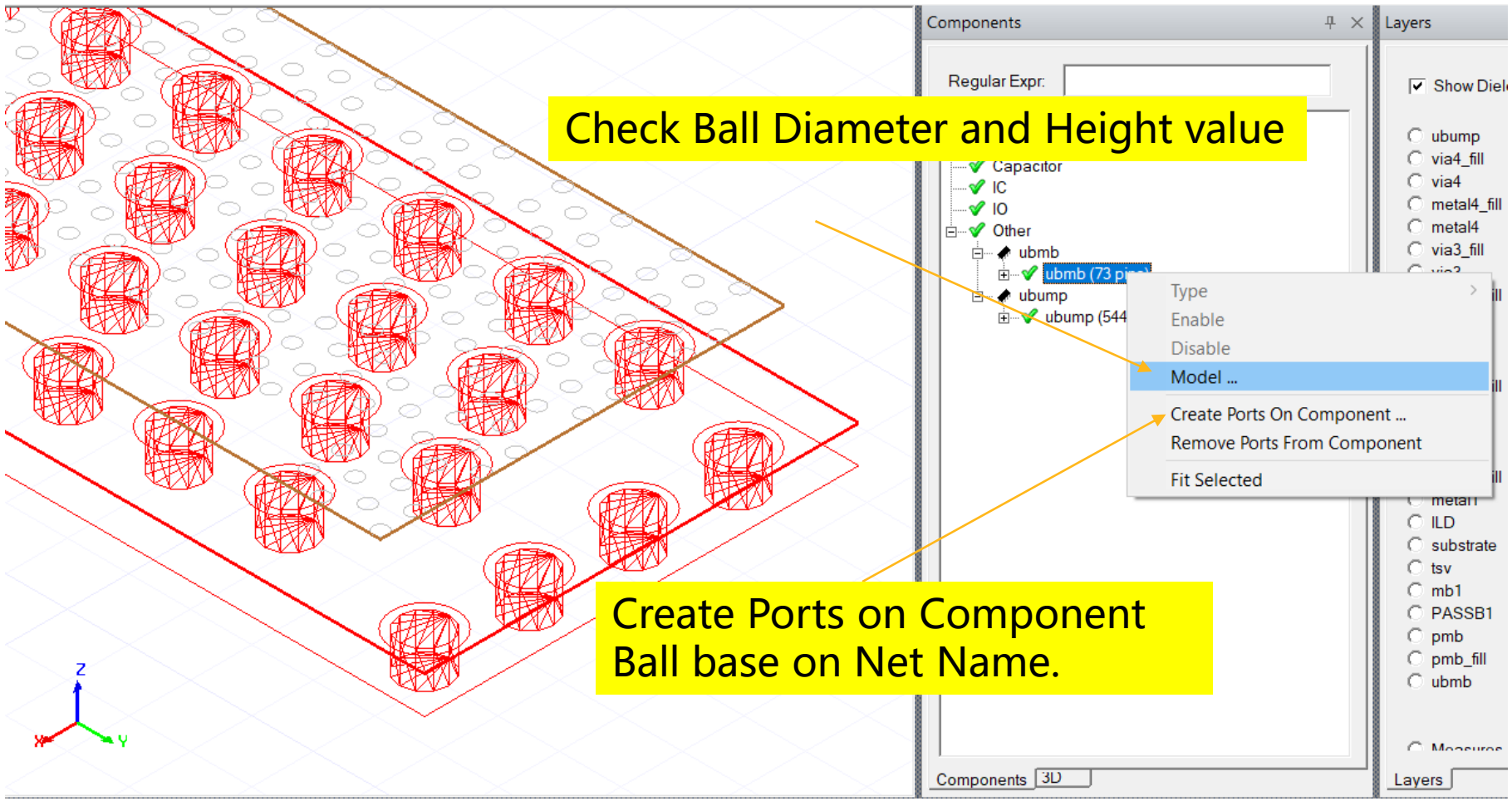


Stackup and Material



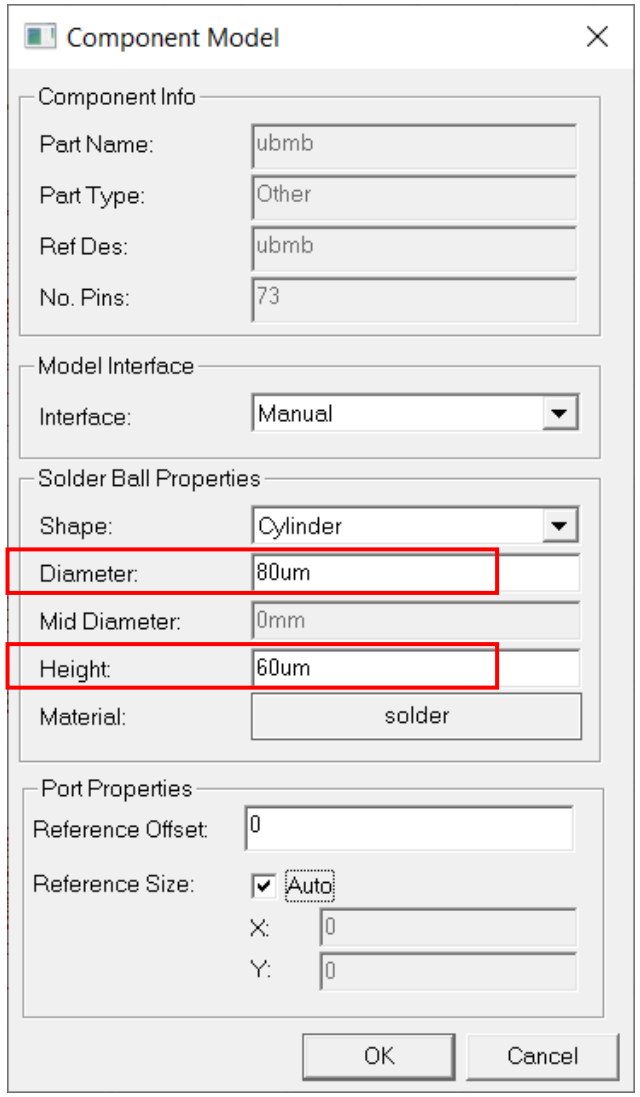
Check Bulk Conductivity for Substrate Material

Component solder ball and port

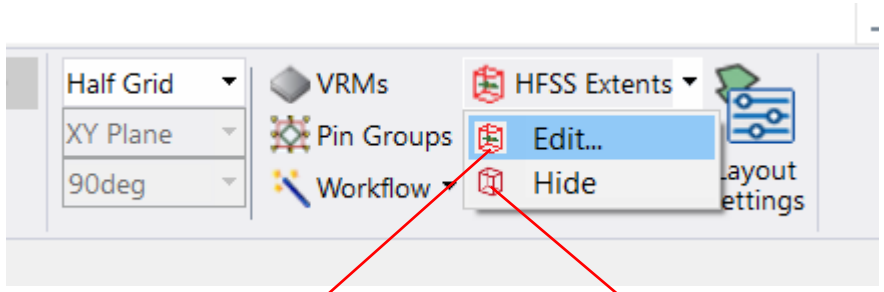


Check Ball Diameter and Height value

Create Ports on Component Ball base on Net Name.

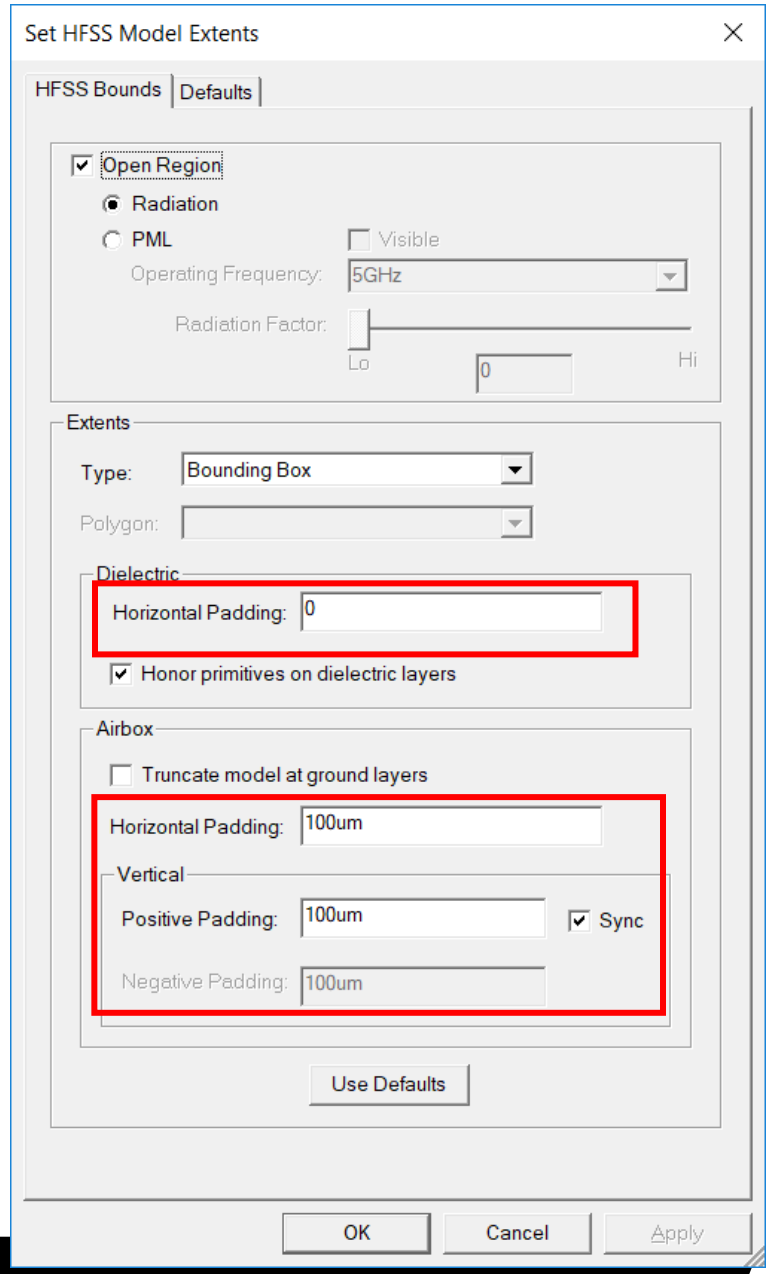


Set HFSS Model Extents(Airbox)

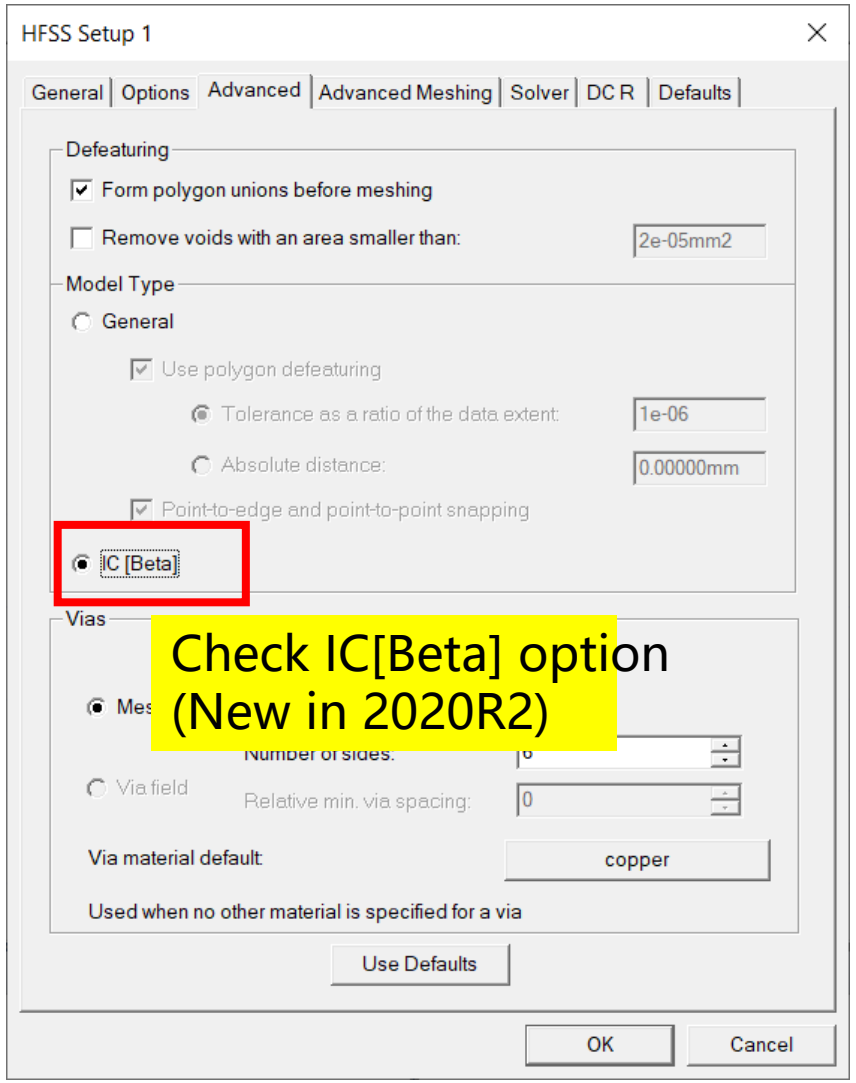


Edit Airbox

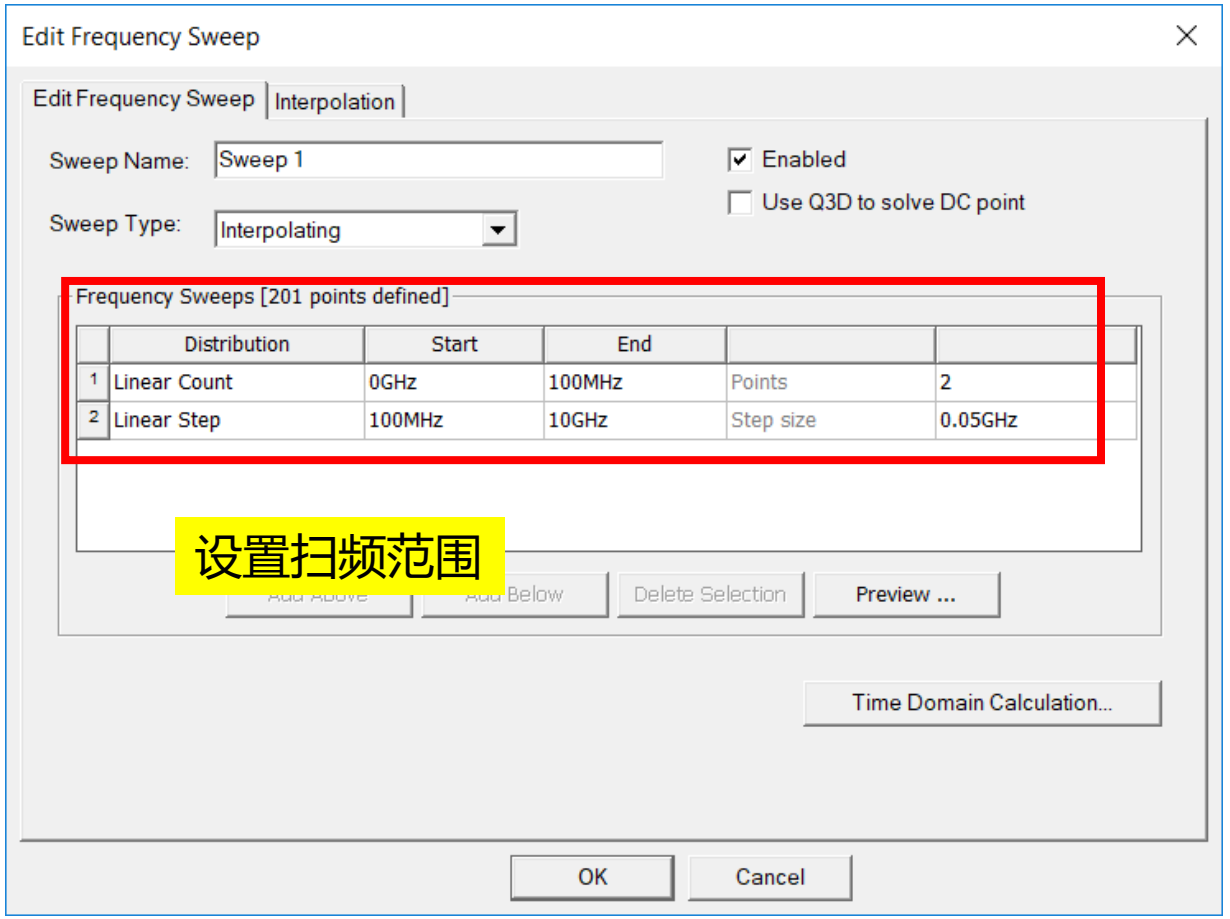
Show Airbox



HFSS Setup

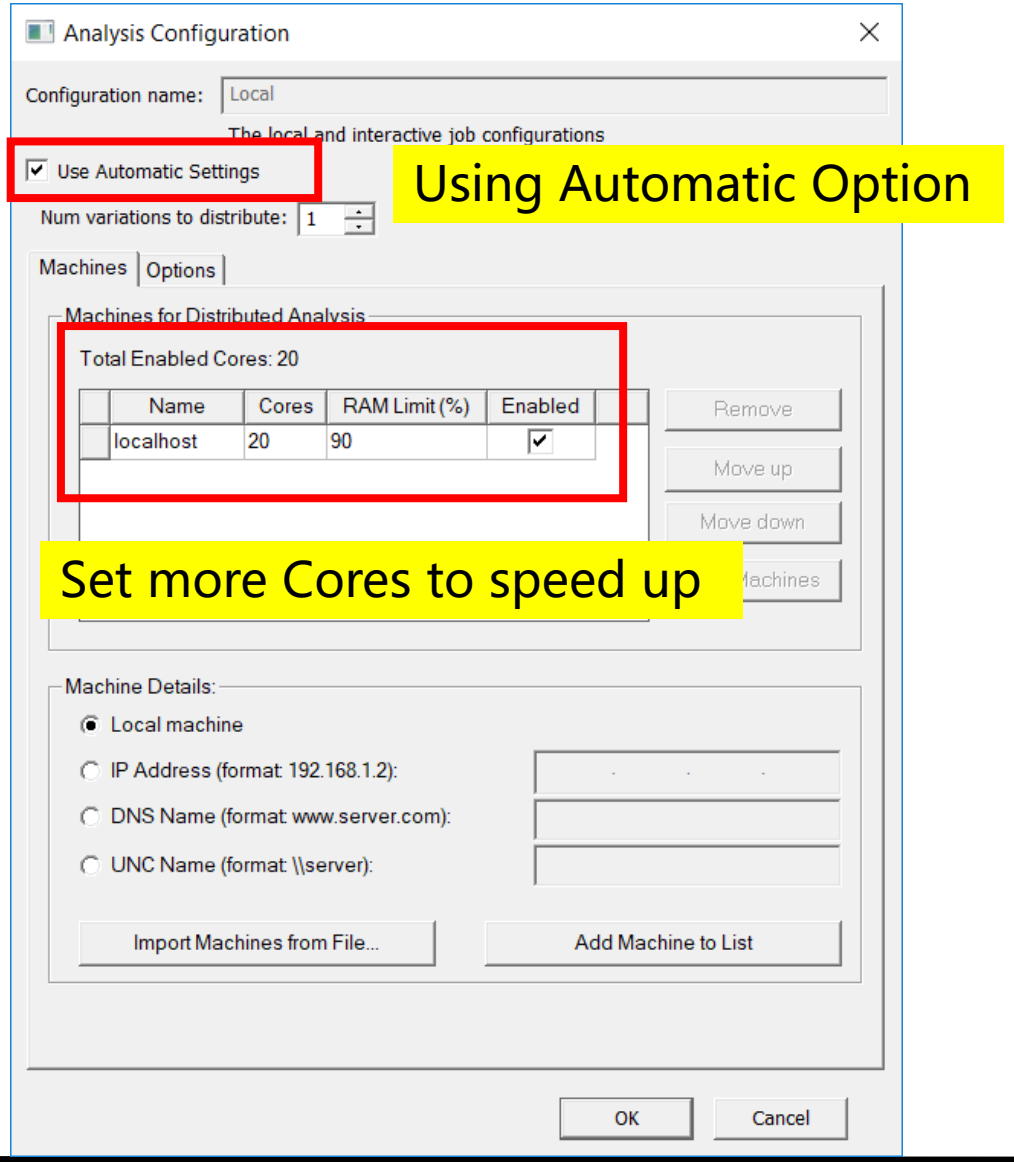


Check IC[Beta] option
(New in 2020R2)



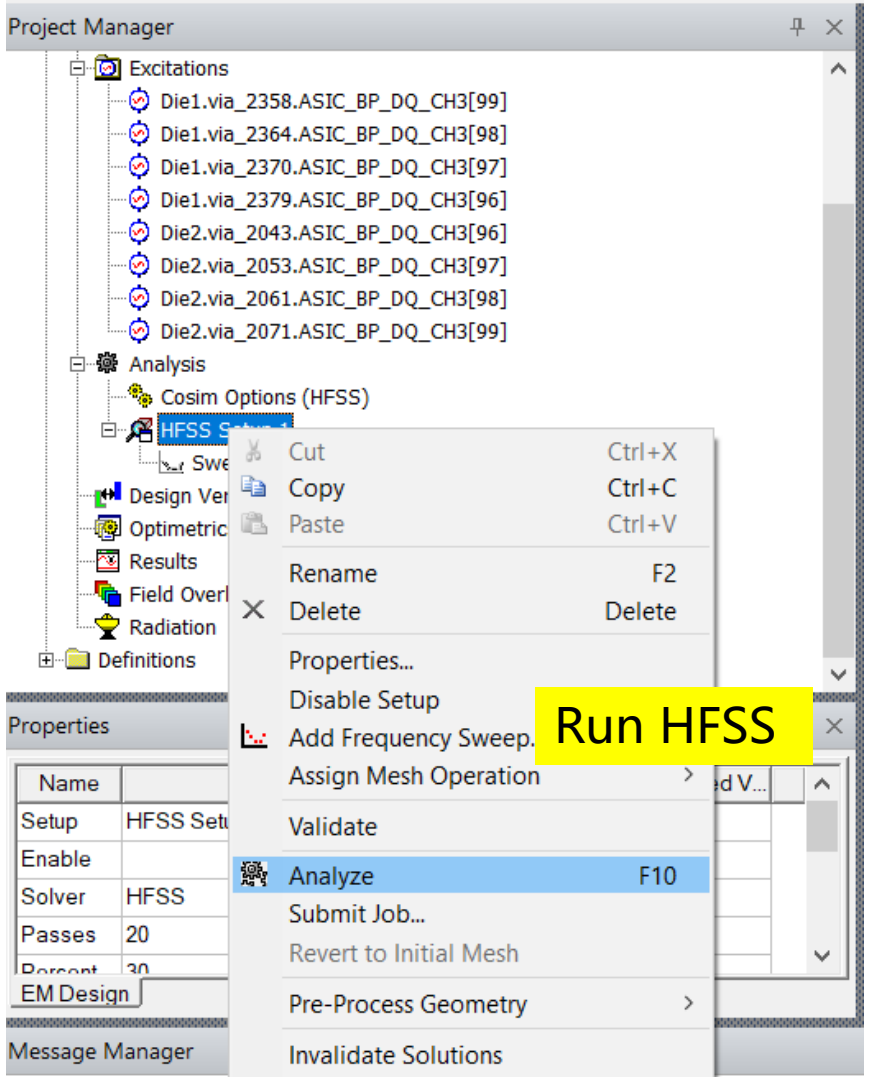
设置扫频范围

Run Simulation



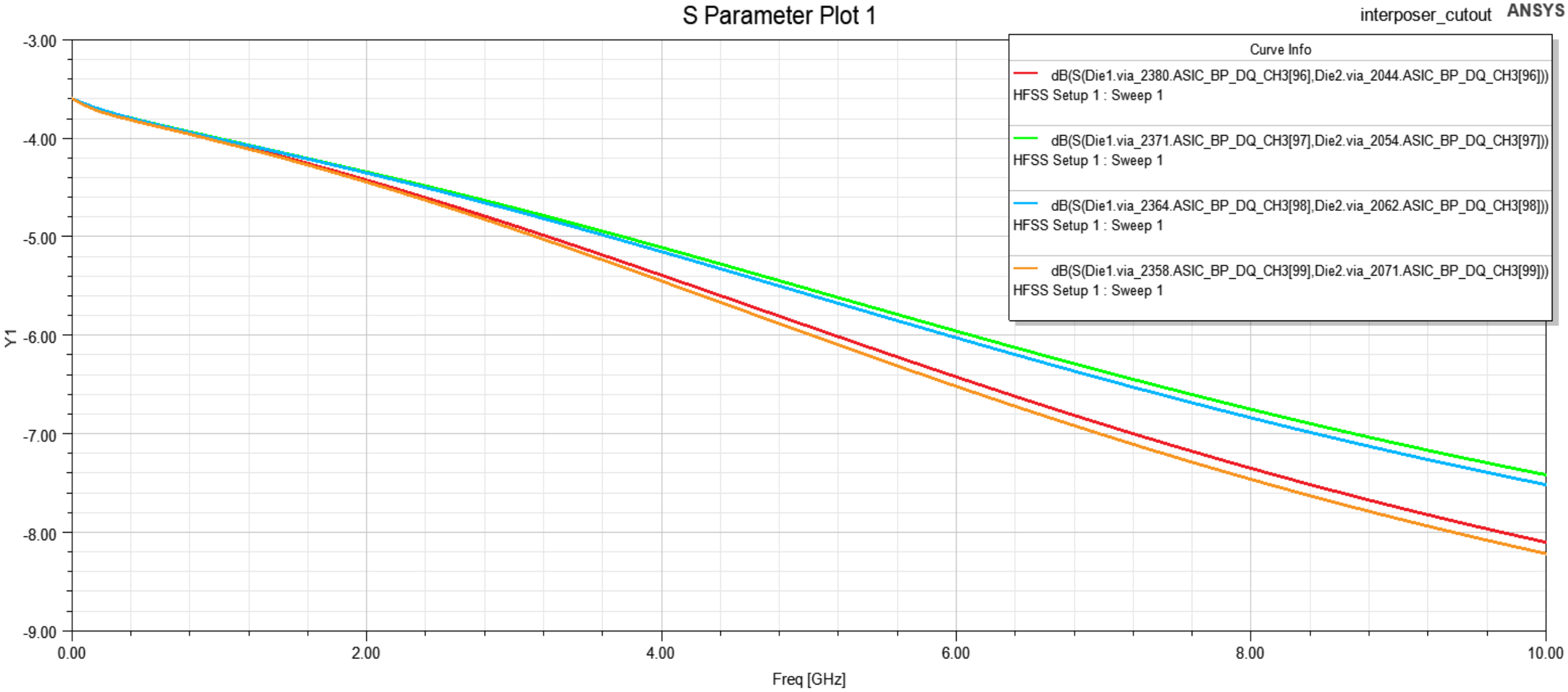
Using Automatic Option

Set more Cores to speed up



Run HFSS

HFSS


S Parameter Plot 1
interposer_cutout
ANSYS
Curve Info
dB(S(Die1.via_2380.ASIC_BP_DQ_CH3[96],Die2.via_2044.ASIC_BP_DQ_CH3[96]))
HFSS Setup 1 : Sweep 1
dB(S(Die1.via_2371.ASIC_BP_DQ_CH3[97],Die2.via_2054.ASIC_BP_DQ_CH3[97]))
HFSS Setup 1 : Sweep 1
dB(S(Die1.via_2364.ASIC_BP_DQ_CH3[98],Die2.via_2062.ASIC_BP_DQ_CH3[98]))
HFSS Setup 1 : Sweep 1
dB(S(Die1.via_2358.ASIC_BP_DQ_CH3[99],Die2.via_2071.ASIC_BP_DQ_CH3[99]))
HFSS Setup 1 : Sweep 1
-3.00
-4.00
-5.00
-6.00
-7.00
-8.00
-9.00
Y1
0.00
2.00
4.00
6.00
8.00
10.00
Freq [GHz]

Running in Batch Mode

Running in batch mode - Windows

Return

- *set aedtInstallPath=C:\Program Files\AnsysEM\AnsysEM20.2\Win64*
- *set gdsPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.gds*
- *set ircxPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\TSMC_INTERPOSER.ircx*
- *set path=%aedtInstallPath%\common\IronPython;%path%*
- *ipy64 GDSImportWizard.py -batch*

- Optional Setting
- set netlistPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.net
- set xmlPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.xml
- set edbPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.aedb

Running in batch mode - Linux

Return

- *export aedtInstallPath='/home/ansys/app/AnsysEM20.1/Linux64'*
- *export gdsPath=/home/ansys/yguo/test/test.gds*
- *export ircxPath=/home/ansys/yguo/test/TSMC_INTERPOSER.ircx*
- *export ipy64="$aedtInstallPath/common/mono/Linux64/bin/mono $aedtInstallPath/common/IronPython/ipy64.exe"*
- *$ipy64 GDSImportWizard.py -batch*

- Optional Setting
- export netlistPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.net
- export xmlPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.xml
- export edbPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.aedb


Ansys