

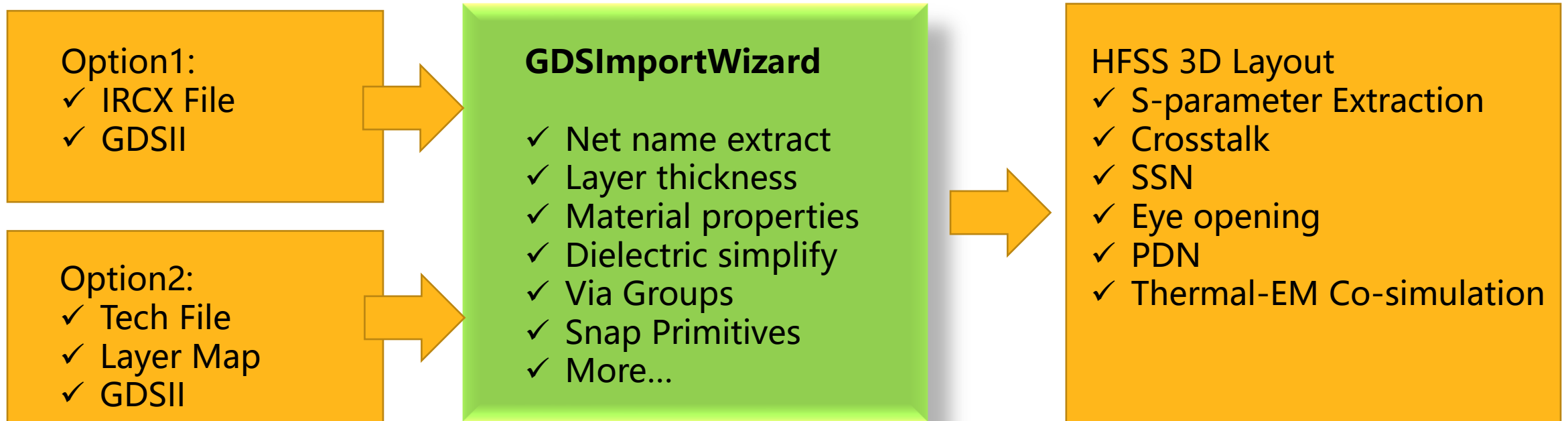


GDS Import Wizard 2.0使用手册

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/ GDS Import Wizard Workflow



/ Getting the latest GDSImportWizard Tool

<https://github.com/YongshengGuo/GDSImportWizard/releases/latest>

The screenshot shows the GitHub repository page for **YongshengGuo / GDSImportWizard**. The navigation bar includes links for Code, Issues, Pull requests, Actions, Projects, Wiki, Security, Insights, and Settings. The **Releases** tab is selected, and an arrow points to it with the text "Click Releases to download earlier version".

On the left sidebar, there is a "Latest release" badge, a commit hash "55fcee7", a "Verified" badge, and a "Compare" dropdown.

The main content area displays the release title **GDSImportWizard Verxx** and the message "YongshengGuo released this 1 hour ago". Below this, the "Assets" section shows two items:

- Source code (zip)**: This asset is highlighted with a red rectangular box. An arrow points from a yellow box labeled "Getting From here!" to this asset.
- Source code (tar.gz)**

Add GDSImportWizard to AEDT

ANSYS Electronics Desktop 2020 R2 - Project40

File Edit View Project Tools Window Help

Tools menu options:

- Edit Libraries
- Library Tools
- Project Tools
- Run Script...
- Pause Script
- Record Script To File...
- Record Script to Project...
- Open Command Window
- Password Manager...
- Debug Logging...
- Stop Debug Logging
- Options
- Keyboard Shortcuts...
- External Tools... (1)
- Show Queued Simulations
- Edit Active Analysis Configuration...
- Import Array from Table...
- Job Management
- Calibration Wizard
- Chip Model Analyzer (CMA)
- Layout Links...
- Network Data Explorer
- PFmag...
- GDSImportWizard (5)

Customize User Tools Menu dialog:

- Menu Contents: GDSImportWizard, HBM Workflow
- Menu Text: GDSImportWizard
- Command: ;2XML_V 3\GDSImportWizard.py ... (3)
- Initial Directory: (4)
- Buttons: Add (2), Remove, Move Up, Move Down

Select Program dialog:

- File name: GDSImportWizard.py
- File type: IronPython Script Files (*.py)
- Buttons: Open, Cancel

5 Open GDSImportWizard from here!

Step1: Define Technology File

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Suggestion

☒ TSMC IRCX

TSMC IRCX

Option 1: Using TSMC IRCX File

☐ LayerMap+TechFile

LayerMap

TechFile

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

☐ TSMC IRCX

TSMC IRCX

☒ LayerMap+TechFile

LayerMap

TechFile

Option 2: Use Apache layermap and Techfile

What about IRCX

IRCX is an EDA data format for interconnect modeling with TSMC's 65- and 40-nm process technologies.

Include:

- ✓ Layer Mapping
- ✓ Layer Thickness
- ✓ Layer Material property

Application:

- ✓ RC parasitic extraction,
- ✓ electromigration analysis,
- ✓ power integrity analysis, and
- ✓ electromagnetic simulation

```
96 [RC SPICE INFORMATION]
97 LAYER {
98 * STACK 34 4 (NAME:V, MEASURED_FROM:V, HEIGHT:V, THICKNESS:V)
99 FIELD      MEASURED_FROM  HEIGHT  THICKNESS
100 NAME
101 ubump      UF1           142.639000  0.001000
102 UF1        PASS4         107.640000  35.000000
103 PASS4      PASS3b        107.040000  0.600000
104 PASS3b     PASS3a        106.640000  0.400000
105 PASS3a     PASS2         105.190000  1.450000
106 metal4     PASS2         105.190000  1.450000
107 PASS2      PASS1         104.490000  0.700000
108 PASS1      IMD3c         104.415000  0.075000
109 IMD3c      IMD3b         103.690000  0.725000
110 IMD3b      IMD3a         103.640000  0.050000
111 metal3     IMD3a         103.565000  0.850000
112 IMD3a      IMD2g         103.020000  0.620000
113 IMD2g      IMD2f         102.970000  0.050000
114 IMD2f      IMD2e         102.245000  0.725000
115 IMD2e      IMD2d         102.195000  0.050000
116 metal2     IMD2d         102.120000  0.850000
117 IMD2d      IMD2c         101.873000  0.322000
118 IMD2c      IMD2b         101.793000  0.080000
119 ctm         IMD2b         101.793000  0.080000
120 IMD2b      IMD2a         101.775000  0.018000
121 IMD2a      IMD1c         101.575000  0.200000
122 cbm         IMD1c         101.575000  0.200000
123 IMD1c      IMD1b         101.525000  0.050000
124 IMD1b      IMD1a         100.800000  0.725000
125 IMD1a      ILD           100.750000  0.050000
126 metal1     ILD           100.675000  0.850000
127 ILD        substrate     100.000000  0.750000
128 substrate  PASSB1         0.000000  100.000000
129 PASSB1     PASSB2b        -0.800000  0.800000
130 mb1         PASSB2b        -0.801000  0.001000
131 PASSB2b    PASSB2a        -2.800000  2.000000
132 PASSB2a    underFill_C    -3.200000  0.400000
133 underFill_C N/A           -3.201000  0.001000
134 ubmb       N/A           -3.201000  0.001000
135
```

```
[LAYER_MAPPING]
#substate is reversed-tone NWELL
#via4 is (ubump AND metal4)
#ubump_top_pin is ubump_pin
#ubmb_top_pin is ubmb_pin
#RC      GDS  LVS      DFII
ubump      170;0      ubump      UBM;drawing
metal4      74;0      metal4      AP;drawing
DUM4        74;1      DUM4        AP;dummy
metal3      33;40     metal3      M3;drawing
DUM3        33;41     DUM3        M3;dummy
metal2      32;40     metal2      M2;drawing
DUM2        32;41     DUM2        M2;dummy
metal1      31;40     metal1      M1;drawing
DUM1        31;41     DUM1        M1;dummy
mb1         31;100    MB1         M1;BSL
ubmb        170;100   UBMB        UBM;BSL
via4         86;0     via4         CB2;drawing
via3         85;0     via3         RV;drawing
via2         52;40     via2         VIA2;drawing
vial         51;40     vial         VIA1;drawing
tsv          251;0     tsv          TSV;drawing
tsv_3t       251;3     tsv_3t       TSV;dummy1
pmb          5;100     PMB          PM;dummy
ubump_pin    125;0     ubm_top_pin   UBM;pin
metal4_pin   126;0     metal4_pin    AP;pin
metal3_pin   133;0     metal3_pin    M3;pin
metal2_pin   132;0     metal2_pin    M2;pin
metal1_pin   131;0     metal1_pin    M1;pin
mb1_pin      131;100   MB1_pin      M1;BSP
ubmb_pin     125;100   UBMB_pin     UBM;test0
ctm          77;0     ctm          CTM;drawing
cbm          88;0     cbm          CBM;drawing
ctm_via      51;40     ctm_via      VIA1;drawing
cbm_via      51;40     cbm_via      VIA1;drawing
```

Step2: Extract Nets information from GDSII

GDSII Import Wizard

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD Help

Extract Nets From GDS

GDSII Browse

NetLayerMap Update

NetRegular

Extract Net Extract Edit

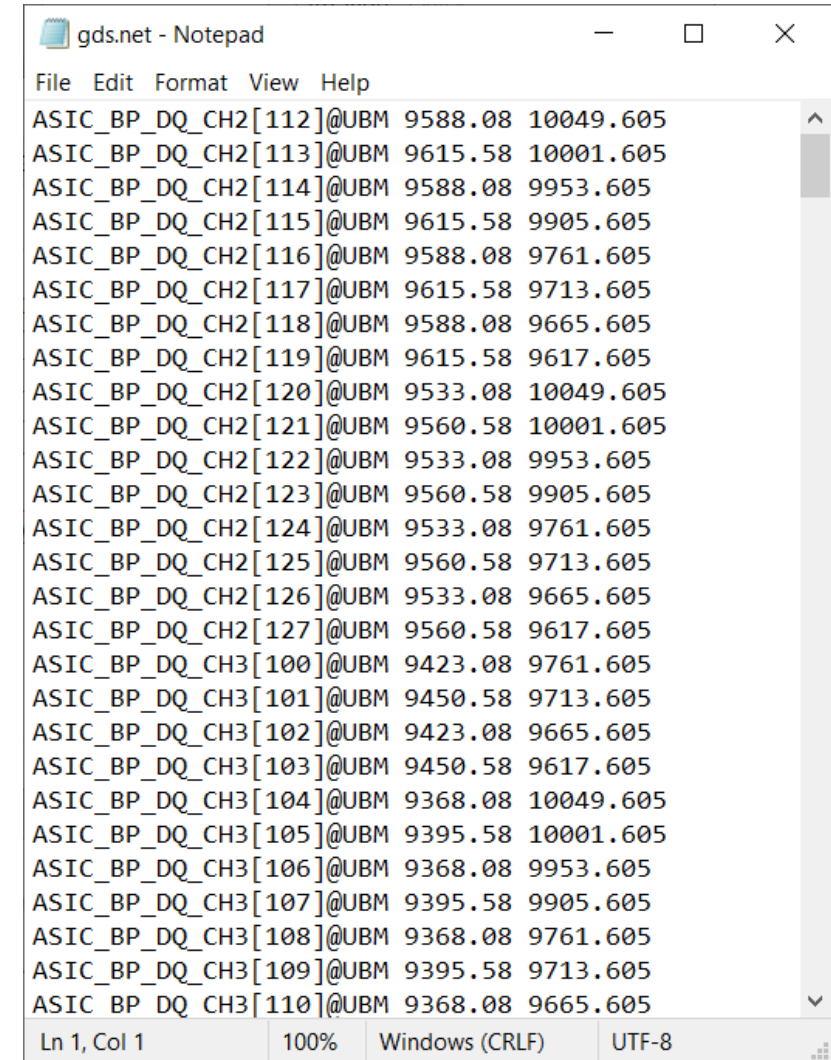
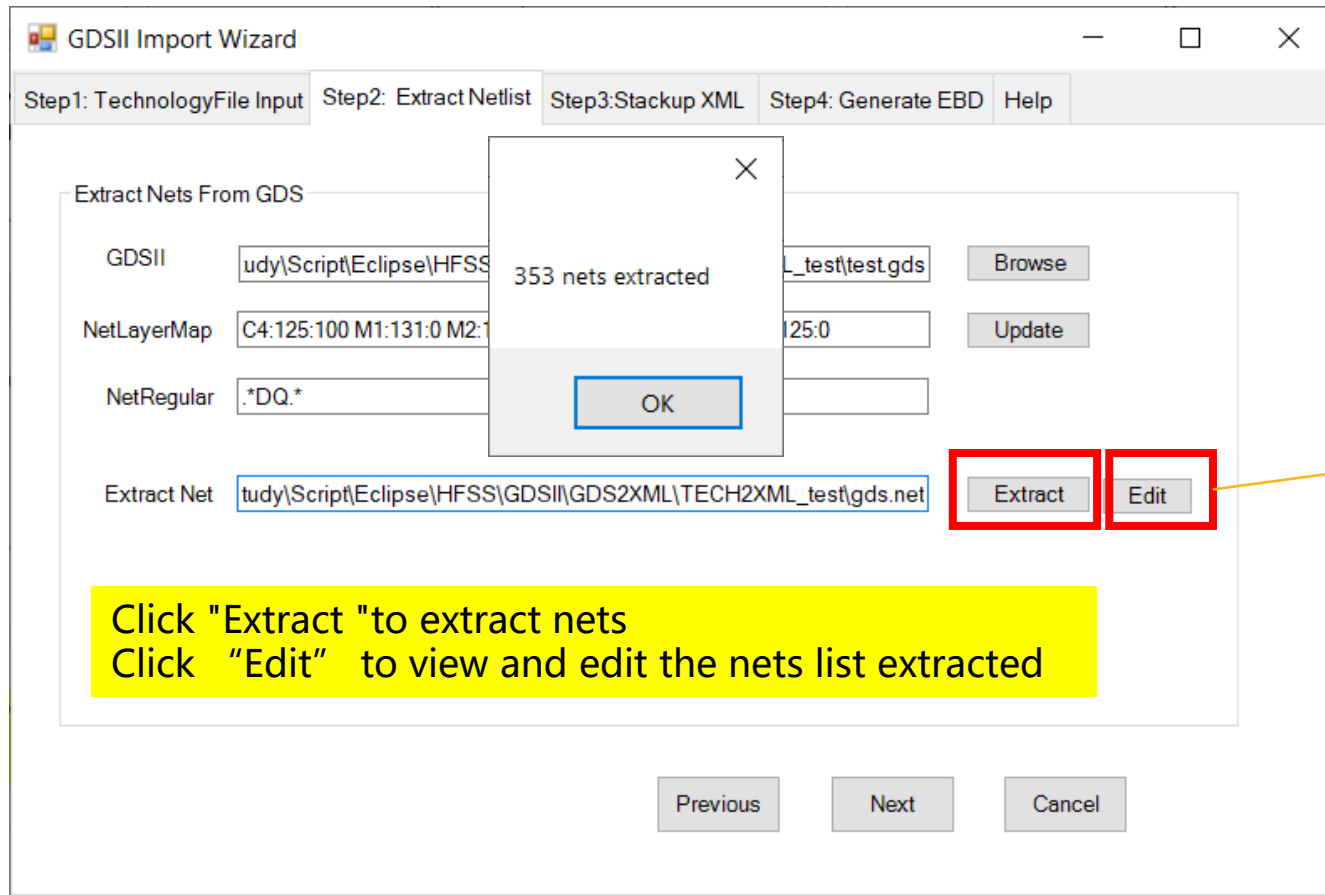
Previous Next Cancel

Select GDS File

NetLayerMap: GDS Layer include net information, click "Update" button to extract from layermap or IRCX.

NetRegular: Using regular expressions to filter nets extracted. Default is extracted all nets.

Step2: Extract Nets information from GDSII



Step3: Generate Stackup XML (Control file)

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML

☒ CreateViaGroups

MergeMethod ☒ NoMergeOnTSV

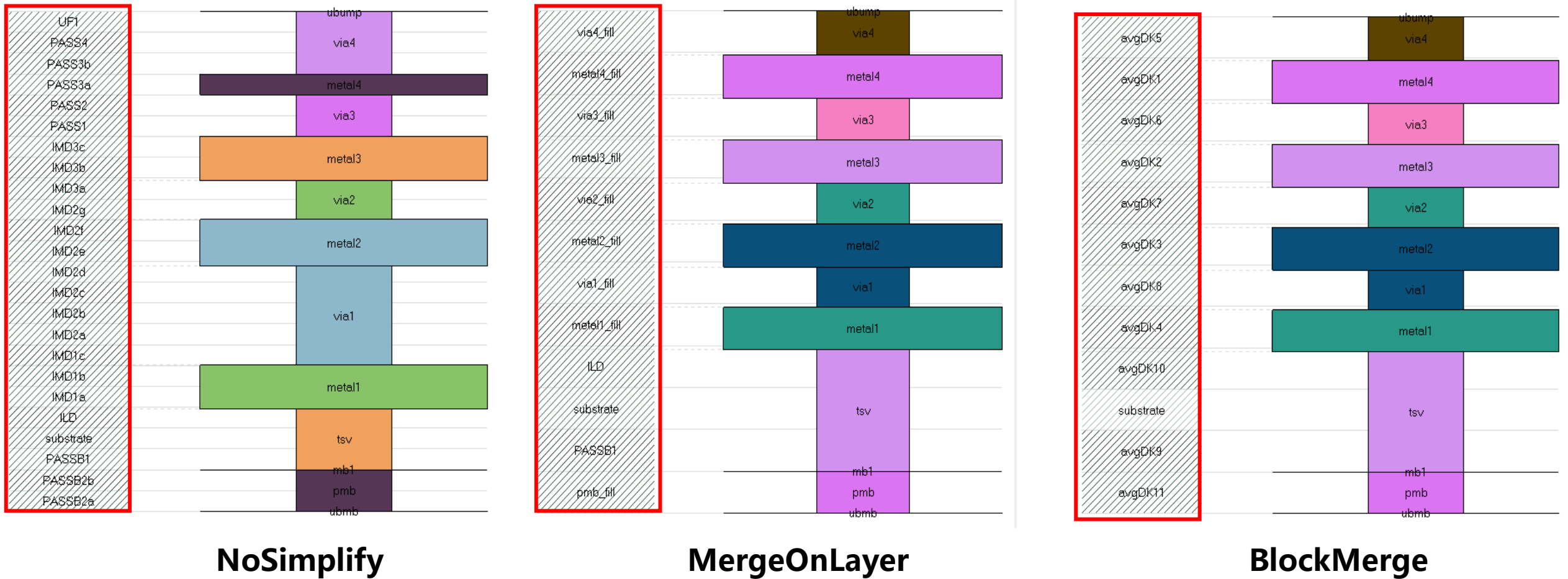
☐ LegacyXml(Laminate) ☐ UseDefaultDF

Previous Next Cancel

Simplify Dielectric Method:
NoSimplify: No Merge on Dielectric
MergeOnLayer: Merge Dielectric on each conduct layer
BlockMerge: use average DK on each conduct (except SI material)

Step3: Generate Stackup XML (Control file)

- Simplify Dielectric Method compare



Step3: Generate Stackup XML (Control file)

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML

Generate Stackup XML

Stackup XML D:\Study\Script\repository\HFSS\GDSII\GDS2XML\TECH

SimplifyDielectric BlockMerge ☒ CreateViaGroup

MergeMethod **Weighted Average** ☒ NoMergeOnTS

☐ LegacyXml(Laminates) ☐ UseDefaultDF

Weighted Capacitance

Weighted Average

Previous

Method	Equation
Weighted Capacitance	$\epsilon_{r_merged} = \frac{\sum_{i=1}^n h_i}{\sum_{i=1}^n \frac{h_i}{\epsilon_i}}$
Weighted Average	$\epsilon_{r_merged} = \frac{\sum_{i=1}^n h_i \epsilon_i}{\sum_{i=1}^n h_i}$

There are Kraszewski (Kraszewski equation)

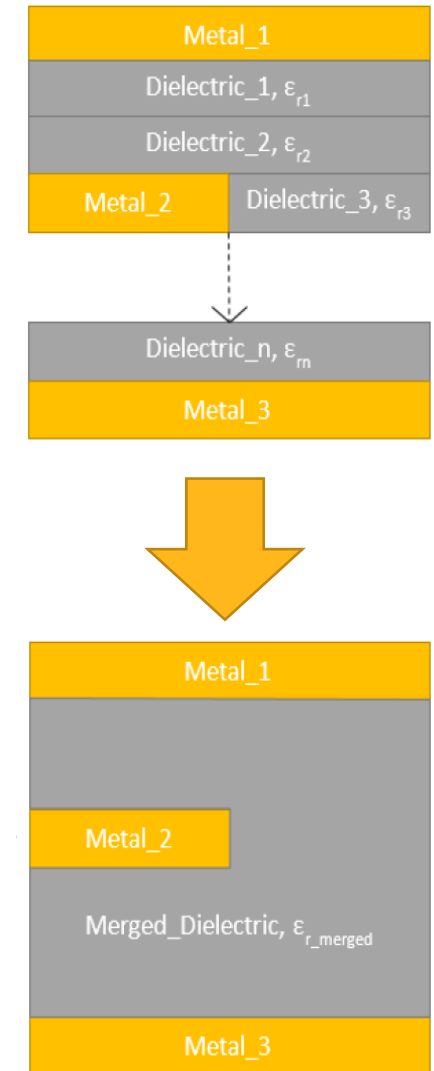
$$\sqrt{\epsilon^*} = v_1 \sqrt{\epsilon_1} + v_2 \sqrt{\epsilon_2} + v_3 \sqrt{\epsilon_3} \quad (1)$$

Landau, Lifshitz and Looyenga, (Landau equation)

$$\sqrt[3]{\epsilon^*} = v_1 \sqrt[3]{\epsilon_1} + v_2 \sqrt[3]{\epsilon_2} + v_3 \sqrt[3]{\epsilon_3} \quad (2)$$

Lichtenecker, (Lichtenecker equation)

$$\ln \epsilon^* = v_1 \ln \epsilon_1 + v_2 \ln \epsilon_2 + v_3 \ln \epsilon_3 \quad (3)$$



Merge Dielectric Method selection.

Merge Dielectric

Note: Merge Dielectric also can be done in 3d Layout stackup editor.

Step3: Generate Stackup XML (Control file)

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

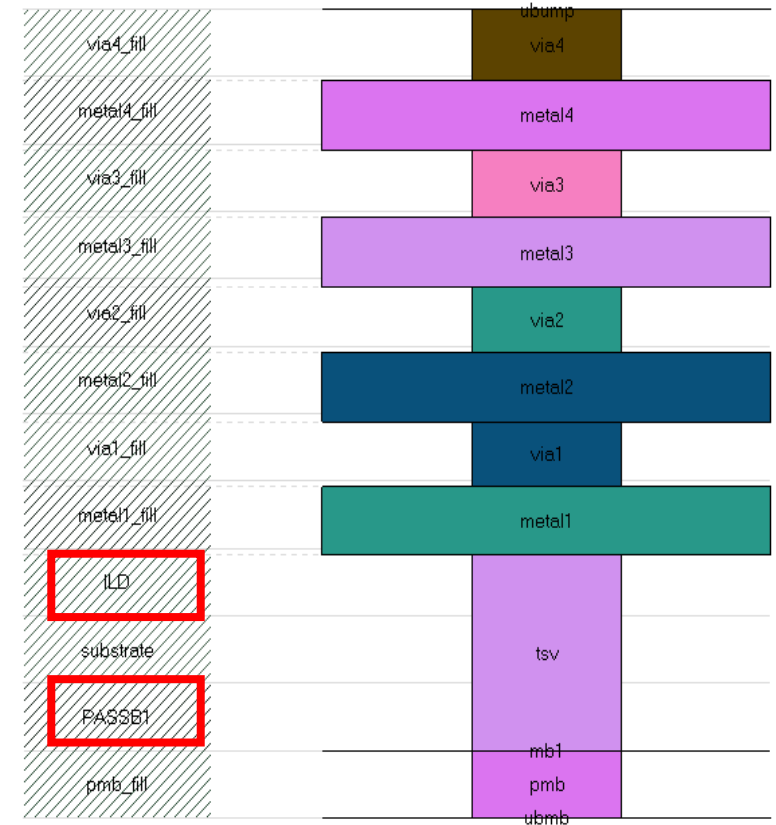
Stackup XML

SimplifyDielectric ☒ CreateViaGroups

MergeMethod ☒ NoMergeOnTSV

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Keep Insulating layer above and below SI Substrate when Simplify Dielectric.



Step3: Generate Stackup XML (Control file)

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

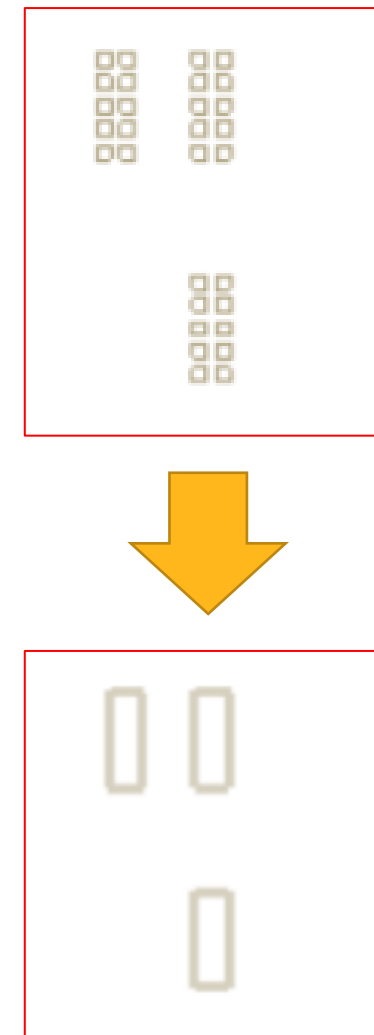
Stackup XML

SimplifyDielectric ☒ CreateViaGroups

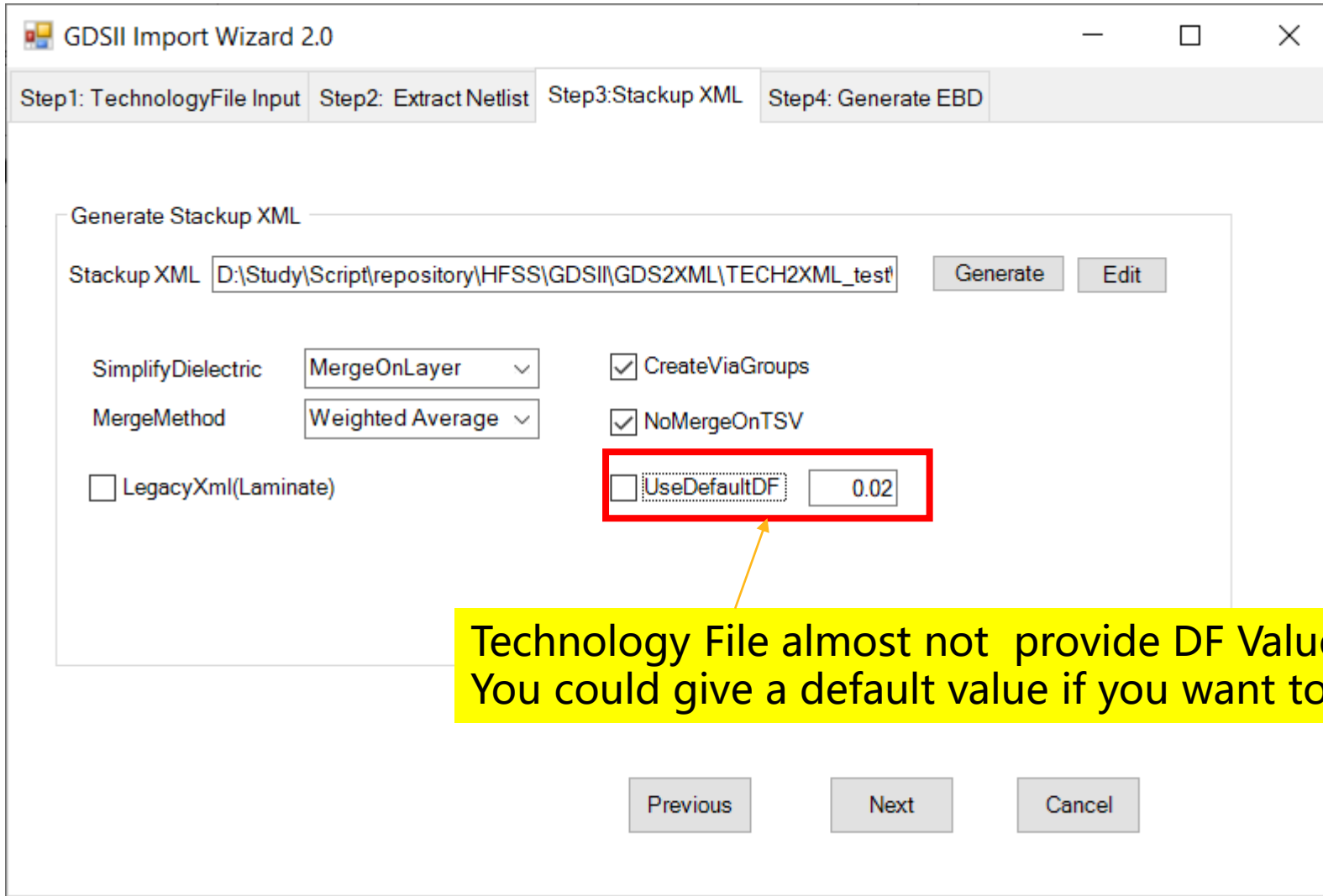
MergeMethod ☒ NoMergeOnTSV

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Automatic create via groups on via layers.



Step3: Generate Stackup XML (Control file)



GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML

SimplifyDielectric ☒ CreateViaGroups

MergeMethod ☒ NoMergeOnTSV

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Technology File almost not provide DF Value for all material. You could give a default value if you want to at here.

Step3: Generate Stackup XML (Control file)

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

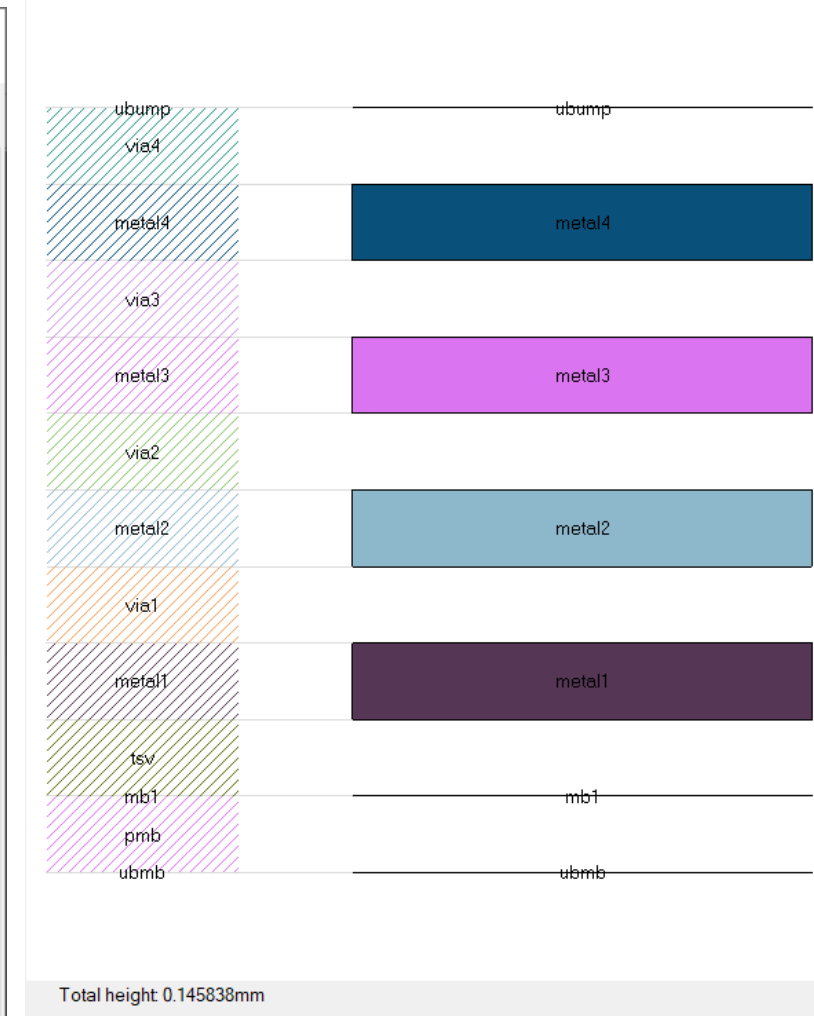
Stackup XML: `F:\SS\GDSII\GDS2XML\TECH2XML_test\TSMC-GDS-XML\legacy.xml` Generate Edit

SimplifyDielectric: MergeOnLayer ▼ ☒ CreateViaGroups

MergeMethod: Weighted Average ▼ ☒ NoMergeOnTSV

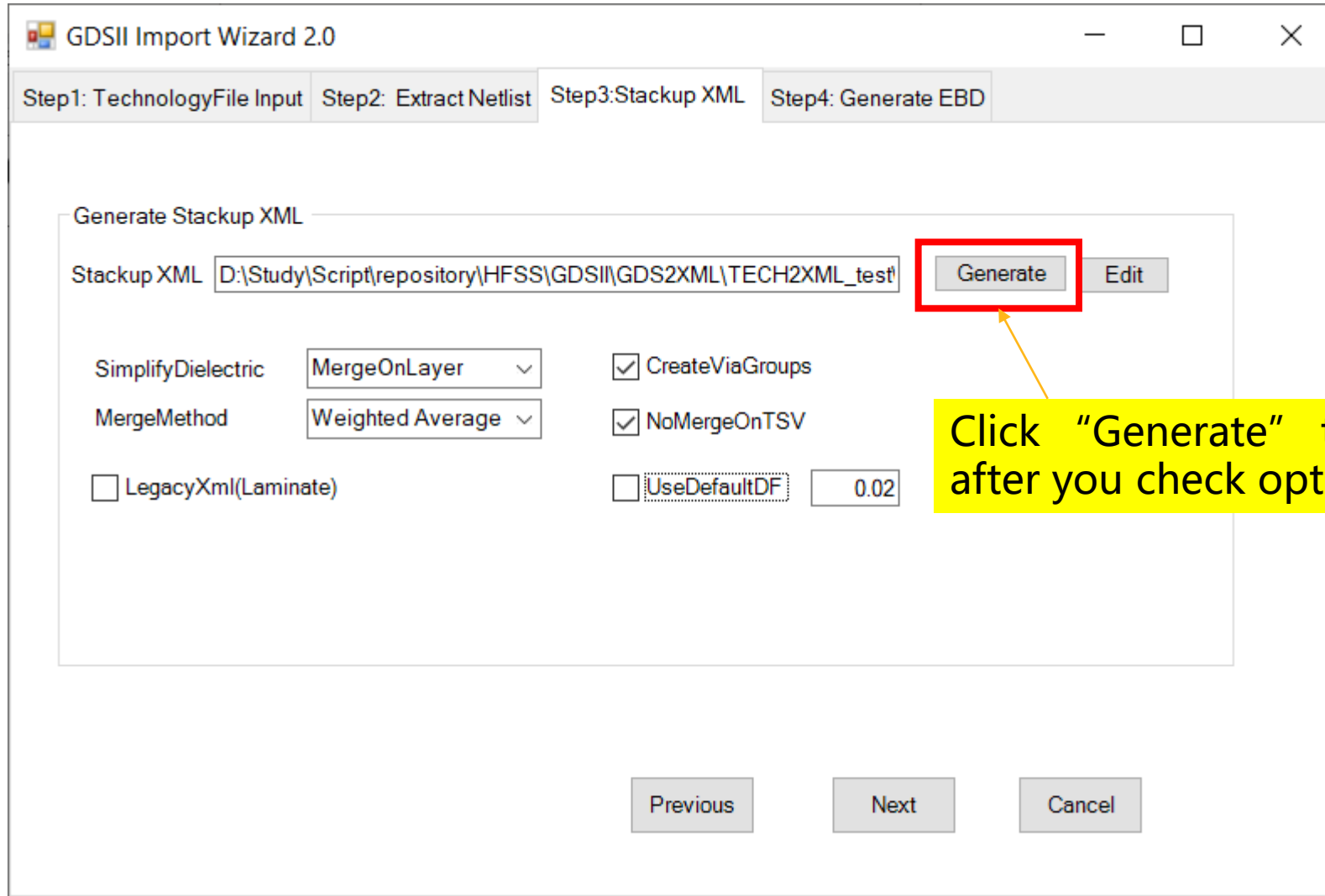
☒ LegacyXml(Laminate) ☐ UseDefaultDF 0.02

Previous Next Cancel



By default, GDSImportWizard generate Overlapping stackup which could create ViaGroups automatically.

Step3: Generate Stackup XML (Control file)



GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML

SimplifyDielectric ☒ CreateViaGroups

MergeMethod ☒ NoMergeOnTSV

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Click "Generate" to generate Control xml after you check options.

Step4: Generate EBD

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

AEDT Installed Dir C:\Program Files\AnsysEM\AnsysEM20.2\Win64 Browse

EBD File Generate

☒ Import to AEDT ☒ Auto Generate Component

☒ Add TSV Insulator Ring 1e-6

Open ECADExplorer Open in AEDT

Previous Finished Cancel

Pull down and Select AEDT version (installed)

When checked, EBD will import to AEDT after generated

Step4: Generate EBD

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

AEDT Installed Dir: C:\Program Files\AnsysEM\AnsysEM20.2\Win64 Browse

EBD File: Generate

☒ Import to AEDT ☒ Auto Generate Component

☒ Add TSV Insulator Ring 1e-6

Open ECADExplorer Open in AEDT

Previous Finished Cancel

Components will be added on first and last layer after EBD import.

Components

Regular Expr:

- ☒ Resistor
- ☒ Inductor
- ☒ Capacitor
- ☒ IC
- ☒ IO
- ☒ Other
 - ☒ ubmb
 - ☒ ubmb (84 pins)
 - ☒ ubump
 - ☒ ubump (270 pins)

Step4: Generate EBD

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

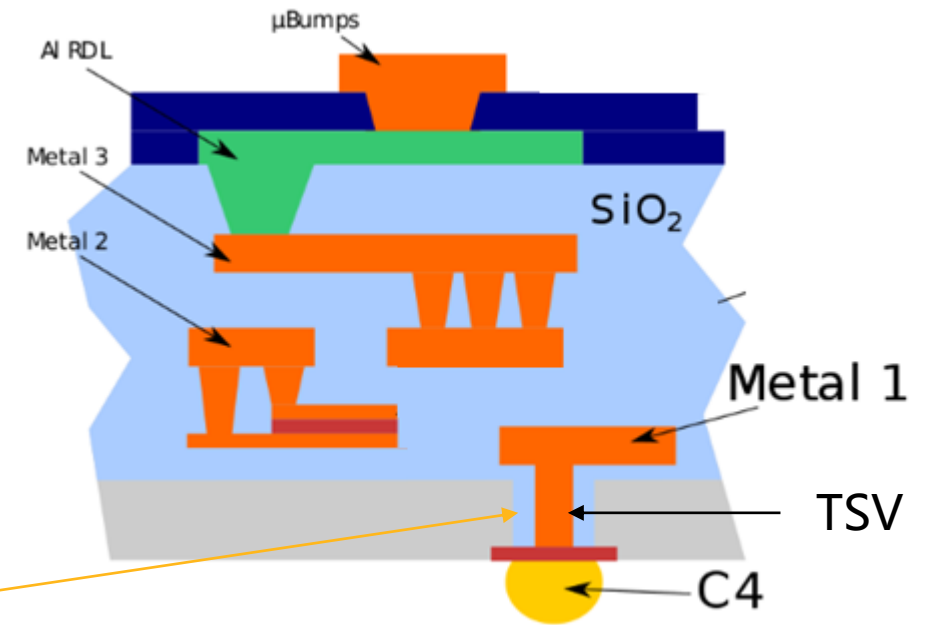
AEDT Installed Dir: C:\Program Files\AnsysEM\AnsysEM20.2\Win64 Browse

EBD File: Generate

☒ Import to AEDT ☒ Auto Generate Component

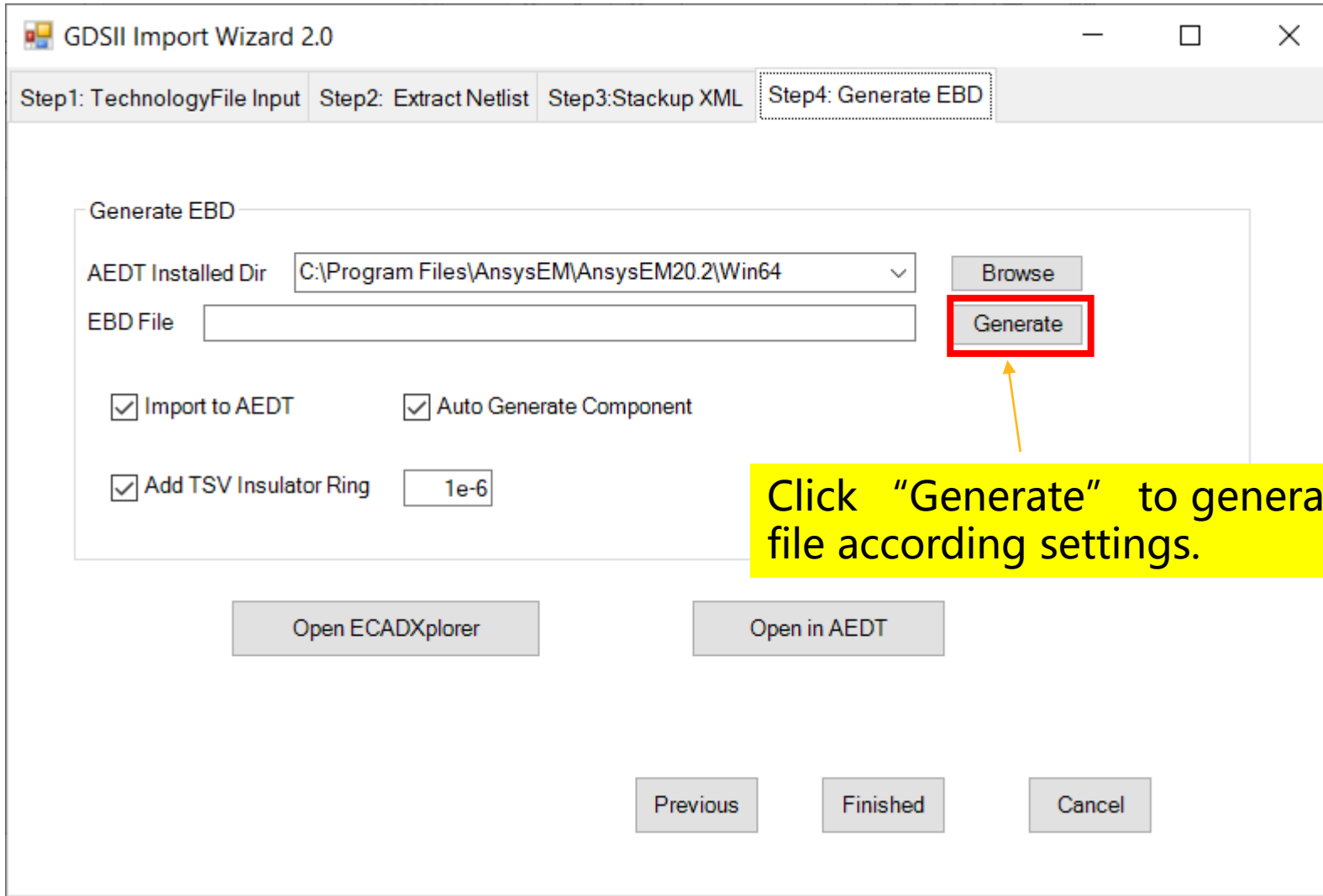
☒ Add TSV Insulator Ring 1e-6

Previous Finished Cancel



TSV Insulator Ring will be added in TSV layer after EBD imported. Ring thickness should be set a purpose value.

Step4: Generate EBD



The screenshot shows the 'GDSII Import Wizard 2.0' window, specifically the 'Step4: Generate EBD' tab. The window has a title bar with standard minimize, maximize, and close buttons. Below the title bar is a tabbed interface with four tabs: 'Step1: TechnologyFile Input', 'Step2: Extract Netlist', 'Step3: Stackup XML', and 'Step4: Generate EBD'. The 'Step4: Generate EBD' tab is active and contains the following elements:

- A section titled 'Generate EBD' containing:
 - 'AEDT Installed Dir': A text box showing 'C:\Program Files\AnsysEM\AnsysEM20.2\Win64' with a dropdown arrow, and a 'Browse' button to its right.
 - 'EBD File': An empty text box.
 - A 'Generate' button, which is highlighted with a red rectangular border and an orange arrow pointing to it from a yellow callout box.
- Four checkboxes with labels:
 - ☒ Import to AEDT
 - ☒ Auto Generate Component
 - ☒ Add TSV Insulator Ring
 - A text box containing '1e-6' next to the 'Add TSV Insulator Ring' checkbox.
- Two buttons at the bottom: 'Open ECADExplorer' and 'Open in AEDT'.
- Three buttons at the very bottom: 'Previous', 'Finished', and 'Cancel'.

Click "Generate" to generate EBD and AEDT file according settings.

Imported Project

ANSYS Electronics Desktop 2020 R2 - comp - FCCC_Interposer - Layout - [comp - FCCC_Interposer - Layout]

File Edit View Project Draw Layout HFSS 3D Layout Tools Window Help

Save Cut Copy Paste Undo Redo Delete

FCCC_Interposer ubump

Zoom Fit All Fit Selected

Half Grid XY Plane 90deg

Layout Settings

Desktop View Layout Simulation Results Automation

Project Manager

- comp*
- FCCC_Interposer*
- Circuit Elements
- Boundaries
- Excitations
- Analysis
- Cosim Option
- HFSS Custom Setup
- Design Verification
- Optimetrics
- Results
- Field Overlays

Properties

Name	Value
Setup	HFSS Custom Setup
Enable	<input checked="" type="checkbox"/>
Solver	Custom
Passes	10
Percent ...	30
Delta S	0.02
Solution ...	10 GHz

EM Design

Message Manager

comp (D:/Study/Script/repository/HFSS/GDSII/GDS2XML/TECH2XML_test/TSMC-GDS-XML/)

Progress

Layers

Show Dielectrics

- ubump
- via4
- metal4
- via3
- metal3
- via2
- metal2
- via1
- metal1
- via0
- metal0
- via1
- metal1
- via2
- metal2
- via3
- metal3
- via4
- metal4
- via5
- metal5

Measures

Slwave Regions

Rats

Errors

Symbols

Postprocessing

Outline

Components

Nets

Finish your simulation base on the project that imported from GDSImportWizard.

- ✓ Check the stackup thinness and material properties.
- ✓ Clip Design could be done in 3D layout to improve efficiency.
- ✓ If you want use Slwave solver, lagacyXML(Laminate) should be checked in step 3.

Running in batch mode - Windows

- *set aedtInstallPath=C:\Program Files\AnsysEM\AnsysEM20.2\Win64*
- *set gdsPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test2.gds*
- *set ircxPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\TSMC_INTERPOSER.ircx*
- *set path=%aedtInstallPath%\common\IronPython;%path%*
- *ipy64 GDSImportWizard.py -batch*
- Optional Setting
 - *set netlistPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.net*
 - *set xmlPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.xml*
 - *set ebdPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.ebd*

/ Running in batch mode - Linux

- *export aedtInstallPath='/home/ansys/app/AnsysEM20.1/Linux64'*
- *export gdsPath=/home/ansys/yguo/test/test.gds*
- *export ircxPath=/home/ansys/yguo/test/TSMC_INTERPOSER.ircx*
- *export ipy64="\$aedtInstallPath/common/mono/Linux64/bin/mono
\$aedtInstallPath/common/IronPython/ipy64.exe"*
- *\$ipy64 GDSImportWizard.py -batch*
- Optional Setting
- `export netlistPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.net`
- `export xmlPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.xml`
- `export ebdPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.ebd`

 **Ansys**

