GDS Import Wizard 2.0使用手册

Yongsheng.guo@ansys.com

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GDS Import Wizard Workflow

Option1:

- ✓ IRCX File
- ✓ GDSII

Option2:

- ✓ Tech File
- ✓ Layer Map
- ✓ GDSII

GDSImportWizard

- ✓ Net name extract
- ✓ Layer thickness
- ✓ Material properties
- ✓ Dielectric simplify
- ✓ Via Groups
- ✓ Snap Primitives
- ✓ More...



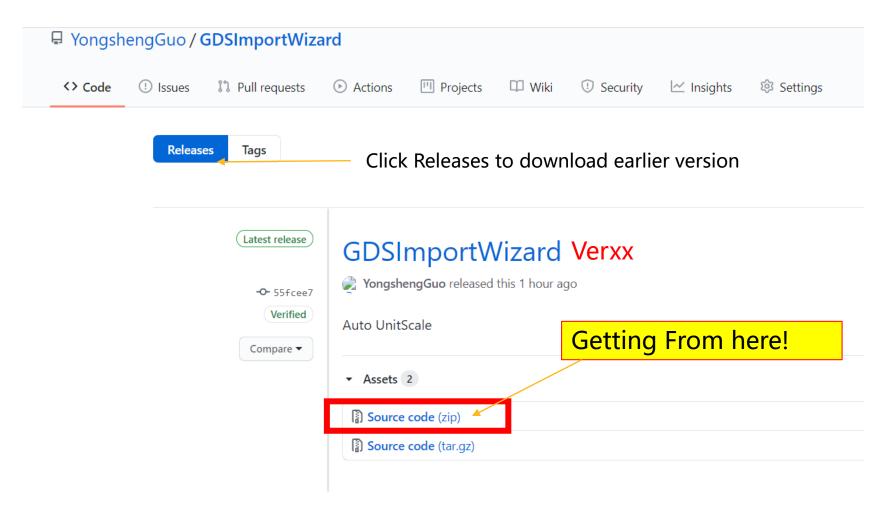
- ✓ S-parameter Extraction
- ✓ Crosstalk
- ✓ SSN
- ✓ Eye opening
- ✓ PDN
- ✓ Thermal-EM Co-simulation



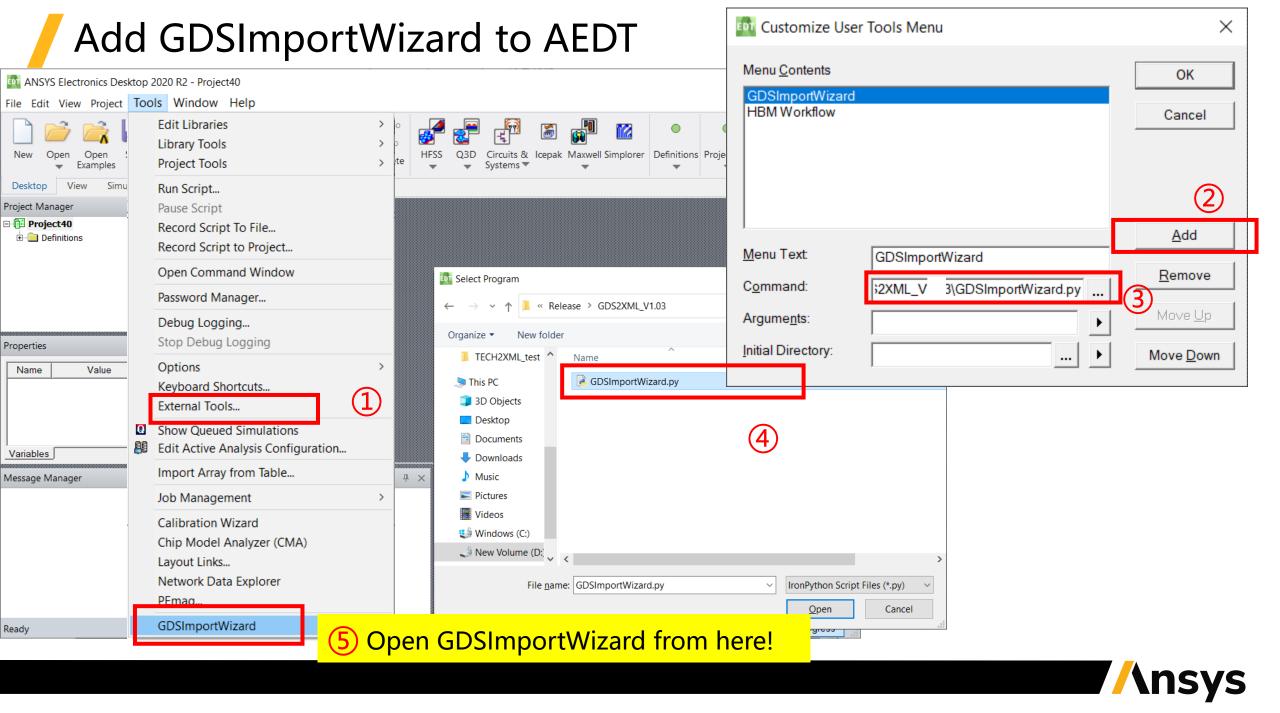


Getting the latest GDSImportWizard Tool

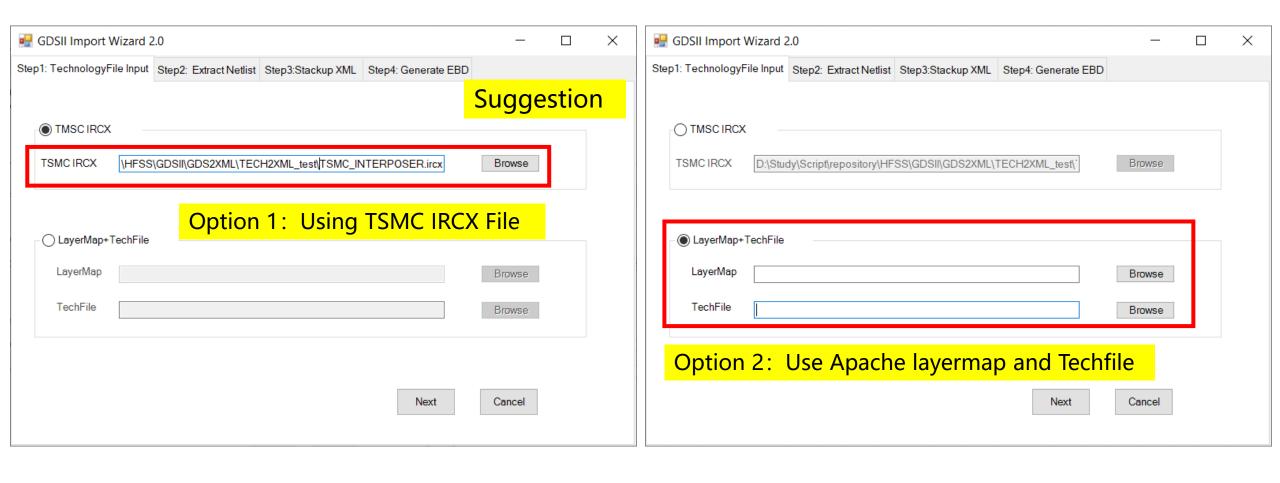
https://github.com/YongshengGuo/GDSImportWizard/releases/latest







Step1: Define Technology File





/ What about IRCX

IRCX is an EDA data format for interconnect modeling with TSMC's 65- and 40-nm process technologies.

Include:

- ✓ Layer Mapping
- ✓ Layer Thickness
- ✓ Layer Material property

Application:

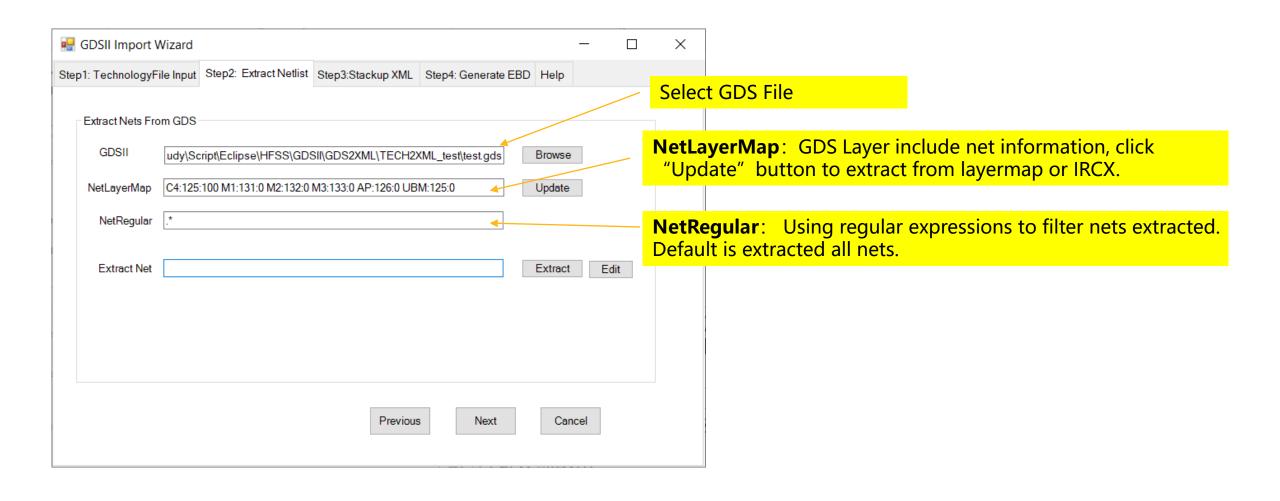
- ✓ RC parasitic extraction,
- ✓ electromigration analysis,
- √ power integrity analysis, and
- ✓ electromagnetic simulation

97	ESS:V)
99 FIELD	ESS:V)
99 FIELD	
101 ubump	
102 UF1 PASS4 107.640000 35.000000 103 PASS4 PASS3b 107.040000 0.600000 104 PASS3b PASS3a 106.640000 0.400000 105 PASS3a PASS2 105.190000 1.450000 106 metal4 PASS2 105.190000 1.450000 107 PASS2 PASS1 104.490000 0.70000 108 PASS1 IMD3c 104.415000 0.075000 109 IMD3c IMD3b 103.690000 0.725000 110 IMD3b IMD3a 103.690000 0.725000 111 metal3 IMD3a 103.640000 0.850000 112 IMD3a IMD2g 103.020000 0.620000 112 IMD3a IMD2g 103.020000 0.620000 113 IMD2g IMD2g 102.970000 0.050000 114 IMD2f IMD2e 102.245000 0.725000 115 IMD2e IMD2d	
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124 IMD1b IMD1a 100.800000 0.725000 125 IMD1a ILD 100.750000 0.050000	
125 IMD1a ILD 100.750000 0.050000	
126 metal1 TLD 100.675000 0.850000	
127 ILD substrate 100.000000 0.750000	
128 substrate PASSB1 0.000000 100.000000	
129 PASSB1 PASSB2b -0.800000 0.800000	
130 mb1 PASSB2b -0.801000 0.001000	
131 PASSB2b PASSB2a -2.800000 2.000000	
132 PASSB2a underFill_C -3.200000 0.400000	
133 underFill_C N/A -3.201000 0.001000	
134 ubmb N/A -3.201000 0.001000	
135	

[LAYER_MAPP]								
#substate is reversed-tone NWELL								
#via4 is (ubump AND metal4)								
#ubump_top_pin is ubump_pin								
#ubmb_top_pin is ubmb_pin								
#RC GDS			-					
ubump	170;0	ubur	np	UBM;	drawing			
metal4	74;	0	metal4		AP;drawing			
DUM4	74;	1	DUM4		AP; dummy			
metal3	33;	40	metal3		M3;drawing			
DUM3	33;	41	DUM3		M3;dummy			
metal2	32;	40	metal2		M2;drawing			
DUM2	32.	41	DITM2		M2;dummy			
metal1	31;	40	metal1 DUM1		M1;drawing			
DUM1	31;	41	DUM1		M1;dummy			
mb1 31;1	100 MB1		M1;BSL					
ubmb	170;100	UBMI	3	UBM;	BSL			
via4	86;0	via	4 CB2;		drawing			
via3 via2	85;0	via:	3		RV;drawing			
via2	52;	40	via2		VIA2;drawing			
via1	51;	40	via1		VIA1;drawing			
tsv 251;	:0 tsv		TSV; draw	ving				
tsv_3t	251;3	tsv	_3t	TSV	dummy1			
pmb 5;10								
					UBM;pin			
metal4_pin								
metal3_pin								
metal2_pin	132	; 0	metal2_p	oin	M2;pin			
metal1_pin	metal1_pin 131;0 mb1_pin 131;100 ubmb_pin 125;100		metal1_pin		M1;pin			
mb1_pin	131	;100	MB1_pin		M1;BSP			
ubmb_pin	125	;100	UBMB_pir	1.	UBM; test0			
ctm 77;	ctm 77;0 ctm cbm 88;0 cbm		CTM; drawing					
ctm_via	51;40	ctm	_via		VIA1;drawing VIA1;drawing			
cbm_v1a	51;40	cbm	_via		VIA1;drawing			

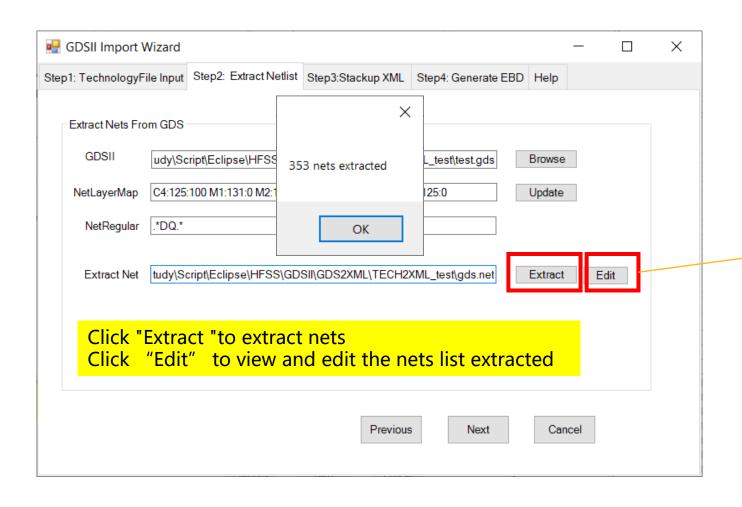


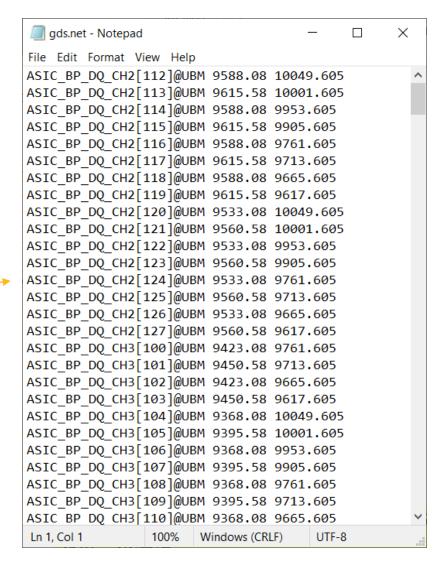
Step2: Extract Nets information from GDSII



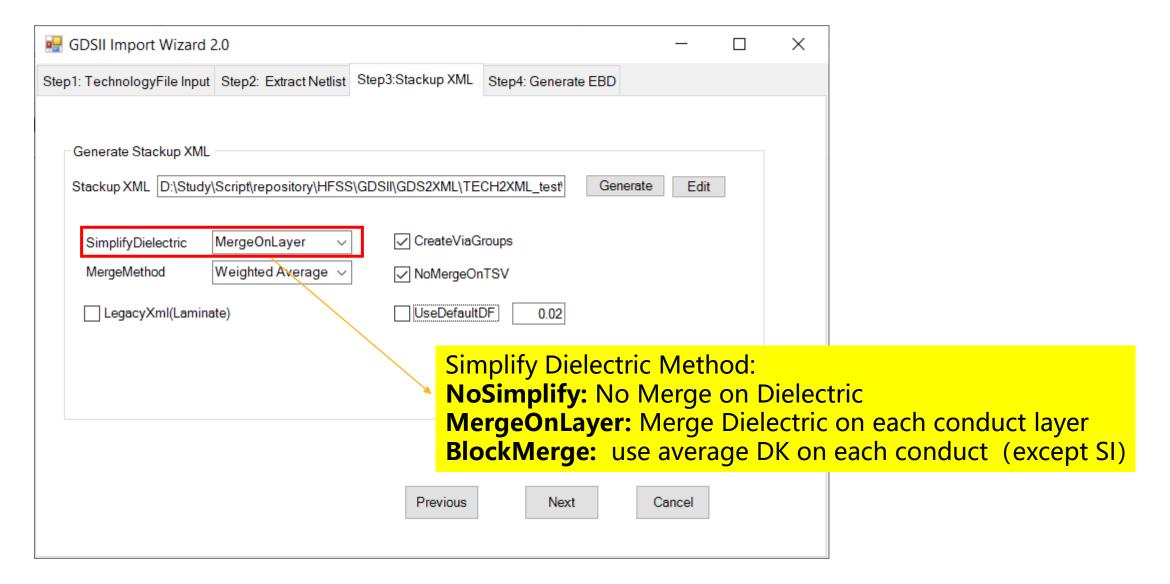


Step2: Extract Nets information from GDSII





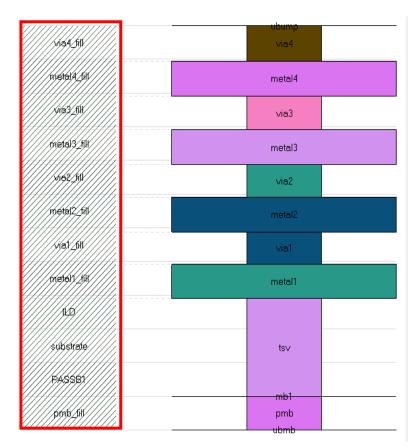


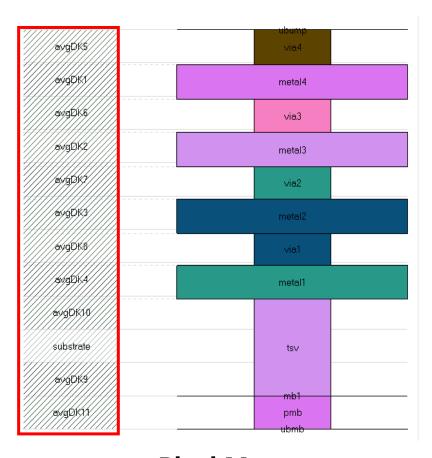




Simplify Dielectric Method compare





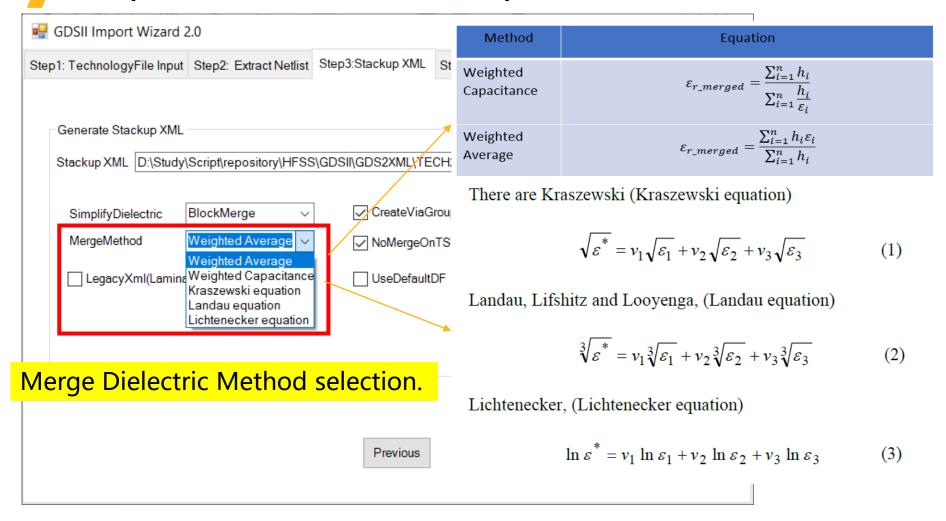


NoSimplify

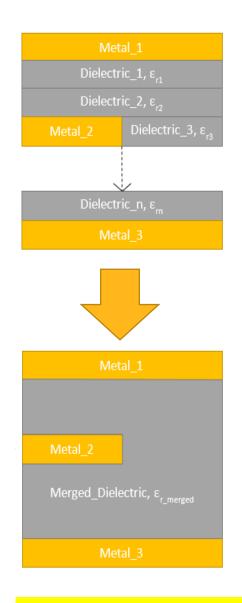
MergeOnLayer

BlockMerge



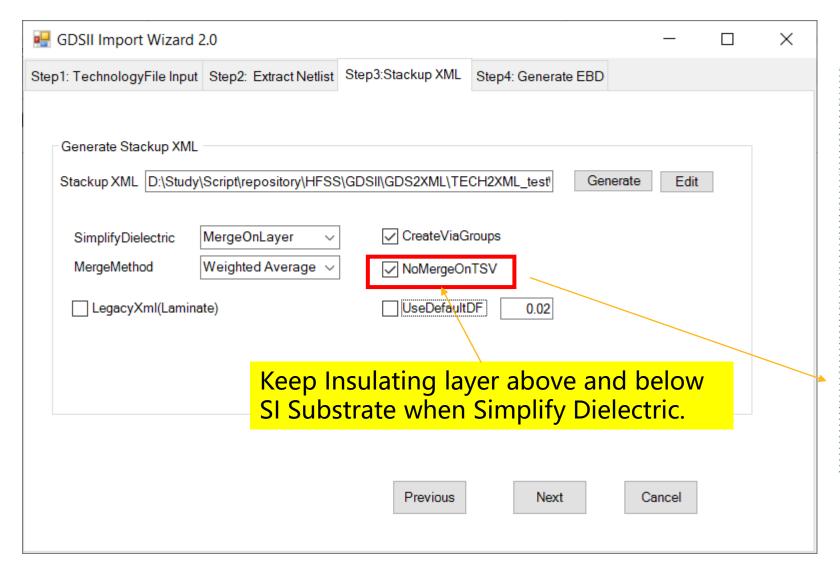


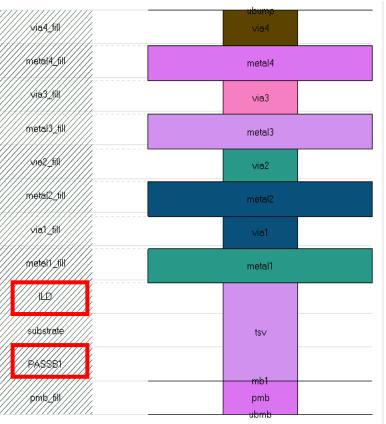
Note: Merge Dielectric also can be done in 3d Layout stackup editor.



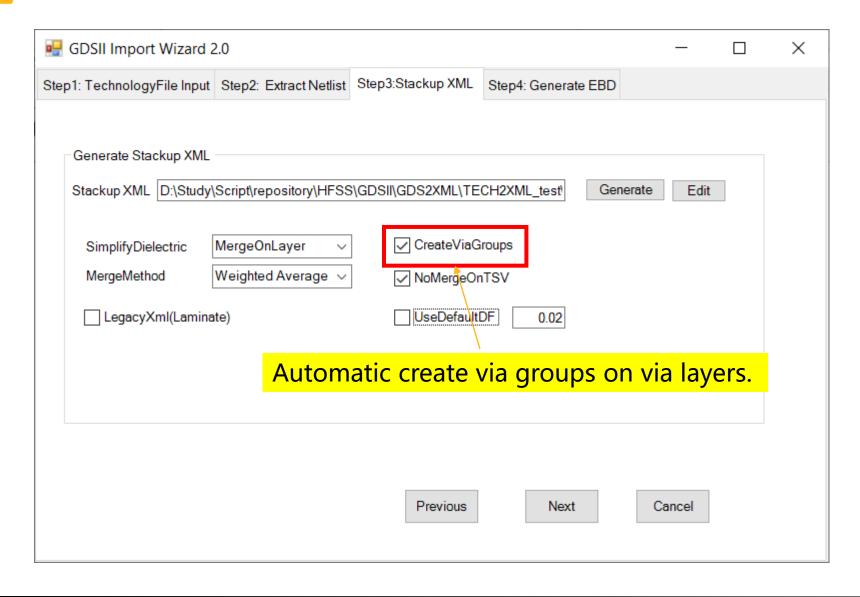
Merge Dielectric

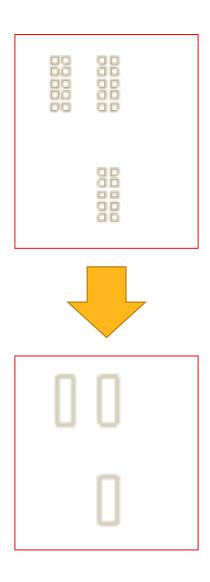




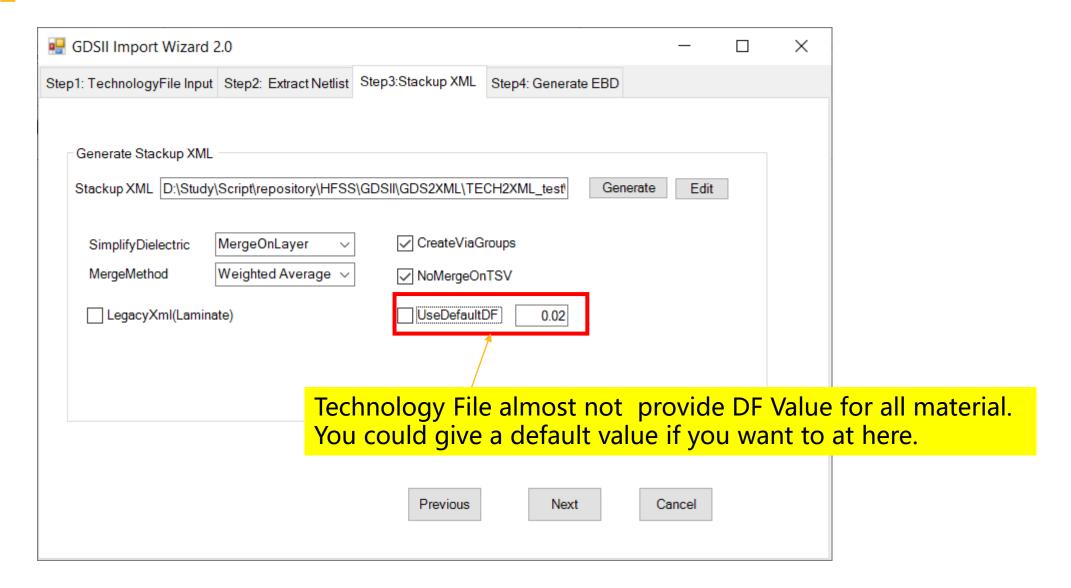




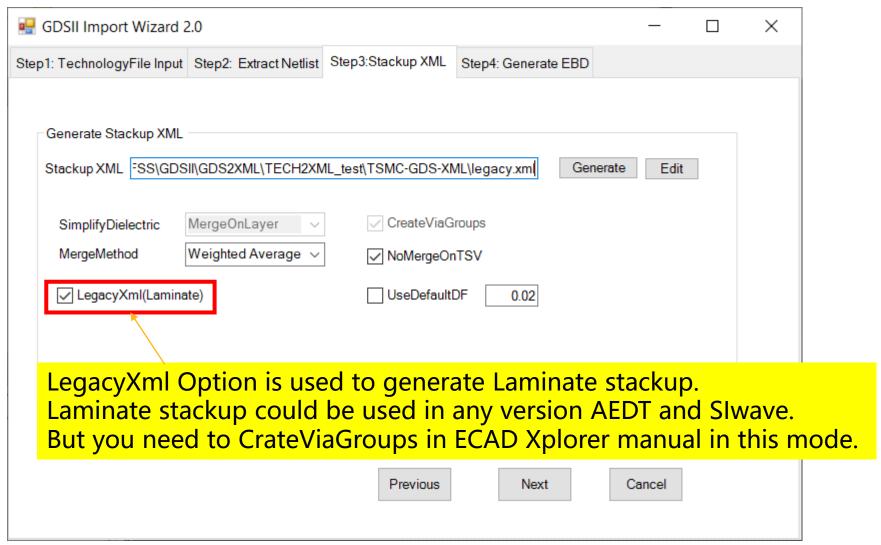




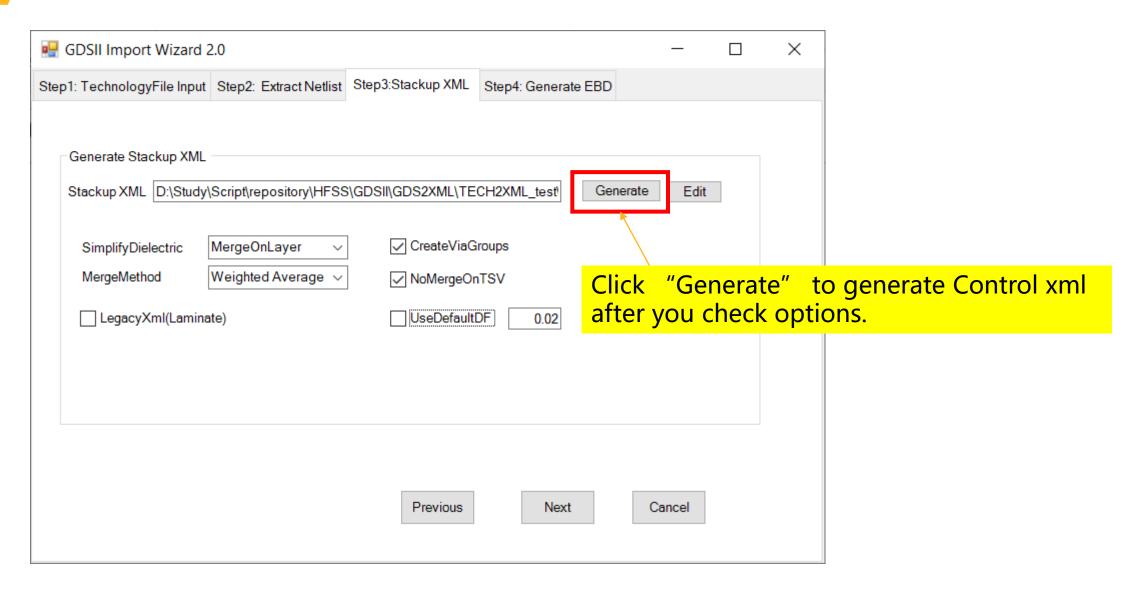






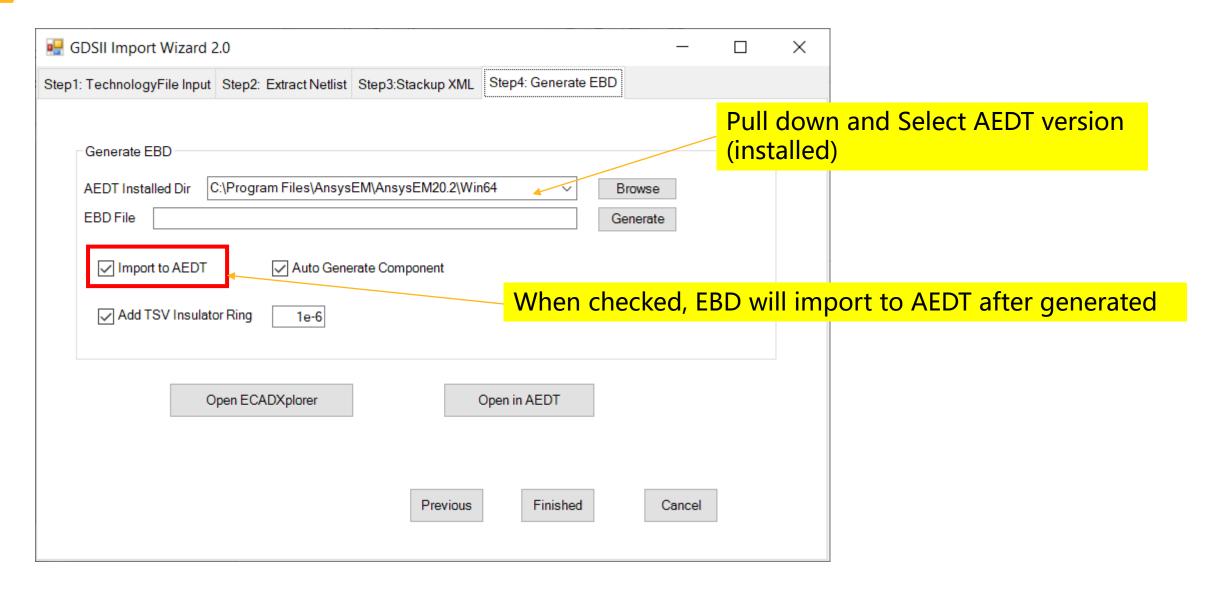


By default, GDSImportWizard generate Overlapping stackup which could create ViaGroups automatically.



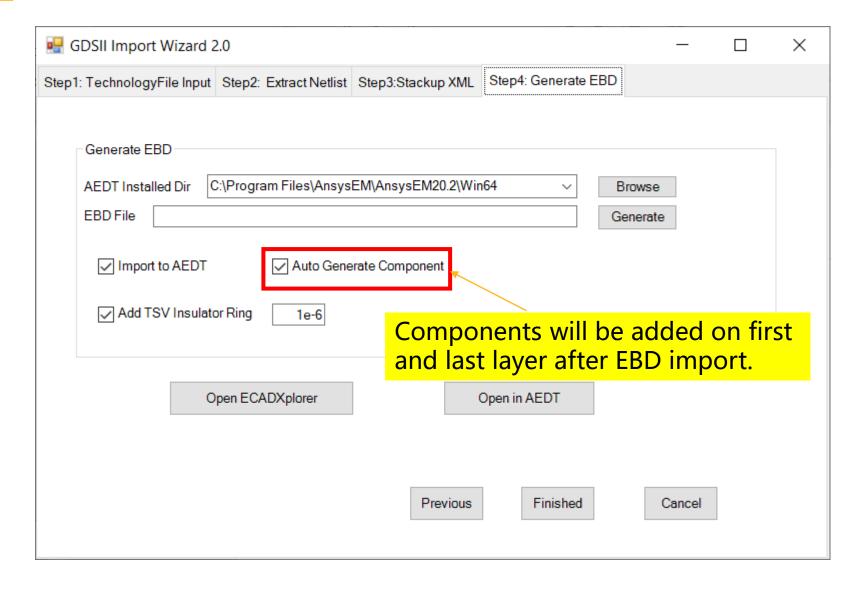


Step4: Generate EBD





Step4: Generate EBD



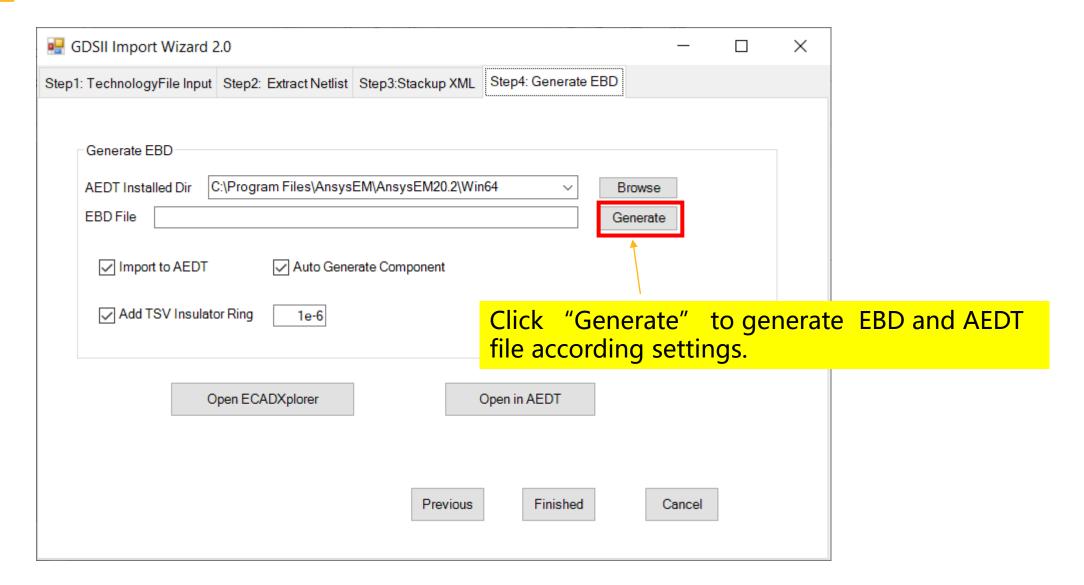
Components	
Regular Expr:	
Resistor Inductor Capacitor IC	
□ ✓ Other □ ✓ ubmb □ ✓ ubmb (84 pins) □ ✓ ubump □ ✓ ubump (270 pins)	



Step4: Generate EBD **µBumps** AI RDL Metal 3 ■ GDSII Import Wizard 2.0 SiO₂ Step4: Generate EBD Step1: TechnologyFile Input | Step2: Extract Netlist | Step3:Stackup XML Metal 2 Generate EBD Metal 1 C:\Program Files\AnsysEM\AnsysEM20.2\Win64 AEDT Installed Dir Browse EBD File **TSV** Generate ✓ Import to AEDT Auto Generate Component Add TSV Insulator Ring 1e-6 TSV Insulator Ring will be added in TSV layer after EBD imported. Ring thickness should be set a purpose value. Previous Finished Cancel

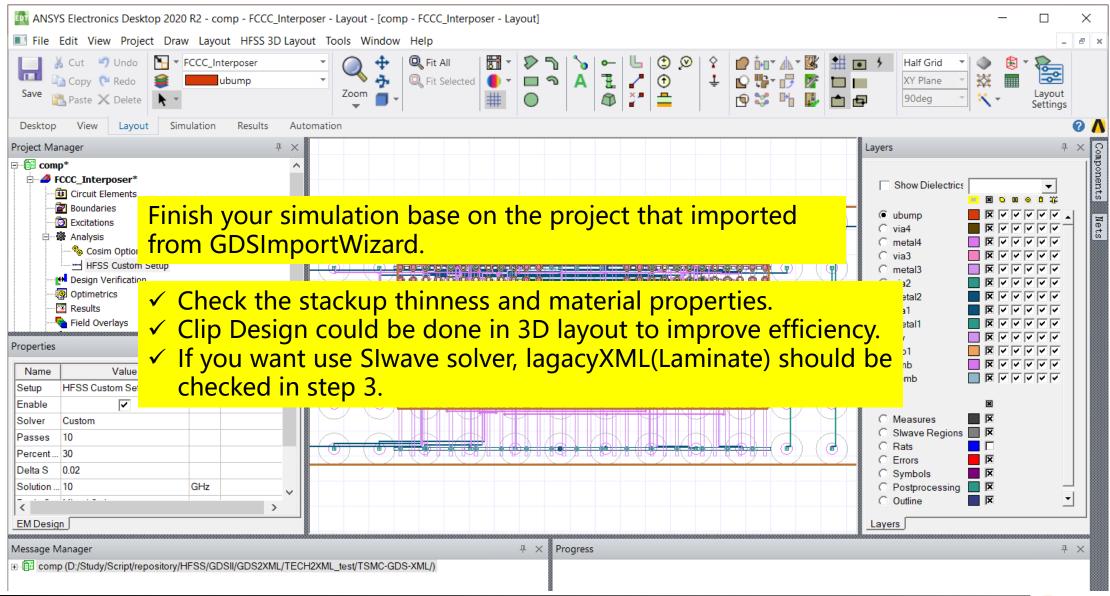


Step4: Generate EBD





Imported Project





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