



GDS Import Wizard V3.1 Manual

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- ANSYS workflow for 2.5D/3D SI Interpower Simulation
- Running in Proficiency Mode
- Running in Wizard Mode
- Running in batch mode - Windows
- Running in batch mode - Linux

About GDS Import Wizard

A smart tool to translate GDSII to 3DLayout EDB quickly:

- Extract nets from GDS and import to EDB
- Extract accurate material property from IRCX
- Extract accurate layer thickness and stack up from IRCX
- Generate control xml for AEDT Import Module
- Support dielectric merge when importing
- Support overlapping and laminated stack up
- Automatic create Via Group and SnapViaGroups
- Generate components on top and bottom layer
- Generate TSV coating and Insulating layer
- Synchronous import to AEDT when EDB prepared

/ ANSYS workflow for 2.5D/3D SI Interpower Simulation

Return

ANSYS AEDT

Option1:

- ✓ TSMC IRCX
- ✓ GDS File

Option2:

- ✓ Tech File
- ✓ Layer Map
- ✓ GDS File

GDSImportWizard

- ✓ Net name extract
- ✓ Stackup
- ✓ Layer thickness
- ✓ Material properties
- ✓ Via Groups
- ✓ Snap Primitives
- ✓ More...

HFSS 3D Layout

- ✓ S-parameter Extraction
- ✓ Crosstalk
- ✓ SSN
- ✓ Eye opening
- ✓ PDN
- ✓ Thermal-EM Co-simulation

Step 1

Step 2

Step 3

Getting the latest GDSImportWizard Tool

Return

<https://github.com/YongshengGuo/GDSImportWizard/releases/latest>

The screenshot shows the GitHub repository page for **YongshengGuo / GDSImportWizard**. The navigation bar includes links for Code, Issues, Pull requests, Actions, Projects, Wiki, Security, Insights, and Settings. The **Releases** tab is selected, and an arrow points to it with the text "Click Releases to download earlier version".

On the left sidebar, there is a "Latest release" badge, a commit hash "55fcee7", a "Verified" badge, and a "Compare" dropdown.

The main content area displays the release title **GDSImportWizard Verxx** and a message from YongshengGuo stating "released this 1 hour ago". Below this, the "Assets" section shows two items:

- Source code (zip)**: This asset is highlighted with a red rectangular box. An arrow points from a yellow box containing the text "Getting From here!" to this asset.
- Source code (tar.gz)**

Add GDS Import Wizard to AEDT

The screenshot illustrates the steps to add the GDS Import Wizard to the AEDT user tools menu:

1. In the **Tools** menu, select **External Tools...**.
2. In the **Customize User Tools Menu** dialog, click the **Add** button.
3. In the **Command** field, enter the path to the GDS Import Wizard script: `\\2XML_V 3\GDSImportWizard.py`.
4. In the **Initial Directory** field, enter the path to the script's directory: `\\2XML_V 3\GDSImportWizard.py`.
5. Open the **GDSImportWizard** from the **Tools** menu.

The **Customize User Tools Menu** dialog also shows the **Menu Contents** list with **GDSImportWizard** and **HBM Workflow** items. The **Menu Text** is **GDSImportWizard**.

The **Select Program** dialog shows the file **GDSImportWizard.py** selected in the **TECH2XML_test** folder.

5 Open GDSImportWizard from here!

New Proficiency Mode modes in V3.0

Switching two modes by click here

GDSII Import Wizard V3.0

GDS Import

☒ TSMC IRCX

Switch to Wizard Mode CheckUpdate

TSMC IRCX Browse

GDSII Browse

SimplifyDielectric MergeOnLayer ☐ CreateViaGroups ☐ LegacyXml(Laminate)

MergeMethod Weighted Average ☐ MergeTSVLayer ☐ UseDefaultDF 0.02

Generate EBD

AEDT Installed Dir C:\Program Files\AnsysEM\AnsysEM20.2\Win64\ Browse

EBD File Browse

☒ Import to AEDT ☒ Auto Generate Component ☒ Add TSV Insulator Ring 1e-6

Generate Close

Mode1: Proficiency Mode

GDSII Import Wizard V3.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

☒ TSMC IRCX

Switch to Proficiency Mode CheckUpdate

TSMC IRCX Browse

☐ LayerMap+Tech

LayerMap Browse

TechFile Browse

Next Cancel

Mode2: Wizard Mode

Running in Proficiency Mode

Proficiency Mode

Switch to wizard mode from here

GDSII Import Wizard V3.1

GDS Import

Switch to Wizard Mode CheckUpdate

☒ TSMC IRCX

TSMC IRCX Browse

GDSII Browse

SimplifyDielectric MergeOnLayer ☒ CreateViaGroups ☐ LegacyXml(Laminate)

MergeMethod Weighted Average ☒ NoMergeTSVLayer ☐ UseDefaultDF 0.02

Generate EBD

AEDT Installed Dir C:\Program Files\AnsysEM\AnsysEM20.2\Win64\ Browse

EBD File Browse

☒ Import to AEDT ☒ Auto Generate Component ☒ Add TSV Insulator Ring 1e-6

Generate Close

Refer to "Wizard Mode" section for the detail comments for Options.

Finished whole import flow once

Note: Proficiency mode has the same options as Wizard mode. Proficiency mode provides quick import way for users who are familiar with the workflow. Please refer to "Wizard Mode "document for the detail comments for all Options input.

Running in Wizard Mode

Step1: Define Technology File

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

☒ TSMC IRCX

TSMC IRCX Browse

☐ LayerMap+TechFile

LayerMap Browse

TechFile Browse

Next Cancel

Option 1: Using TSMC IRCX File

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

☐ TSMC IRCX

TSMC IRCX Browse

☒ LayerMap+TechFile

LayerMap Browse

TechFile Browse

Next Cancel

Option 2: Use Apache layermap and Techfile

Option 1: Using TSMC IRCX File is suggested workflow.

What about IRCX

IRCX is an EDA data format for interconnect modeling with TSMC's 65- and 40-nm process technologies.

Include:

- ✓ Layer Mapping
- ✓ Layer Thickness
- ✓ Layer Material property

Application:

- ✓ RC parasitic extraction,
- ✓ electromigration analysis,
- ✓ power integrity analysis, and
- ✓ electromagnetic simulation

```
96 [RC SPICE INFORMATION]
97 LAYER {
98 * STACK 34 4 (NAME:V, MEASURED_FROM:V, HEIGHT:V, THICKNESS:V)
99 FIELD      MEASURED_FROM  HEIGHT  THICKNESS
100 NAME
101 ubump      UF1           142.639000  0.001000
102 UF1        PASS4         107.640000  35.000000
103 PASS4      PASS3b        107.040000  0.600000
104 PASS3b     PASS3a        106.640000  0.400000
105 PASS3a     PASS2         105.190000  1.450000
106 metal4     PASS2         105.190000  1.450000
107 PASS2      PASS1         104.490000  0.700000
108 PASS1      IMD3c         104.415000  0.075000
109 IMD3c      IMD3b         103.690000  0.725000
110 IMD3b      IMD3a         103.640000  0.050000
111 metal3     IMD3a         103.565000  0.850000
112 IMD3a      IMD2g         103.020000  0.620000
113 IMD2g      IMD2f         102.970000  0.050000
114 IMD2f      IMD2e         102.245000  0.725000
115 IMD2e      IMD2d         102.195000  0.050000
116 metal2     IMD2d         102.120000  0.850000
117 IMD2d      IMD2c         101.873000  0.322000
118 IMD2c      IMD2b         101.793000  0.080000
119 ctm         IMD2b         101.793000  0.080000
120 IMD2b      IMD2a         101.775000  0.018000
121 IMD2a      IMD1c         101.575000  0.200000
122 cbm         IMD1c         101.575000  0.200000
123 IMD1c      IMD1b         101.525000  0.050000
124 IMD1b      IMD1a         100.800000  0.725000
125 IMD1a      ILD           100.750000  0.050000
126 metal1     ILD           100.675000  0.850000
127 ILD        substrate     100.000000  0.750000
128 substrate  PASSB1         0.000000  100.000000
129 PASSB1     PASSB2b        -0.800000  0.800000
130 mb1        PASSB2b        -0.801000  0.001000
131 PASSB2b    PASSB2a        -2.800000  2.000000
132 PASSB2a    underFill_C    -3.200000  0.400000
133 underFill_C N/A           -3.201000  0.001000
134 ubmb       N/A           -3.201000  0.001000
135
```

```
[LAYER_MAPPING]
#substate is reversed-tone NWELL
#via4 is (ubump AND metal4)
#ubump_top_pin is ubump_pin
#ubmb_top_pin is ubmb_pin
#RC      GDS  LVS      DFII
ubump      170;0      ubump      UBM;drawing
metal4      74;0      metal4      AP;drawing
DUM4        74;1      DUM4        AP;dummy
metal3      33;40     metal3      M3;drawing
DUM3        33;41     DUM3        M3;dummy
metal2      32;40     metal2      M2;drawing
DUM2        32;41     DUM2        M2;dummy
metal1      31;40     metal1      M1;drawing
DUM1        31;41     DUM1        M1;dummy
mb1         31;100    MB1         M1;BSL
ubmb        170;100   UBMB        UBM;BSL
via4         86;0     via4         CB2;drawing
via3         85;0     via3         RV;drawing
via2         52;40     via2         VIA2;drawing
vial         51;40     vial         VIA1;drawing
tsv          251;0     tsv          TSV;drawing
tsv_3t       251;3     tsv_3t       TSV;dummy1
pmb          5;100    PMB          PM;dummy
ubump_pin    125;0     ubm_top_pin   UBM;pin
metal4_pin   126;0     metal4_pin    AP;pin
metal3_pin   133;0     metal3_pin    M3;pin
metal2_pin   132;0     metal2_pin    M2;pin
metal1_pin   131;0     metal1_pin    M1;pin
mb1_pin      131;100   MB1_pin       M1;BSP
ubmb_pin     125;100   UBMB_pin      UBM;test0
ctm          77;0     ctm          CTM;drawing
cbm          88;0     cbm          CBM;drawing
ctm_via      51;40     ctm_via       VIA1;drawing
cbm_via      51;40     cbm_via       VIA1;drawing
```

Step2: Extract Nets information from GDSII

GDSII Import Wizard

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD Help

Extract Nets From GDS

GDSII Browse

NetLayerMap Update

NetRegular

Extract Net

Extract Edit

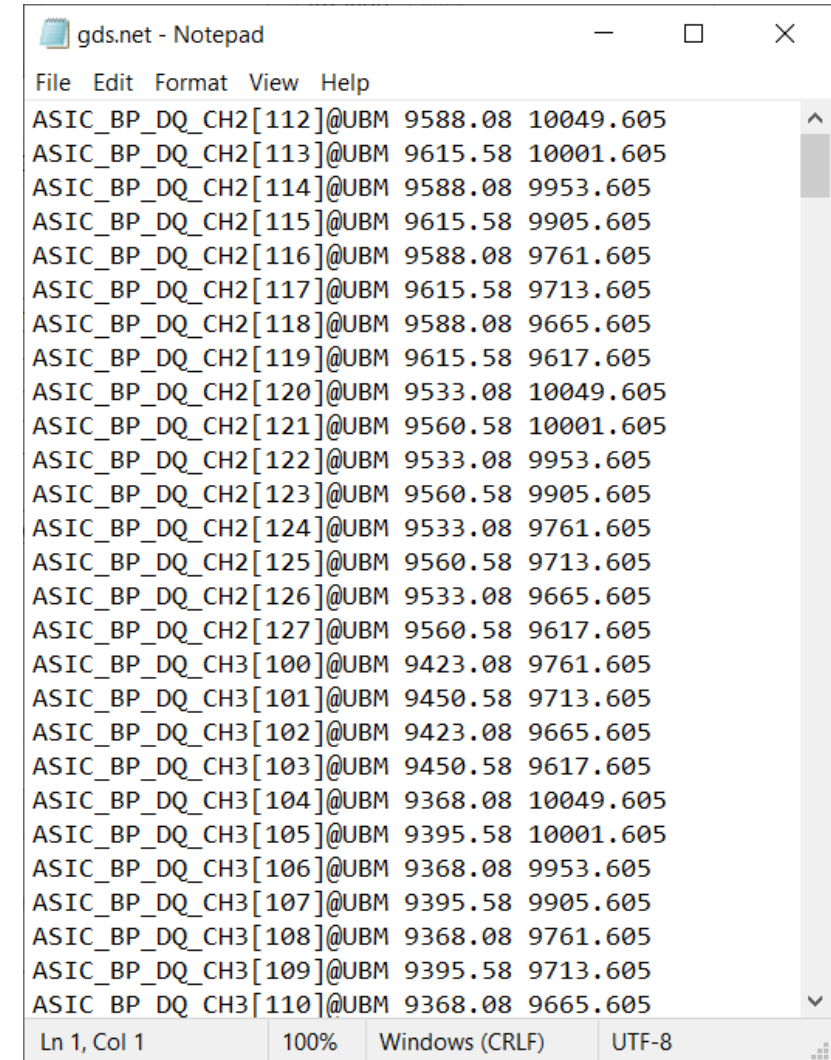
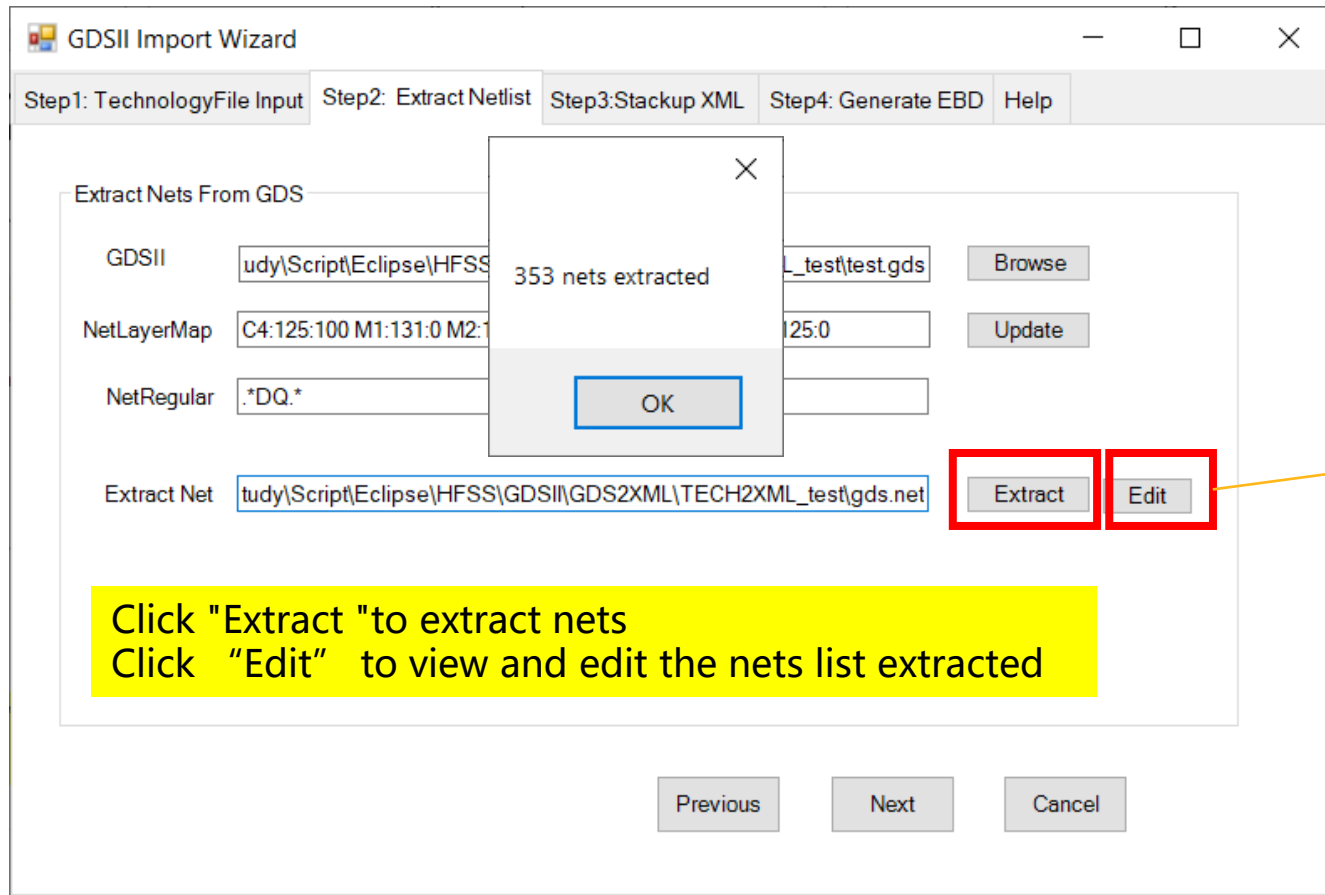
Previous Next Cancel

GDSII: set GDS File

NetLayerMap: GDS Layer include net information, click "Update" button to extract from layermap or IRCX.

NetRegular: Using regular expressions to filter nets extracted. Default is extracted all nets.

Step2: Extract Nets information from GDSII



Step3: Generate Stackup XML (Control file)

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML

☒ CreateViaGroups

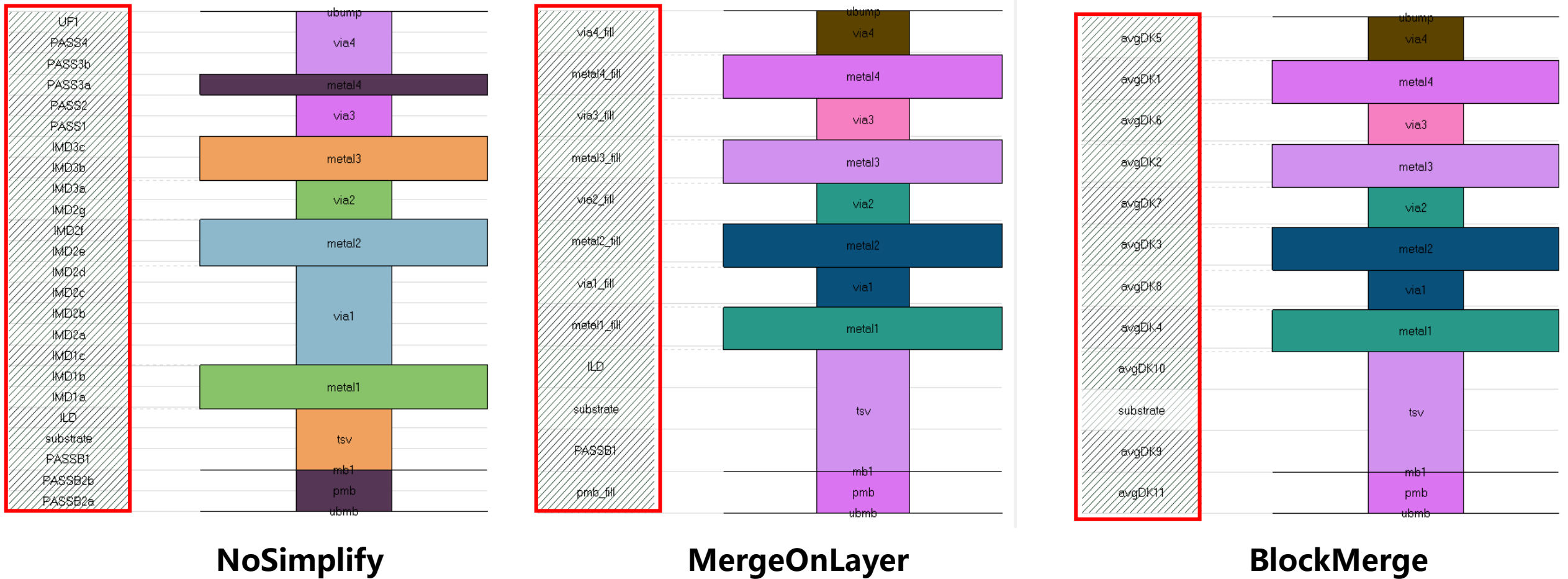
MergeMethod ☒ NoMergeTSVLayer

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Simplify Dielectric Method:
NoSimplify: No Merge on Dielectric
MergeOnLayer: Merge Dielectric on each conduct layer
BlockMerge: use average DK on each conduct (except SI material)

Step3: Generate Stackup XML (Control file)

- Simplify Dielectric Method compare



Step3: Generate Stackup XML (Control file)

GDSII Import Wizard 2.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML

Generate Stackup XML

Stackup XML D:\Study\Script\repository\HFSS\GDSII\GDS2XML\TECH

SimplifyDielectric BlockMerge ☒ CreateViaGroup

MergeMethod **Weighted Average** ☒ NoMergeOnTS

☐ LegacyXml(Laminates) ☐ UseDefaultDF

Weighted Capacitance

Weighted Average

Previous

Method	Equation
Weighted Capacitance	$\epsilon_{r_merged} = \frac{\sum_{i=1}^n h_i}{\sum_{i=1}^n \frac{h_i}{\epsilon_i}}$
Weighted Average	$\epsilon_{r_merged} = \frac{\sum_{i=1}^n h_i \epsilon_i}{\sum_{i=1}^n h_i}$

There are Kraszewski (Kraszewski equation)

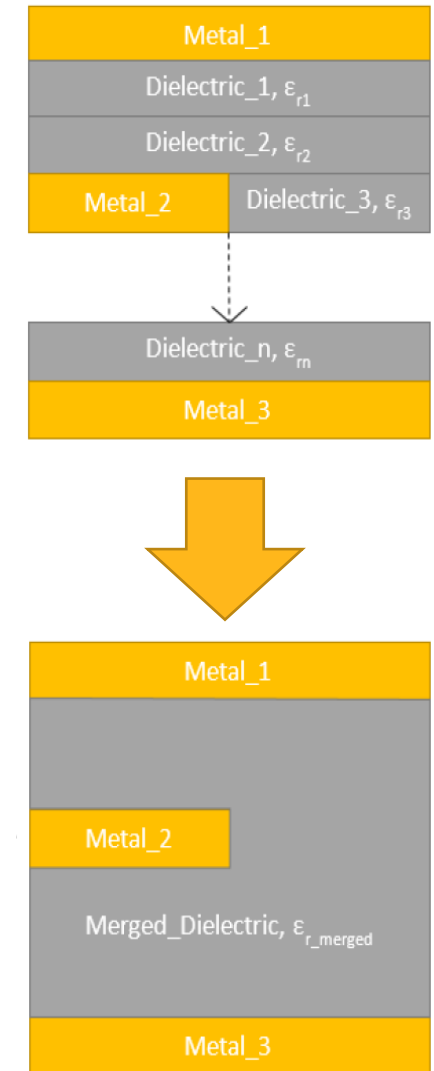
$$\sqrt{\epsilon^*} = v_1 \sqrt{\epsilon_1} + v_2 \sqrt{\epsilon_2} + v_3 \sqrt{\epsilon_3} \quad (1)$$

Landau, Lifshitz and Looyenga, (Landau equation)

$$\sqrt[3]{\epsilon^*} = v_1 \sqrt[3]{\epsilon_1} + v_2 \sqrt[3]{\epsilon_2} + v_3 \sqrt[3]{\epsilon_3} \quad (2)$$

Lichtenecker, (Lichtenecker equation)

$$\ln \epsilon^* = v_1 \ln \epsilon_1 + v_2 \ln \epsilon_2 + v_3 \ln \epsilon_3 \quad (3)$$



Merge Dielectric Method selection.

Merge Dielectric

Note: Merge Dielectric also can be done in 3d Layout stackup editor.

Step3: Generate Stackup XML (Control file)

GDSII Import Wizard V3.0

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

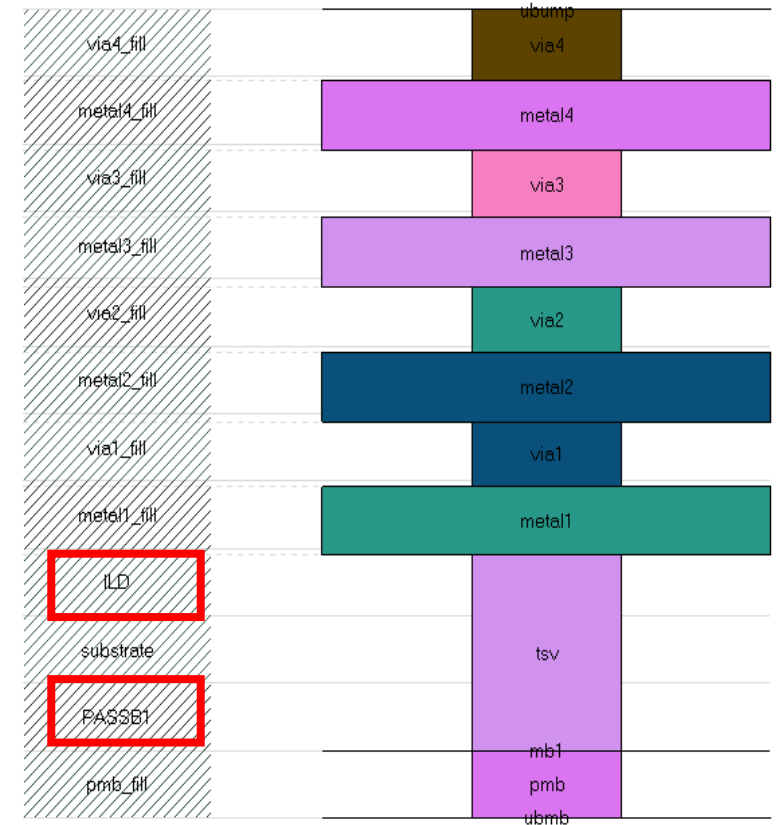
Stackup XML

SimplifyDielectric ☒ CreateViaGroups

MergeMethod ☐ MergeTSVLayer

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Keep Insulating layer above and below SI Substrate when Simplify Dielectric.



Step3: Generate Stackup XML (Control file)

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

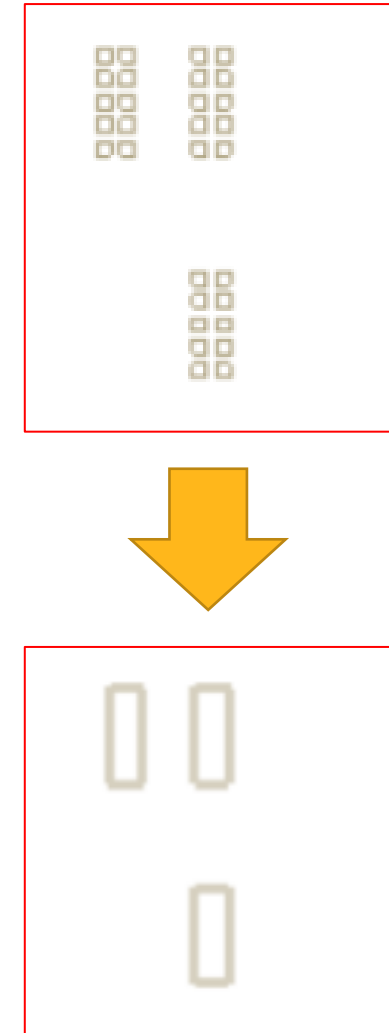
Stackup XML

SimplifyDielectric ☒ CreateViaGroups

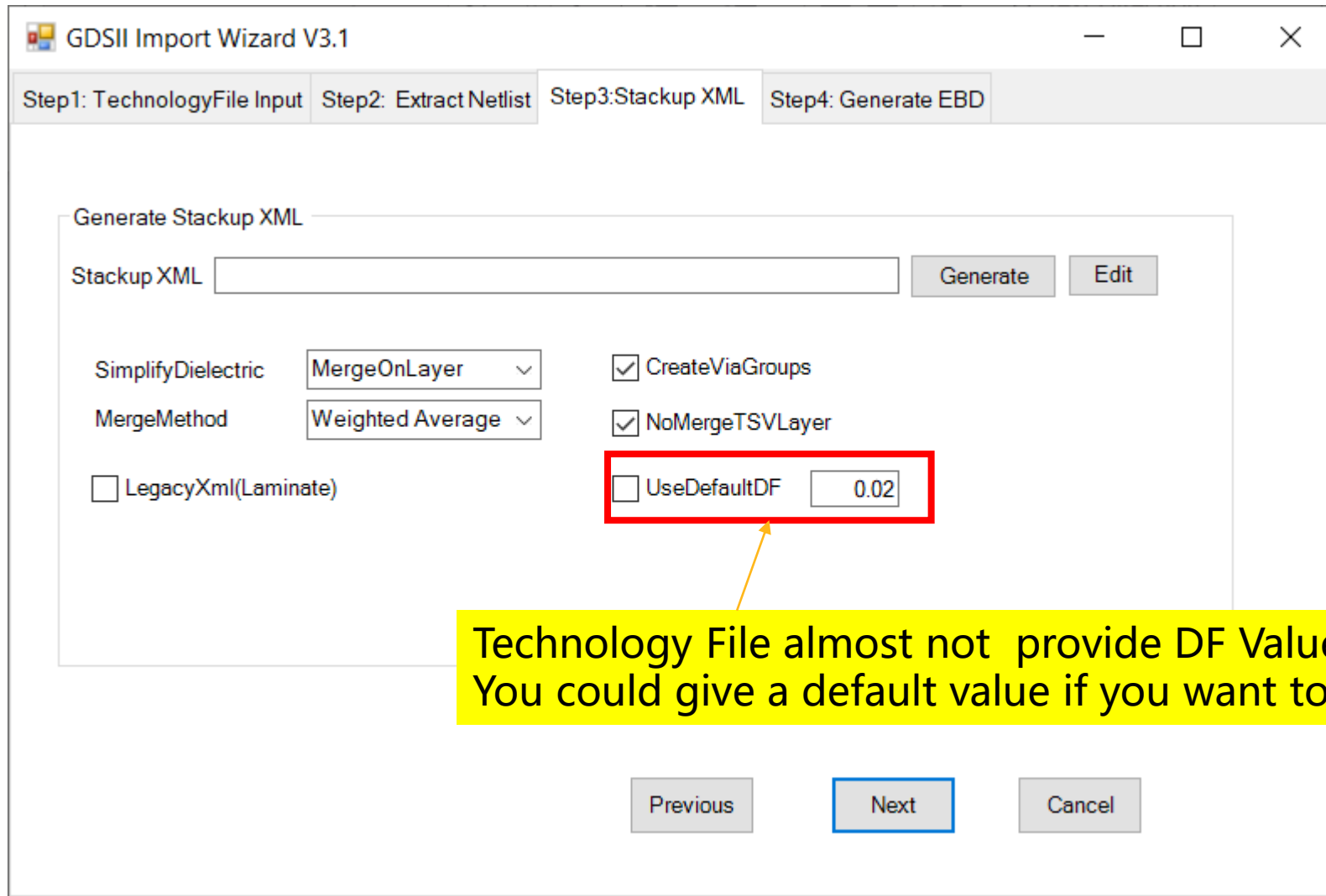
MergeMethod ☒ NoMergeTSVLayer

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Automatic create via groups on via layers.



Step3: Generate Stackup XML (Control file)



GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML Generate Edit

SimplifyDielectric MergeOnLayer ☐ CreateViaGroups

MergeMethod Weighted Average ☒ NoMergeTSVLayer

☐ LegacyXml(Laminate) ☐ UseDefaultDF 0.02

Previous Next Cancel

Technology File almost not provide DF Value for all material. You could give a default value if you want to at here.

Step3: Generate Stackup XML (Control file)

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML

SimplifyDielectric ☒ CreateViaGroups

MergeMethod ☒ NoMergeTSVLayer

☐ LegacyXml(Laminate) ☐ UseDefaultDF

LegacyXml Option is used to generate Laminate stackup. Laminate stackup could be used in any version AEDT and SIwave. But you need to CreateViaGroups in ECAD Xplorer manual in this mode.



By default, GDSImportWizard generate Overlapping stackup which could create ViaGroups automatically.

Step3: Generate Stackup XML (Control file)

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate Stackup XML

Stackup XML

SimplifyDielectric ☒ CreateViaGroups

MergeMethod ☒ NoMergeTSVLayer

☐ LegacyXml(Laminate) ☐ UseDefaultDF

Click "Generate" to generate Control xml after you check options.

Step4: Generate EBD

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

AEDT Installed Dir C:\Program Files\AnsysEM\AnsysEM20.2\Win64\ Browse

EBD File Generate EBD

☒ Import to AEDT ☒ Auto Generate Component

☒ Add TSV Insulator Ring 1e-6

Open ECADExplorer Open in AEDT

Previous Finished Cancel

Pull down and Select AEDT version (installed)

When checked, EBD will import to AEDT after generated

Step4: Generate EBD

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

AEDT Installed Dir: C:\Program Files\AnsysEM\AnsysEM20.2\Win64\ Browse

EBD File: Generate EBD

☒ Import to AEDT ☒ Auto Generate Component

☒ Add TSV Insulator Ring 1e-6

Open ECADExplorer Open in AEDT

Previous Finished Cancel

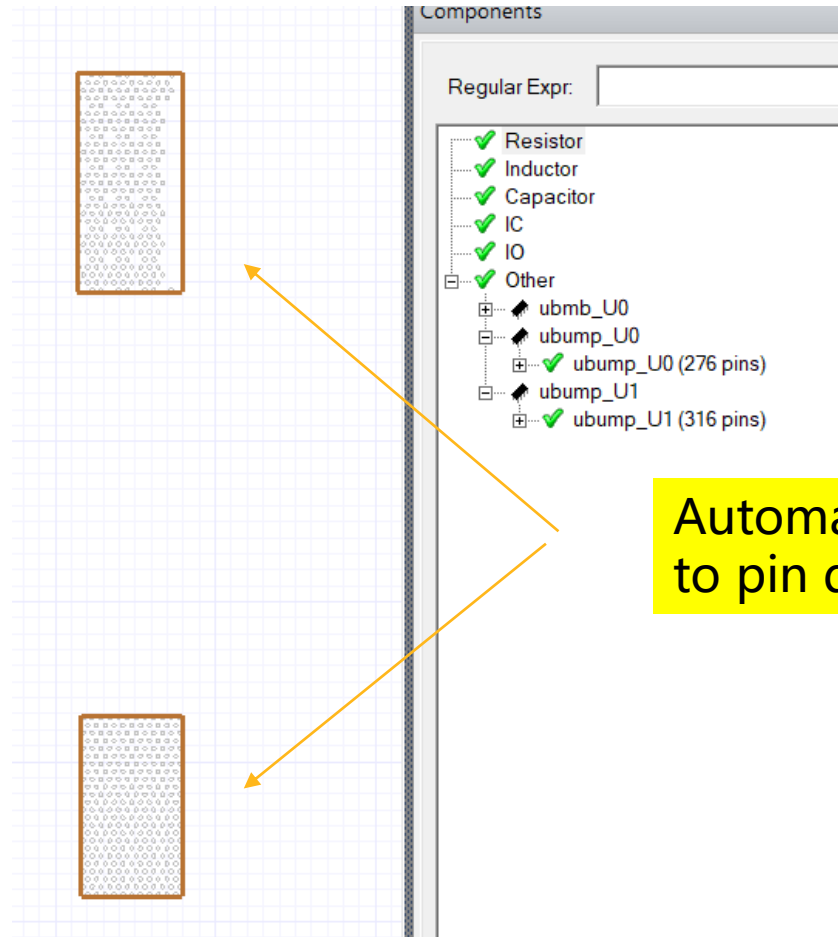
Components will be added on first and last layer after EBD import.

Components

Regular Expr:

- ☒ Resistor
- ☒ Inductor
- ☒ Capacitor
- ☒ IC
- ☒ IO
- ☒ Other
 - ☒ ubmb
 - ☒ ubmb (84 pins)
 - ☒ ubump
 - ☒ ubump (270 pins)

Step4: Generate EBD



Automatically generate individual components according to pin distribution and spacing. (New in V3.x)

Step4: Generate EBD

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

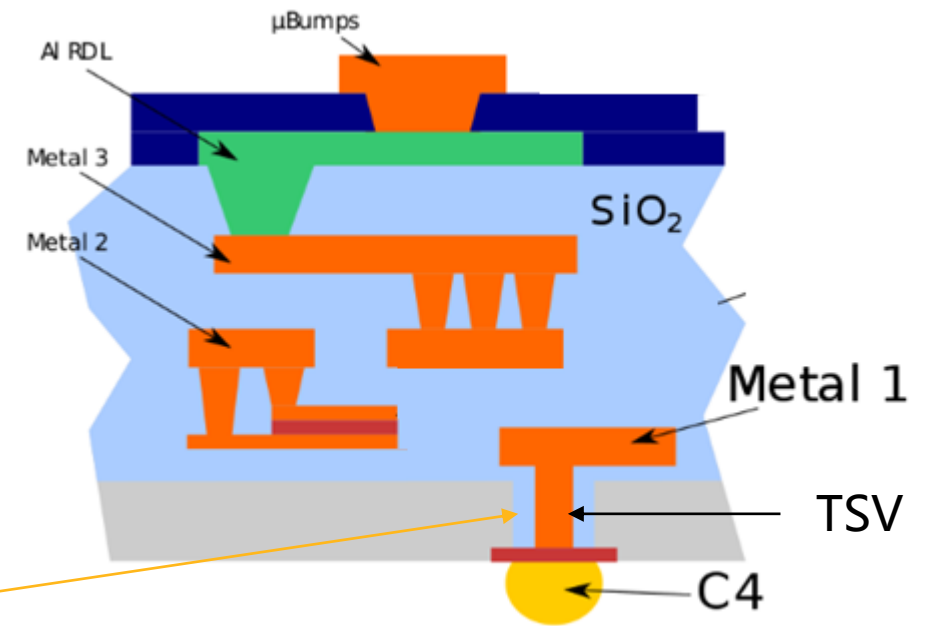
AEDT Installed Dir: C:\Program Files\AnsysEM\AnsysEM20.2\Win64\ Browse

EBD File: Generate EBD

☒ Import to AEDT ☒ Auto Generate Component

☒ Add TSV Insulator Ring 1e-6

Previous Finished Cancel



TSV Insulator Ring will be added in TSV layer after EBD imported. Ring thickness should be set a purpose value.

Step4: Generate EBD

GDSII Import Wizard V3.1

Step1: TechnologyFile Input Step2: Extract Netlist Step3: Stackup XML Step4: Generate EBD

Generate EBD

AEDT Installed Dir C:\Program Files\AnsysEM\AnsysEM20.2\Win64\ Browse

EBD File

☒ Import to AEDT ☒ Auto Generate Component

☒ Add TSV Insulator Ring 1e-6

Generate EBD

Open ECADExplorer Open in AEDT

Previous Finished Cancel

Click "Generate" to generate EBD and AEDT file according settings.

Imported Project

The screenshot displays the ANSYS Electronics Desktop 2020 R2 interface. The main window shows a layout of a circuit board with various components and traces. The Project Manager on the left lists the project structure, including 'comp*', 'FCCC_Interposer*', and 'Circuit Elements'. The Properties panel on the bottom left shows the 'EM Design' tab with settings for 'Setup', 'Solver', 'Passes', 'Percent...', 'Delta S', and 'Solution...'. The Layers panel on the right shows a list of layers with checkboxes for 'Show Dielectrics', 'Measures', 'Slwave Regions', 'Rats', 'Errors', 'Symbols', 'Postprocessing', and 'Outline'. A blue text box is overlaid on the center of the image, containing instructions and a checklist.

Finish your simulation base on the project that imported from GDSImportWizard.

- ✓ Check the stackup thickness and material properties.
- ✓ Clip Design could be done in 3D layout to improve efficiency.
- ✓ If you want use Slwave solver, lagacyXML(Laminate) should be checked in step 3.

Stackup and Material

Edit Layers - interposer

Stackup Layer Zone

Primary

- Display
- ☒ Stackup layers
 - ☐ Non-stackup layers
 - ☐ All layers

Stackup

Type:

Units:

							Name	Type	Material	Thickness	Etch	Rough	Solver
	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	metal1	signal	metal1_cond	0.85um	<input type="checkbox"/>	<input type="checkbox"/>	0.
	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	ILD	dielectric	ILD	0.75um	<input type="checkbox"/>	<input type="checkbox"/>	0.
	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	substrate	dielectric	substrate	100um	<input type="checkbox"/>	<input type="checkbox"/>	0.
	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	tsv	via	tsv_cond	101.476um	<input type="checkbox"/>	<input type="checkbox"/>	m
	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	mb1	signal	mb1_cond	0um	<input type="checkbox"/>	<input type="checkbox"/>	0.
	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	PASSB1	dielectric	PASSB1	0.8um	<input type="checkbox"/>	<input type="checkbox"/>	0.
	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	pmb	via	pmb_cond	2.4um	<input type="checkbox"/>	<input type="checkbox"/>	ut
	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	pmb_fill	dielectric	pmb_fill	2.399um	<input type="checkbox"/>	<input type="checkbox"/>	0r
	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	ubmb	signal	ubmb_cond	0um	<input type="checkbox"/>	<input type="checkbox"/>	0r

Layer

Insert above...

Insert below...

Remove

Select all

Edit selected

Name:

Type:

Material:

Thickness:

Top bottom:

Visibility

- ☒
- ☒
- ☒
- ☒
- ☒

Attributes

- ☐ Negative
 - ☒
 - ☐
- 10%

Analysis

- ☐ Etch
 - ☐ Rough
 - ☐ Solver
- Roughness...
- Solver...

View / Edit Material

Material Name:

Properties of the Material

Name	Type	Value	Units
Relative Permittivity	Simple	11.9	
Relative Permeability	Simple	1	
Bulk Conductivity	Simple	10	siemens/m
Dielectric Loss Tangent	Simple	0	
Magnetic Loss Tangent	Simple	0	

View/Edit Material for

- ☒ Active Design
- ☐ Active Project
- ☐ All Properties

Physics:

- ☒ Electromagnetic
- ☐ Thermal
- ☐ Structural

Material Appearance

- ☐ Use Material Appearance

Color:

Transparency:

Notes:

Set Frequency Dependency... Calculate Properties for:

Reset OK Cancel

Validate Material

Relative Permeability: 1

PASSB1

pmb_fill

mb1

pmb

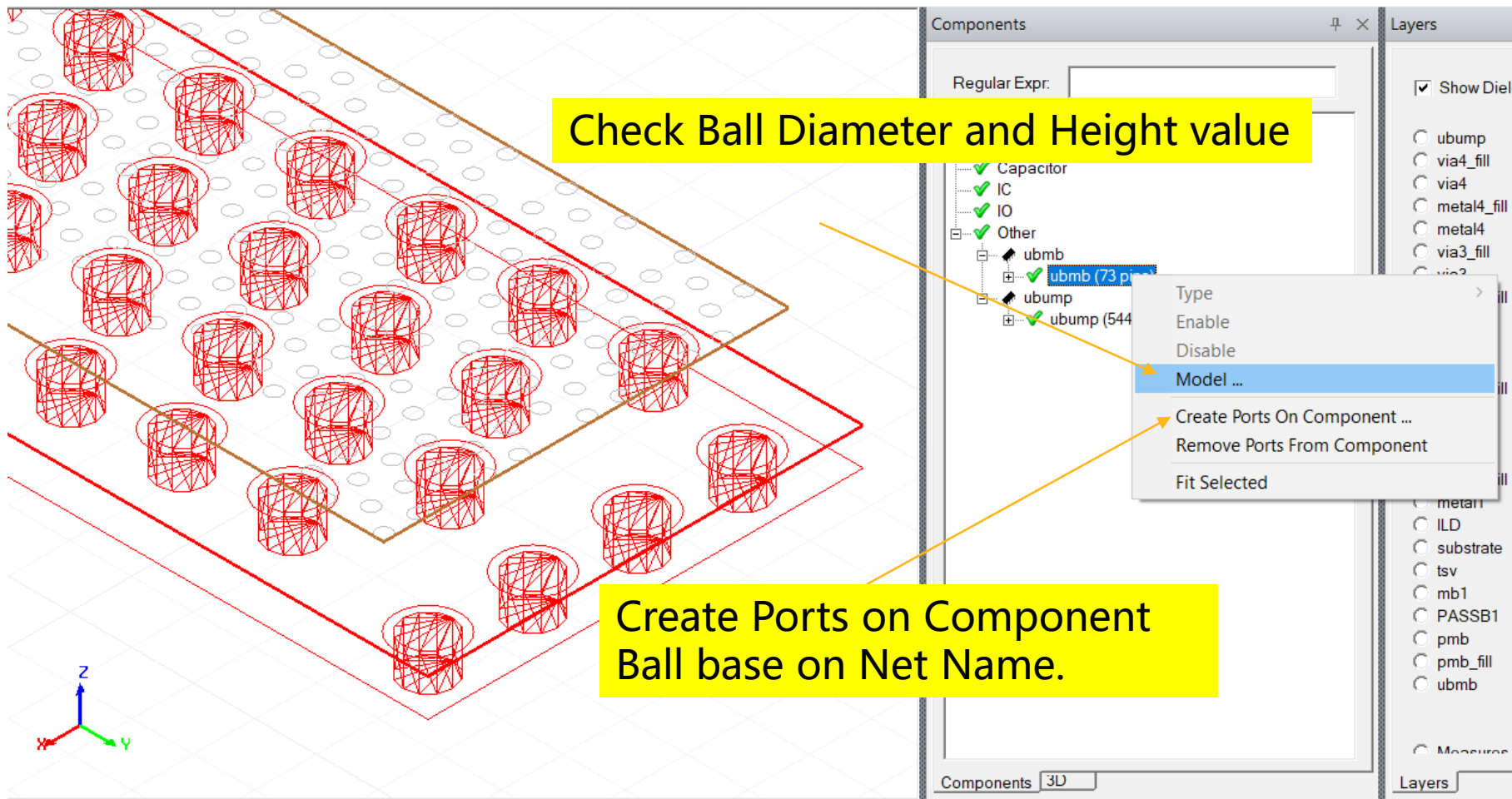
ubmb

Total height 0.145913mm

Apply and Close Apply Close

Check Bulk Conductivity for Substrate Material

Component solder ball and port



Component Model

Component Info

Part Name: ubmb

Part Type: Other

Ref Des: ubmb

No. Pins: 73

Model Interface

Interface: Manual

Solder Ball Properties

Shape: Cylinder

Diameter: 80um

Mid Diameter: 0mm

Height: 60um

Material: solder

Port Properties

Reference Offset: 0

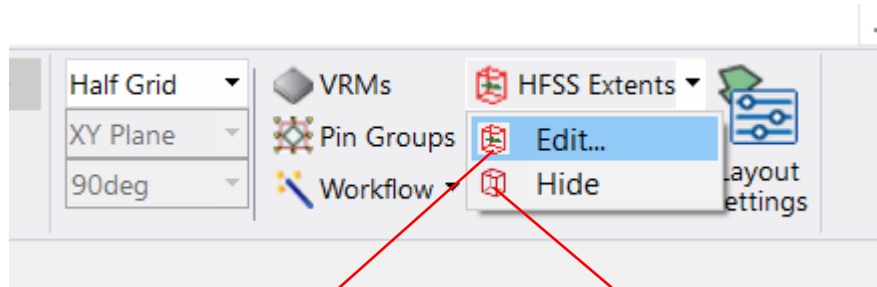
Reference Size: ☒ Auto

X: 0

Y: 0

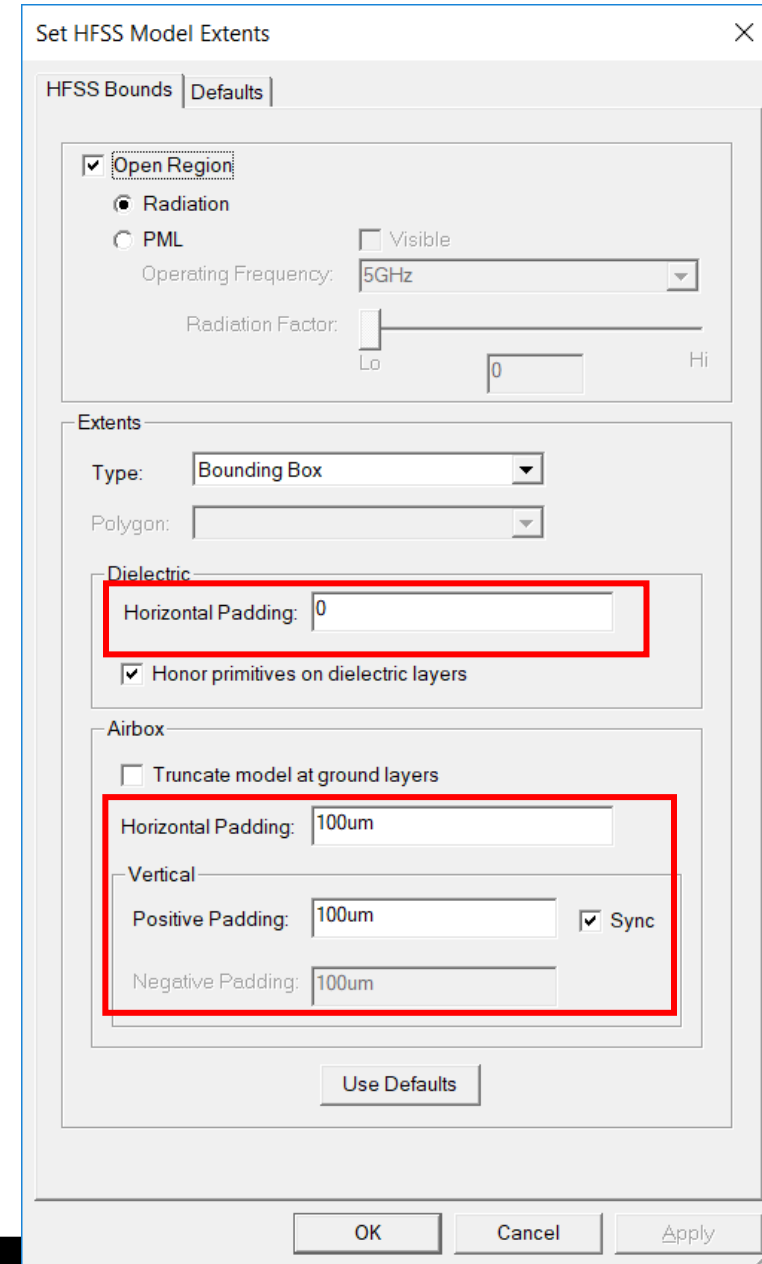
OK Cancel

/ Set HFSS Model Extents(Airbox)

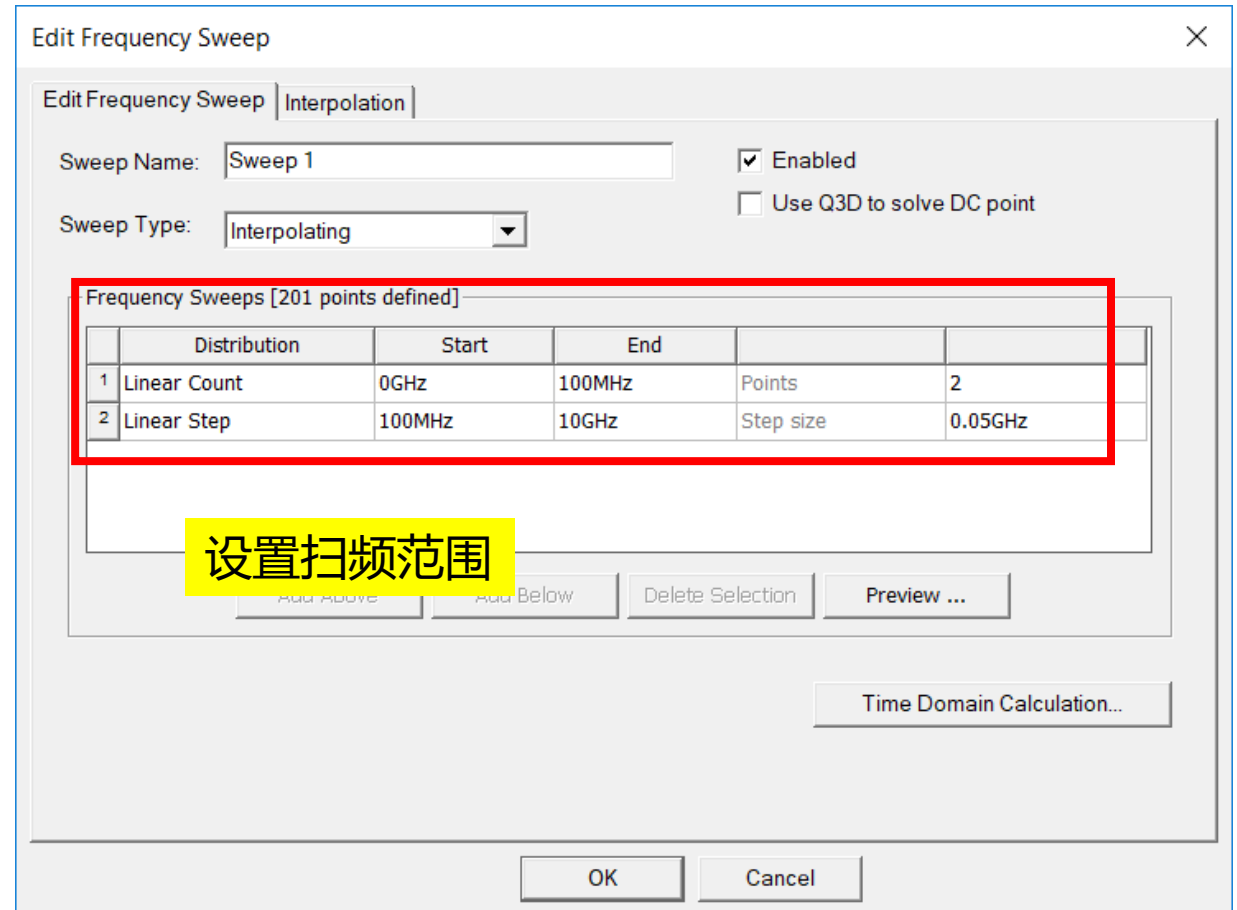
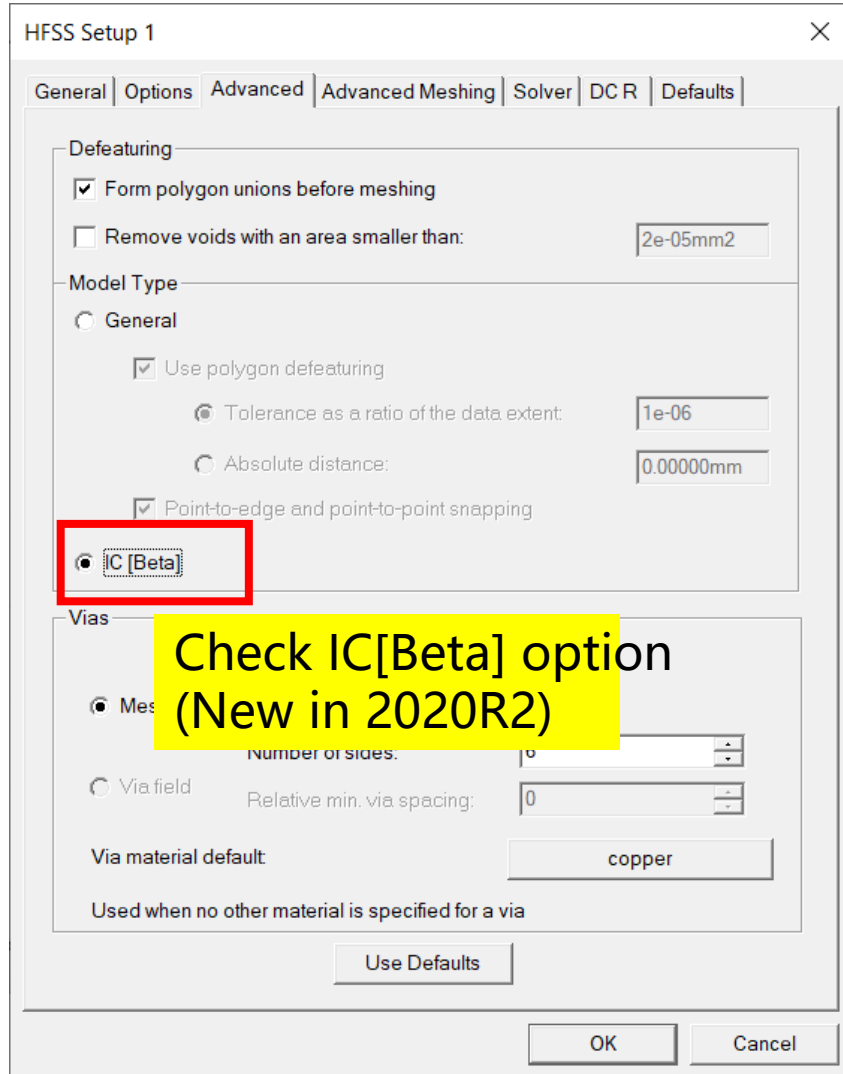


Edit Airbox

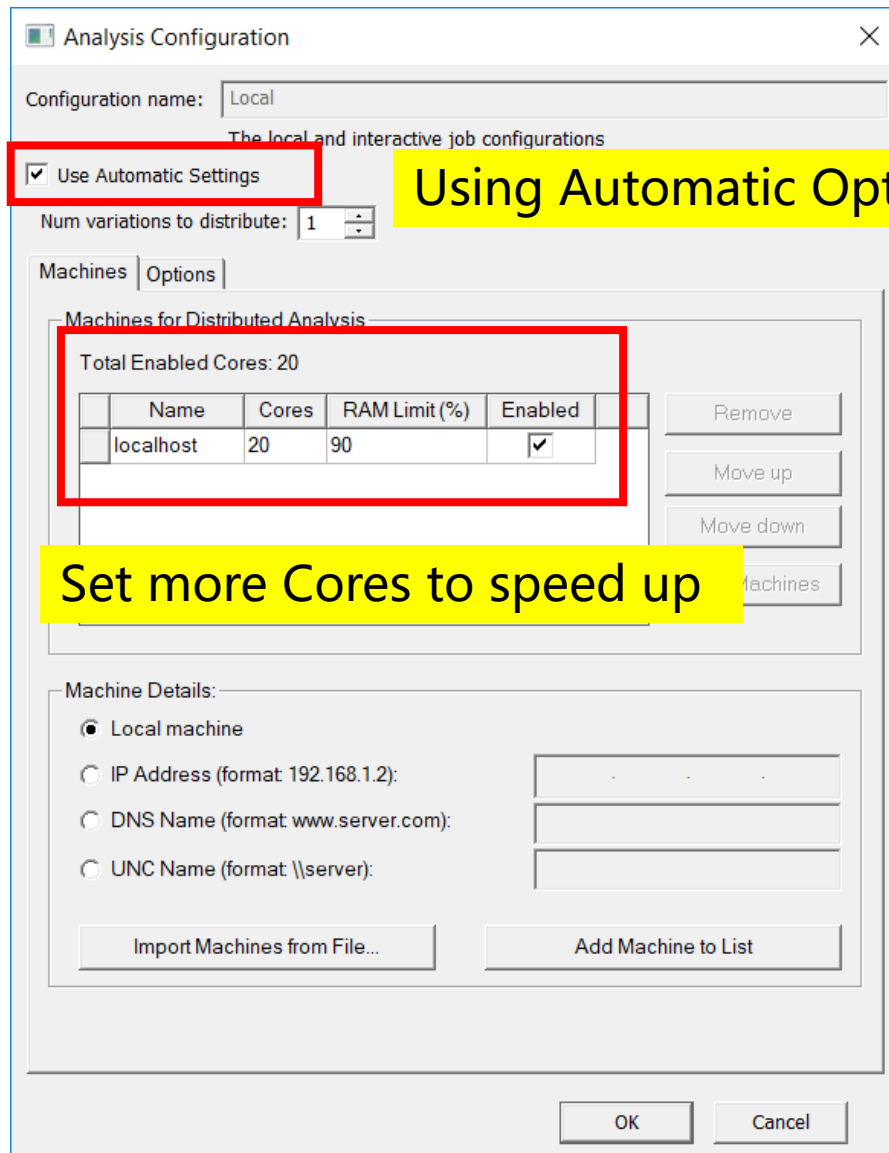
Show Airbox



HFSS Setup

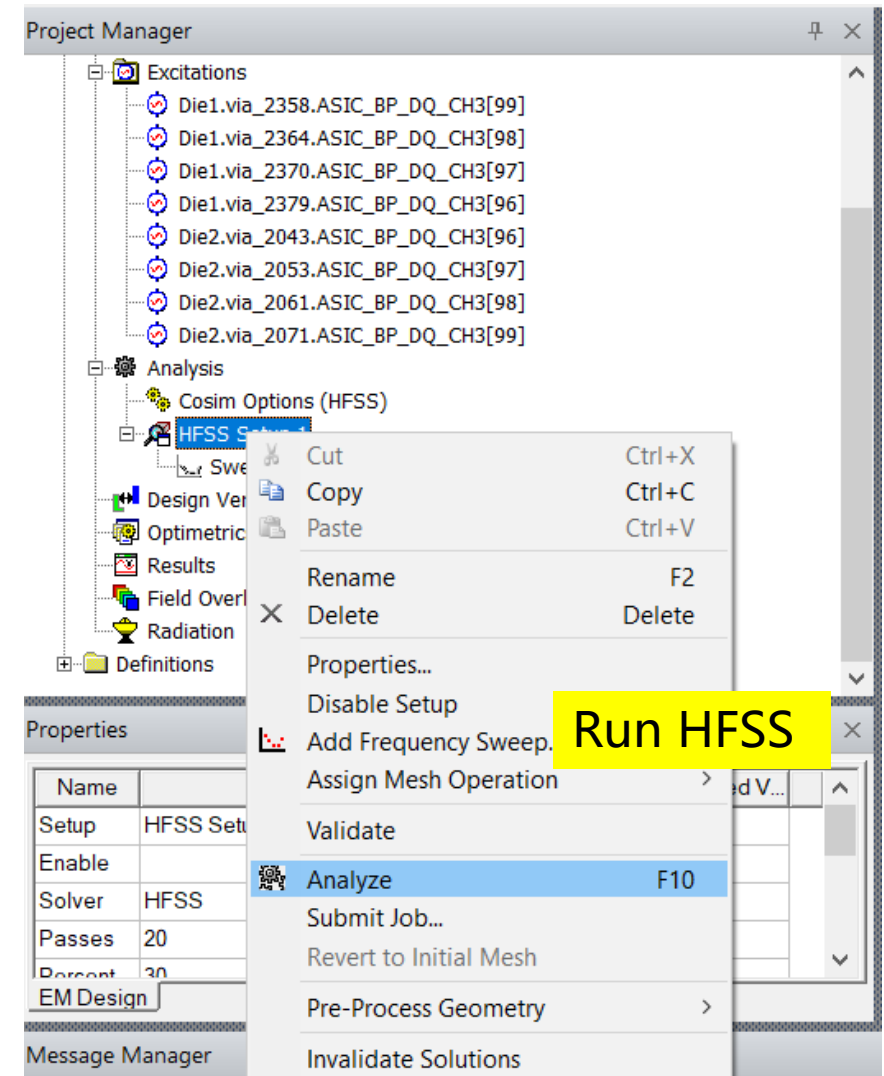


Run Simulation



Using Automatic Option

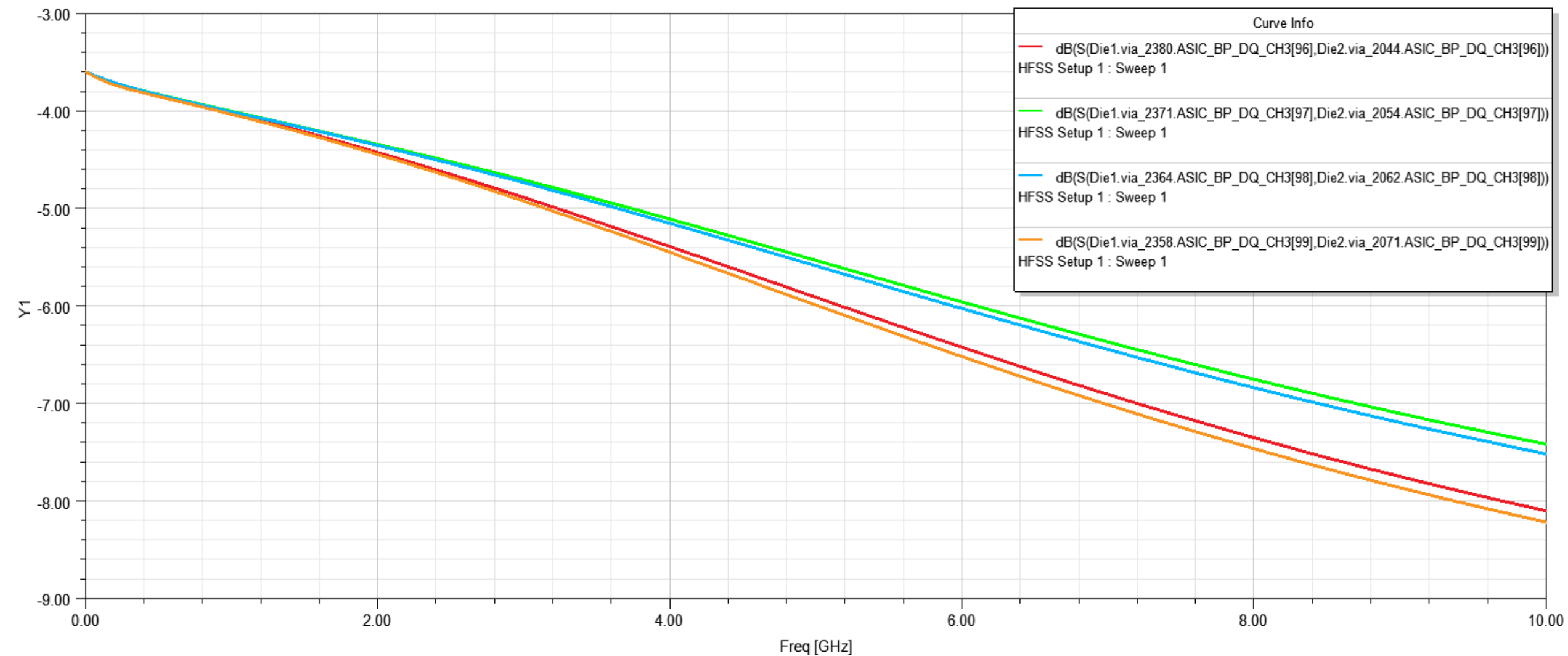
Set more Cores to speed up



Run HFSS

S Parameter Plot 1

interposer_cutout ANSYS





Running in Batch Mode

- *set aedtInstallPath=C:\Program Files\AnsysEM\AnsysEM20.2\Win64*
- *set gdsPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.gds*
- *set ircxPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\TSMC_INTERPOSER.ircx*
- *set path=%aedtInstallPath%\common\IronPython;%path%*
- *ipy64 GDSImportWizard.py -batch*
- Optional Setting
 - *set netlistPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.net*
 - *set xmlPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.xml*
 - *set edbPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.aedb*

/ Running in batch mode - Linux

Return

- *export aedtInstallPath='/home/ansys/app/AnsysEM20.1/Linux64'*
- *export gdsPath=/home/ansys/yguo/test/test.gds*
- *export ircxPath=/home/ansys/yguo/test/TSMC_INTERPOSER.ircx*
- *export ipy64="\$aedtInstallPath/common/mono/Linux64/bin/mono \$aedtInstallPath/common/IronPython/ipy64.exe"*
- *\$ipy64 GDSImportWizard.py -batch*
- Optional Setting
- `export netlistPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.net`
- `export xmlPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.xml`
- `export edbPath=D:\HFSS\GDSII\GDS2XML\TECH2XML_test\test.aedb`

 **Ansys**

