Design Name	Multi-core
Target FPGA Device	Cyclone IV GX EP4CGX150DF31I7AD
Logic Utilization	4-input LUTs: 18831 Reg: 13416
Memory Usage	0 for corelet since SRAMs are instantiated in core.v
Max Frequency	103.9 MHz
Power Estimate (mW)	291.9

Flow Summary

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Flow Status	Successful - Sat Dec 13 05:00:14 2025
Quartus Prime Version	25.1std.0 Build 1129 10/21/2025 SC Standard Edition
Revision Name	ece284_final_project_alpha4_corelet
Top-level Entity Name	ece284_final_project_alpha4_corelet
Family	Cyclone IV GX
Device	EP4CGX150DF31I7AD
Timing Models	Final
Total logic elements	18,831 / 149,760 (13 %)
Total registers	13416
Total pins	463 / 508 (91 %)
Total virtual pins	0
Total memory bits	0 / 6,635,520 (0 %)
Embedded Multiplier 9-bit elements	0 / 720 (0 %)
Total GXB Receiver Channel PCS	0 / 8 (0 %)
Total GXB Receiver Channel PMA	0 / 8 (0 %)
Total GXB Transmitter Channel PCS	0 / 8 (0 %)
Total GXB Transmitter Channel PMA	0 / 8 (0 %)
Total PLLs	0 / 8 (0 %)

Fitter Resource Utilization by Entity

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	Compilation Hierarchy Node	Logic Cells	Dedicated Logic Registers
1	|ece284_final_project_alpha4_corelet	18831 (0)	13416 (0)
1	|l0:l0_buffer|	2721 (26)	2183 (16)
2	|mac_array:mac_array_inst0|	5657 (384)	2680 (16)
3	|ofifo:ofifo_inst|	10251 (7)	8305 (1)
4	|sfp:sfp_inst|	378 (378)	248 (248)

Fitter Resource Usage Summary

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	Resource	Usage
1	▼ Total logic elements	18,831 / 149,760 (13 %)
1	-- Combinational with no register	5415
2	-- Register only	5313
3	-- Combinational with a register	8103
2		
3	▼ Logic element usage by number of LUT inputs	
1	-- 4 input functions	8371
2	-- 3 input functions	3347
3	-- <=2 input functions	1800
4	-- Register only	5313
4		
5	▼ Logic elements by mode	
1	-- normal mode	10656
2	-- arithmetic mode	2862
6		

* Register count does not include registers inside RAM blocks or DSP blocks.

Timing Closure:
This design contains failing setup paths with a worst-case slack of -8.621 ns. In the multi-core design, the worst failing setup path (WNS = −8.621 ns) is reported from the reg holding activation data in mac_tiles inside MAC array (mac_array…a*_q) to the output FIFO (ofifo…q). This indicates that the critical path is dominated by the MAC-array-to-OFIFO transfer, which includes the array's final registered outputs, the wide partial-sum bus routing, and the OFIFO input/memory read-write logic. Compared to the vanilla design, the multi-core wrapper increases the fanout and routing complexity of the partial-sum network because two arrays produce outputs in parallel and feed the OFIFO/accumulation pipeline concurrently. As a result, the interconnect delay and FIFO interface logic become timing-limiting, shifting the reported critical path boundary from an internal OFIFO pointer path to a datapath boundary that startes from MAC-array registers and ends at the FIFO. Importantly, this behavior is consistent with the observed frequency reduction (109.96 MHz → 103.9 MHz): the added parallelism improves throughput, but introduces additional routing load at the OFIFO boundary that slightly worsens worst-case slack. We avoided additional pipelining on this critical path because it lies on the steady-state 1-batch-per-cycle psum producing path, and adding pipeline stages would lead to bubbles that would weaken the strength of multi-core design in improving throughput.

Timing Closure Recommendations

Top Failing Paths

	Slack	From	To
1	-8.621	mac_array:mac_arr...instance|a1_q[1]mac_array:mac_array_inst0|mac_row:row_num[8].mac_row_instance|mac_tile:col_num[1].mac_tile_instance|a1_q[1]	ofifo:ofifo_inst|...instance|q14[15]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|q14[15]
2	-8.599	mac_array:mac_arr...instance|a0_q[1]mac_array:mac_array_inst0|mac_row:row_num[8].mac_row_instance|mac_tile:col_num[4].mac_tile_instance|a0_q[1]	ofifo:ofifo_inst|...instance|q59[14]ofifo:ofifo_inst|fifo_depth64:col_num[4].fifo_instance|q59[14]
3	-8.579	mac_array:mac_arr...instance|a1_q[1]mac_array:mac_array_inst0|mac_row:row_num[8].mac_row_instance|mac_tile:col_num[1].mac_tile_instance|a1_q[1]	ofifo:ofifo_inst|...instance|q14[15]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|q14[15]