Design Name	Vanilla
Target FPGA Device	Cyclone IV GX EP4CGX150DF31I7AD
Logic Utilization	4-input LUTs: 16865 Reg: 12224
Memory Usage	0 for corelet since SRAMs are instantiated in core.v
Max Frequency	109.96 MHz
Power Estimate (mW)	282.14

Flow Summary

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Flow Status	Successful - Fri Dec 12 19:46:37 2025
Quartus Prime Version	25.1std.0 Build 1129 10/21/2025 SC Standard Edition
Revision Name	ece284_final_project_corelet
Top-level Entity Name	ece284_final_project_corelet
Family	Cyclone IV GX
Device	EP4CGX150DF31I7AD
Timing Models	Final
Total logic elements	16,865 / 149,760 (11 %)
Total registers	12224
Total pins	430 / 508 (85 %)
Total virtual pins	0
Total memory bits	0 / 6,635,520 (0 %)
Embedded Multiplier 9-bit elements	0 / 720 (0 %)
Total GXB Receiver Channel PCS	0 / 8 (0 %)
Total GXB Receiver Channel PMA	0 / 8 (0 %)
Total GXB Transmitter Channel PCS	0 / 8 (0 %)
Total GXB Transmitter Channel PMA	0 / 8 (0 %)
Total PLLs	0 / 8 (0 %)

Fitter Resource Utilization by Entity

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	Compilation Hierarchy Node	Logic Cells	Dedicated Logic Registers
1	|ece284_final_project_corelet	16865 (0)	12224 (0)
1	▸ |l0:l0_buffer|	2643 (13)	2119 (8)
2	▸ |mac_array:mac_array_inst|	3720 (16)	1552 (16)
3	▸ |ofifo:ofifo_inst|	10265 (7)	8305 (1)
4	|sfp:sfp_inst|	378 (378)	248 (248)

Timing Closure:
This design contains failing setup paths with a worst-case slack of -8.094 ns. Timing analysis indicates that the critical path of the design lies within the output FIFO (OFIFO), specifically along the path from the read/write pointer update logic to the FIFO output data register. This path includes pointer arithmetic, full/empty comparison, address generation, and read logic, all of which must complete within a single clock cycle. Because the OFIFO sits directly on the main data path between the systolic array and the accumulation stages, it is triggered every cycle during execution and therefore dominates the timing behavior of the system. This timing limitation is not due to the MAC computation itself, which is fully pipelined and timing-clean, but rather due to FIFO control and memory access latency. While applying multi-cycle constraints or inserting additional pipeline stages in the OFIFO could alleviate timing pressure by shortening the critical path, such changes would require architectural modification of the dataflow. Since the OFIFO lies on the main execution path and is designed to deliver partial sums every cycle, increasing its effective latency would reduce the steady-state throughput unless additional buffering or retiming is introduced across the downstream accumulation pipeline.

Timing Closure Recommendations

Top Failing Paths

	Slack	From	To	Recommendations
1	-8.094	ofifo:ofifo_inst|...stance|wr_ptr[5]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|wr_ptr[5]	ofifo:ofifo_inst|..._instance|q38[4]ofifo:ofifo_inst|fifo_depth64:col_num[0].fifo_instance|q38[4]	Report recommendations for this path
2	-8.070	ofifo:ofifo_inst|...stance|wr_ptr[5]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|wr_ptr[5]	ofifo:ofifo_inst|..._instance|q54[4]ofifo:ofifo_inst|fifo_depth64:col_num[0].fifo_instance|q54[4]	Report recommendations for this path
3	-8.070	ofifo:ofifo_inst|...stance|wr_ptr[5]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|wr_ptr[5]	ofifo:ofifo_inst|...instance|q54[10]ofifo:ofifo_inst|fifo_depth64:col_num[0].fifo_instance|q54[10]	Report recommendations for this path
4	-8.054	ofifo:ofifo_inst|...stance|wr_ptr[5]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|wr_ptr[5]	ofifo:ofifo_inst|..._instance|q54[0]ofifo:ofifo_inst|fifo_depth64:col_num[0].fifo_instance|q54[0]	Report recommendations for this path
5	-8.054	ofifo:ofifo_inst|...stance|wr_ptr[5]ofifo:ofifo_inst|fifo_depth64:col_num[1].fifo_instance|wr_ptr[5]	ofifo:ofifo_inst|..._instance|q54[1]ofifo:ofifo_inst|fifo_depth64:col_num[0].fifo_instance|q54[1]	Report recommendations for this path