ECE284 FA25 Final Progress Report

1. Fill the table below. This helps us to understand your current progress status.

Item	Current Status	Status during Poster Presentation	Note
Part1	Complete	Complete	
Part2	Complete	Complete	
Part3	In Progress	In Progress	90% complete, WS mapping correct. need to fix order of sending OS weight/activation data in testbench
Alpha 1 (Ex: Tiling)	Complete	Complete	SkipBlock implementation to assist training and to improve gradient flow during pre-QAT training
Alpha 2	Complete	In Progress	PQT implementation for Bidirectional Encoder Representations from Transformers (BERT) model
Alpha 3 and 4	Complete	Complete	RTL Implementation and FPGA synthesis for multi-core wrapper for Tiled layer