

Ga-wun Kim

ENGR 250

Scott Koss

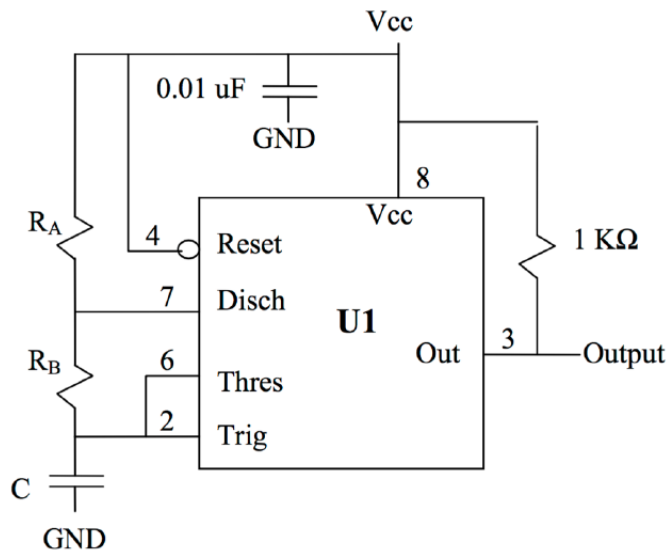
Lab Partners: Rebecca, Kantas

Digital Logic Design Lab #5

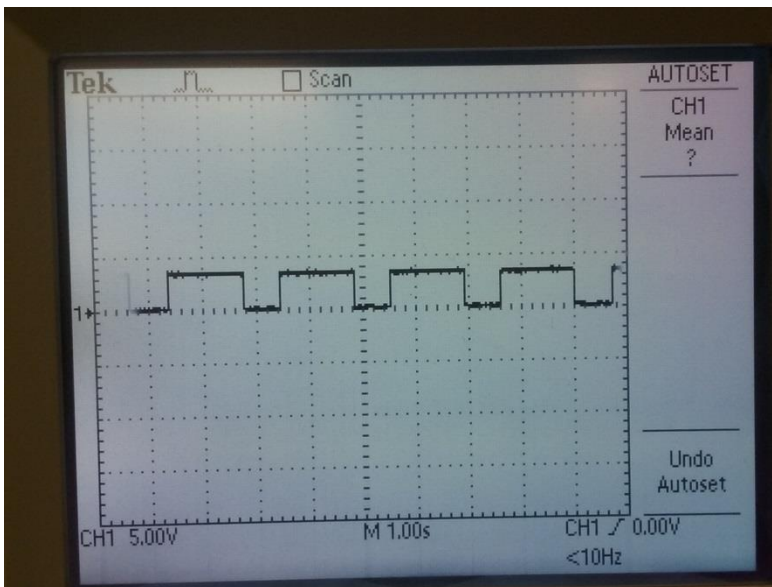
Introduction

In this lab, we used the three main objects: Clock chip (NE 555P), Binary counter chip (74LS93), 3-8 Decoder (74LS138). When we designed the circuits by using NE 555P chip, the 555P chip controlled the output that we set it diode. It made the diode turned on for 2 seconds and turned off. This cycle was kept going.

Experiment #1. NE 555P Astable Operation (Clock generator application)



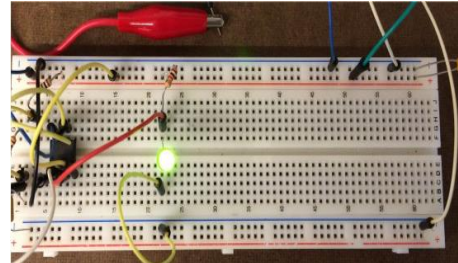
In this experiment, we used two 1 M Ω resistors, 0.01 μF capacitor, 1 μF capacitor, 1 k Ω resistor, and NE 555P chip. For checking whether this circuit work or not, we put the diode on the output. By this way, we could confirm it easily and after that we connected this circuit with the oscilloscope. From this device, we could know the clock time period.



T (High) : 1.5 sec

T (Low) : 0.5 sec

Above things are an approximation values

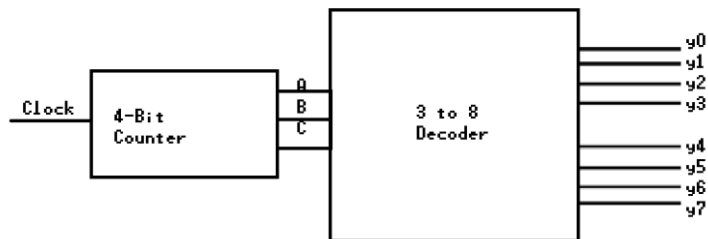


This (left) is the picture of the oscilloscope that is connected with the NE555P chip circuit.

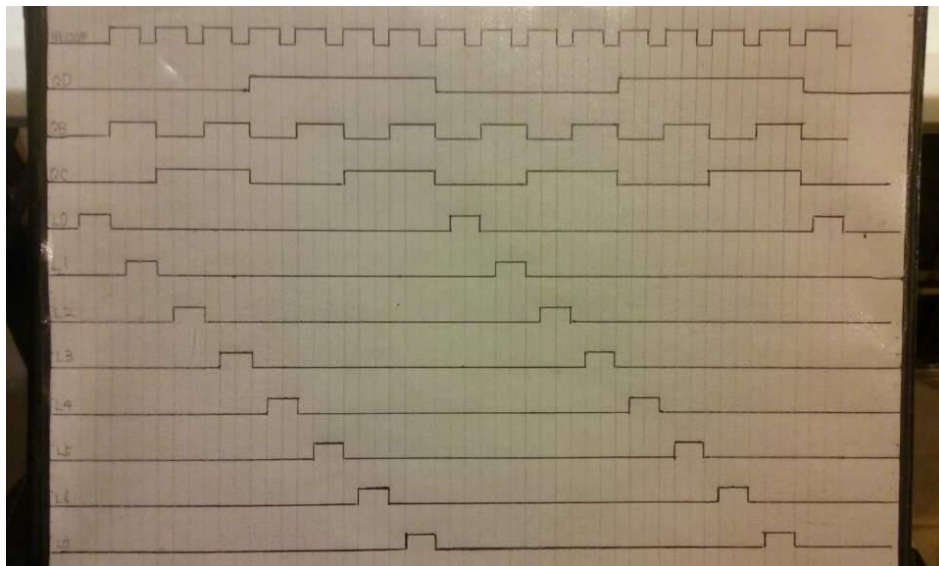
Experiment #2. Sequencing Light System

In this experiment, we used the clock circuit that we made before. Then, we added 4-binary counter and 3 to 8 decoder. In 3 to 8 decoder, we set diodes in each part of outputs.

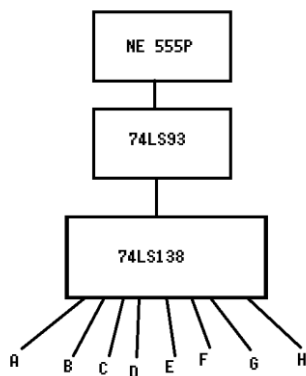
System Diagram



Time Diagram



Block Diagram



NE555P chip is connected with 4-binary counter (74LS93) and it is connected with 3-8 decoder. It produces eight outputs that are from A to H. Also, diodes are located each part.

Test plan

We set diodes in each part of output so that we could confirm output easily. We set nine outputs and these diodes turned on for 2 seconds and off, sequentially. In other word, the first diode turned on for 2 seconds and turned off, after that, the next diode turned on. However, the last one (#9 diode) did not turn on because the number of output is eight.

Signature

ENGR 250 Lab #5
11/22/2016
Rebecca Ann, Ga-wun Kim, Kantas Zilpys, Andrew Learing
Good Demo!
[Signature]

Experiment #3. Design of “2-bit binary adder with carry” using a PLD

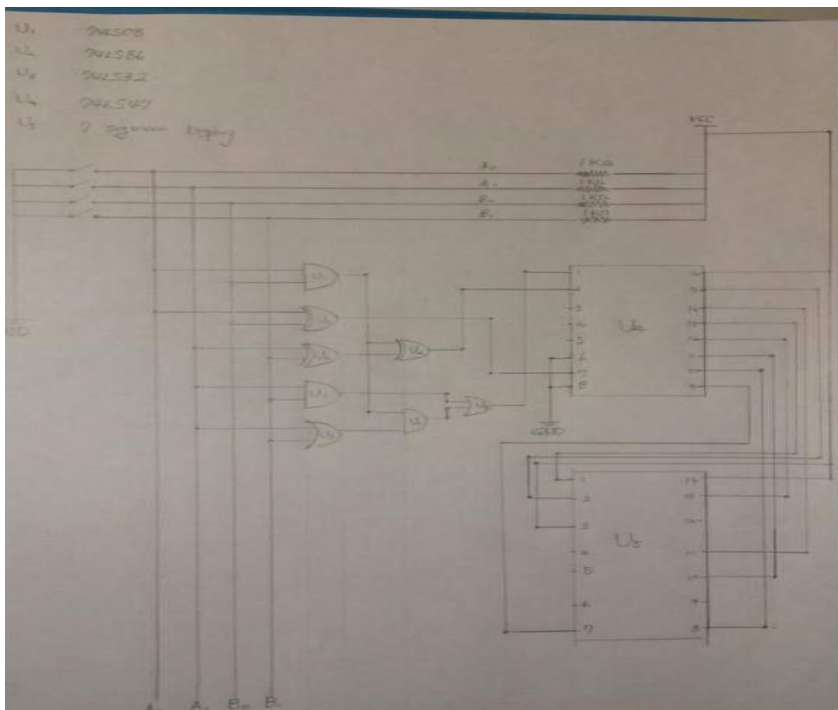
In this experiment, we used the Atmel ATF16V8B-15PU-ND. This is because it is more available rather than others and it is cheap price (around \$1.7 in each logic gate)

SOP functions

$$S0 = a0 \oplus b0$$

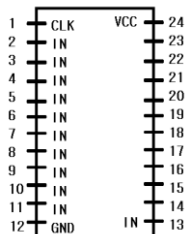
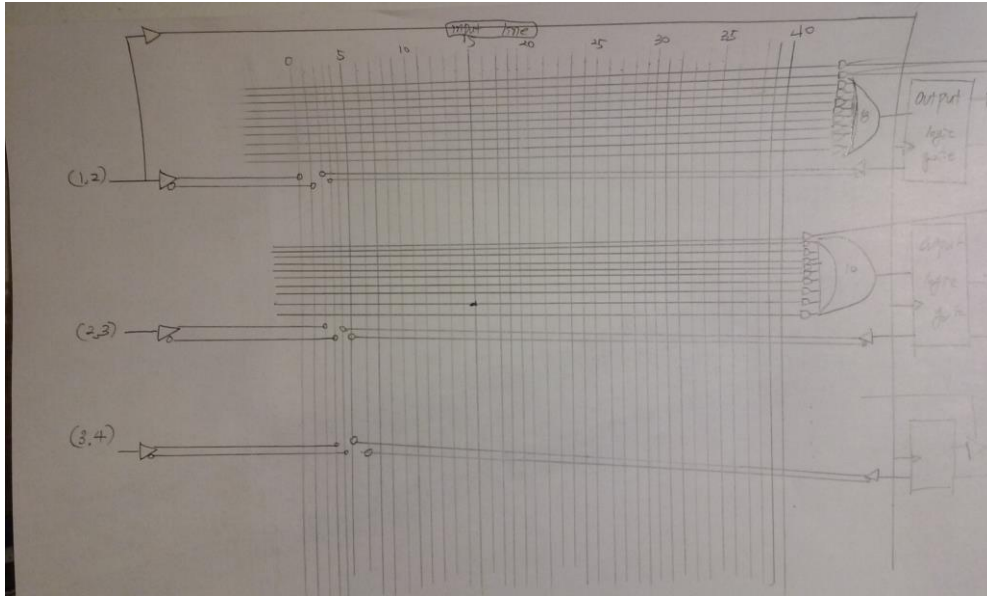
$$S1 = a0 \oplus b0 \oplus a0b0$$

$$S2 = a1b1 + a0b0 \cdot (a0 + b0)$$



Schematics

PLD fuse map



I draw just two specific logic gate (8 and 10) and there are three more gates (12, 14, and 16).

Learn from these experiments.

- I learned how to make clock circuit by using NE555P chip.
- I learned how to combine clock circuit, binary counter chip, and 3 to 8 decoder.

Conclusion (New experiment)

We used the NE 555P chip for the first time. Actually, when I learned about the clock by the textbook, I thought it would be consisted of just only one object. It means I assumed that I did not need to organize the clock circuit by using wires and other things. However, by this lab, I could realize that my first think was wrong and this experiment could be a chance to learn about the clock generator. This was very interesting experience and, by this lab, I could understand about the clock deeply and more.