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ENGR 250

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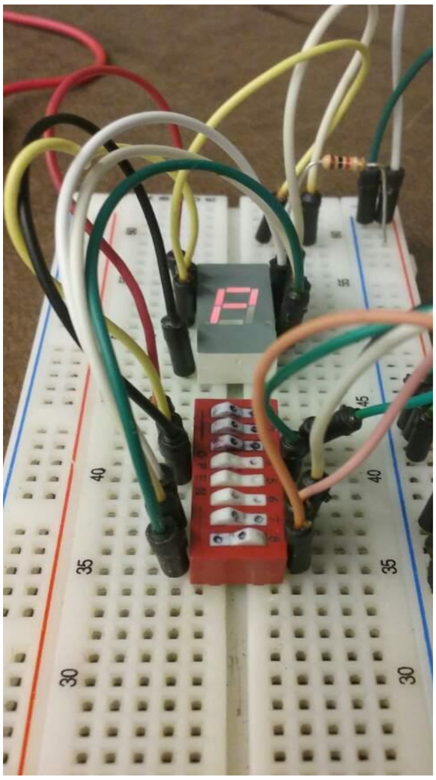
Digital Logic Design Lab #4

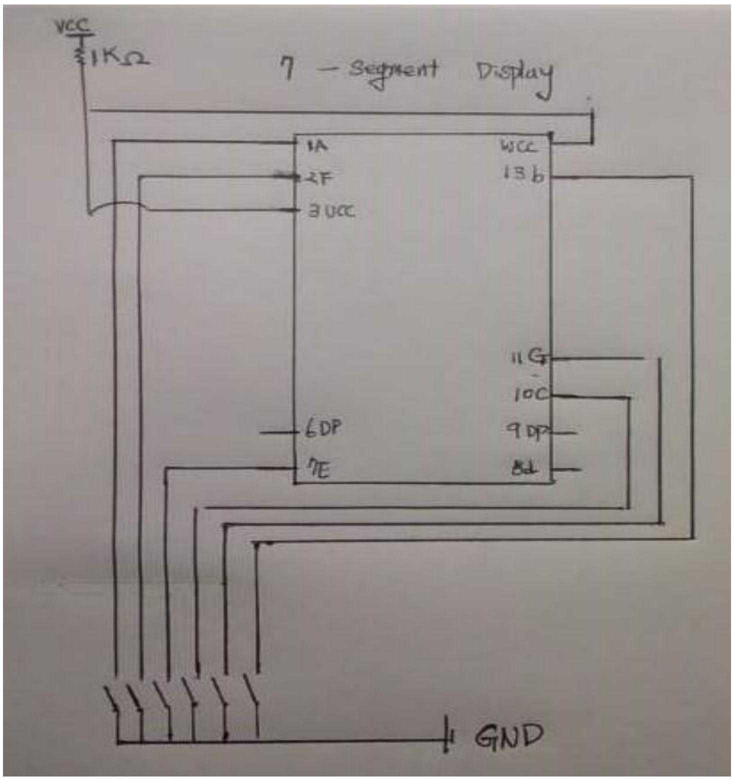
Introduction

In this lab, we used "the 7-Segment Display" and "BCD to 7-Segment Decoder/Driver (74LS47)" for the first time. At first, we took much of time to try to understand these items because we did not have any idea about that and this time was for getting familiar with them.

Experiment 1 – 7 Segment Design

In this experiment 1, we used the 7-Segment Display, wires, switch, resistor and proto-board. By changing the switch (by combination of each switch turn on and off), we could control the 7 LED in the 7 segment display. The below picture(left) is our circuit and (right) is the schematic of our circuit. The total forward current through all 8 diodes is I=V/R=5/1000=5mA.





Schematics

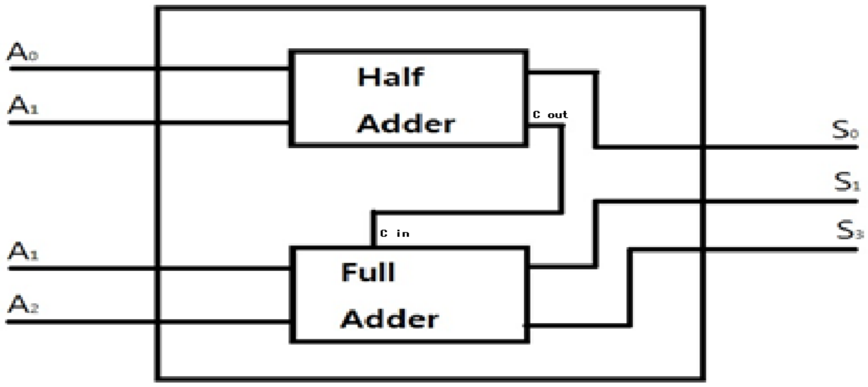
Experiment 2 – 2 bit Adder

In the experiment 2, building the two 2-bit binary input(a_1a_0 & b_1b_2) through switches and display the results of the addition in decimal format using the 7-segment display is the objective of this experiment.

A) The identified independent variables(input) and dependent variables(output) for the 2-bit binary adder system.

We divided the two things: More significant digits and less significant digits. We thought that A_0 and B_1 are more significant than A_1 and B_0.

In addition, this is the order of the significance : $S_0 < S_1 < S_2$



B) Truth Table

Full-Adder

A_1	B_1	C_{In}	S_1	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1		1	0	1
1	1	0	0	1
1	1	1	1	0

Half-Adder

gdasf

A_0	B_0	C_{out}	S_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Bit adder Truth table

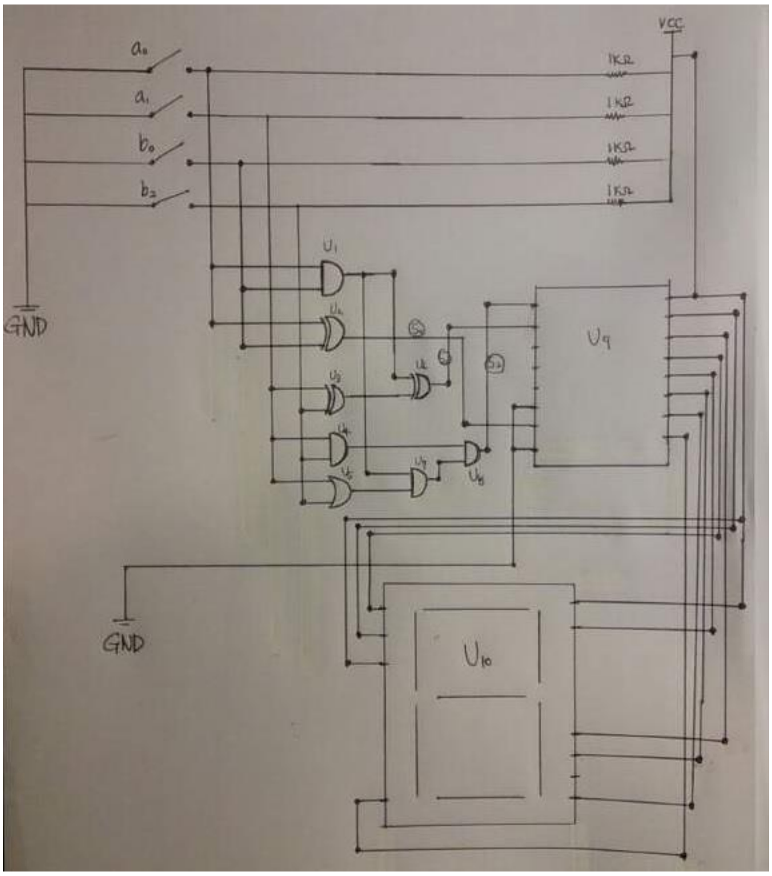
A_1	A_0	B_1	B_0	S_2	S_1	S_0
0	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**	**0**	**1**
0	**0**	**1**	**0**	**0**	**0**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**
0	**1**	**0**	**0**	**0**	**0**	**1**
0	**1**	**0**	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**	**1**	**1**
0	**1**	**1**	**1**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**1**
1	**0**	**0**	**1**		**1**	**1**
1	**0**	**1**	**0**	**1**	**0**	**0**
1	**0**	**1**	**1**	**1**	**0**	**1**
1	**1**	**0**	**0**		**1**	**1**
1	**1**	**0**	**1**	**1**	**0**	**0**
1	**1**	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**	**1**	**0**

This is the truth table of the half adder and the full adder, forming a 2-bit adder.

C) The minimized output functions

$S_0 = A_0 \oplus B_0$	literals: 2
$S_1 = A_0 \oplus B_0 \oplus A_0B_0$	literals: 4
$S_2 = A_1B_1 + A_0B_0\,(A_0 + B_0)$	literals: 6

D) Schematics



U (1, 4, 7, 8)	**AND**	**74LS08**
U (2 3 6)	**XOR**	**74LS86**
U (5)	**OR**	**74LS32**
U (9)	**BCD to 7-segment Decoder / Driver**	**74LS47**
U (10)	**7-Segment Display**	**-**

Learn from these experiments.

1. Learn about what is “the 7-Segment Display” and How to use that.
2. Learn about designing a 2-bit binary adder.
3. Confirmation of the truth table by the experiment with 7-segment display and two 2-bit binary input.

Conclusion (New experiment)

In the experiment 2, we built the circuit 4 times; because the previous circuits did not work well. This is because that was too complex to alter the small part of the circuit. Though we spent a lot of time to make the circuit, it was helpful to understand the circuit and the related conception, deeply. Also, during that time, we pondered the relationship between the switches and the display. It made us clarify the conception that we learned from book and instruction. In sum, this lab was the impressive experience to be able to handle the new device (7-segment display) and to organize the truth table with this device and switch.