ICSI 404 Unit Test 1

Yoon Young Jo

<add: opcode 1>
addimmediate r1 90 (91 5A) addimmediate r2 17 (92 11) add r1 r2 r3 (1123) interrupt 0 (8000) R1 == 90 R2 == 17 R3 == 107
<addimmediate: opcode 9>
addimmediate r1 75 (91 4B) addimmediate r1 27 (91 1B) interrupt 0 (8000) R1 == 102
<and: opcode 2>
addimmediate r1 40 (91 28) addimmediate r2 36 (92 24) and r1 r2 r3 (2 123) interrupt (8000) R1 == 40 //40 -> 0010 1000 (2) R2 == 36 //36 -> 0010 0100 (2) R3 == 32 //32 <- 0010 0000 (2)

<branchifequal : opcode 10>

addimmediate r1 84 (91 54)

store r1 r2 10 (F12A)

branchifequal r1 r2 6 (A1 20 00 06)

addimmediate r1 10 (91 0A)

addimmediate r2 5 (92 05)

addimmediate r3 20 (93 14)

interrupt 0 (8000)

If it works well	If it does not work
R1 == 84	R1 == 94
R2 == 84	R2 == 89
	R3 == 20

<branchifless: opcode 11>

addimmediate r1 85 (91 55)

addimmediate r2 34 (92 22)

branchifless r1 r2 2 (B1 20 00 02)

store r1 r3 10 (F23A)

addimmediate r1 12 (91 0C)

addimmediate r2 20 (92 14)

interrupt 0 (8000)

If it works well	If it does not work
R1 == 85	R1 == 97
R2 == 34	R2 == 54
	R3 == 85

<divide: opcode 3>
addimmediate r1 98 (91 62) addimmediate r2 14 (92 0E) divide r1 r2 r3 (3 123) interrupt 0 (8000)   R1 == 98 R2 == 14 R3 == 7
<halt: opcode 0>
halt (0 0 0 0) addimmediate r1 10 (910A) interrupt 0 (8000)   //If this print out R1 == 10 test halt is fail.
<interrupt: opcode 8>
addimmediate r1 0 (9100) interrupt 0 (8000)   R1 == 0

<iterateover: opcode 13>

Address	Value
24	12
28	97
32	50
36	8

addimmediate r1 24 (91 18)

addimmediate r2 12 (92 0C)

store r1 r2 0 (F 12 0)

subtract r1 r1 r1 (5 111)

subtract r2 r2 r2 (5 222)

addimmediate r1 28 (91 1C)

addimmediate r2 97 (92 61)

store r1 r2 0 (F 12 0)

subtract r1 r1 r1 (5 111)

subtract r2 r2 r2 (5 222)

addimmediate r1 32 (91 20)

addimmediate r2 50 (92 32)

store r1 r2 0 (F 12 0)

subtract r1 r1 r1 (5 111)

subtract r2 r2 r2 (5 222)

addimmediate r1 36 (91 24)

addimmediate r2 8 (92 08)

store r1 r2 0 (F 12 0)

subtract r1 r1 r1 (5 111)

subtract r2 r2 r2 (5 222)

addimmediate r1 24 (91 18)

load r2 r1 0 (E 21 0)

interrupt 0 (8000)

iterateover r1 4 4 (1101 0001 0000 0100 0000 0000 0000 0100) : (D104 0004)

load r2 r1 0 (E 21 0)

interrupt 0 (8000)

load r2 r1 0 (E 21 0)

interrupt 0 (8000)

load r2 r1 0 (E 21 0)

interrupt 0 (8000)

R1 == 24

R2 == 12

R1 == 28

R2 == 97

R1 == 32

R2 == 50

R1 == 36

R2 == 8

<jump: opcode 12>

addimmediate r1 43 (91 2B)

addimmediate r2 56 (92 38)

jump 8 (C0 00 00 08)

store r2 r3 10 (F 23 A)

addimmediate r1 30 (9 1 1E)

addimmediate r2 28 (9 2 1C)

addimmediate r3 4 (9 3 04)

interrupt 0 (8000)

If it works well	If it does not work
R1 == 43	R1 == 73
R2 == 56	R2 == 84
	R3 == 60

<leftshift: opcode 7>

addimmediate r1 84 (91 54)

leftshift r1 5 (0111 0001 00 0 00101) : (71 0 5)

interrupt 0 (8000)

//84 -> 0101 0100 (2)

//128 <- 1000 0000 (2)

R1 == 128

<load: opcode 14>
addimmediate r1 67 (91 43) load r1 r2 10 (E 12 A) interrupt 0 (8000) R1 == 67 R2 == 67
<multiply: opcode 4>
addimmediate r1 95 (91 5F) addimmediate r2 34 (91 22) multiply r1 r2 r3 (4 123) interrupt 0 (8000) R1 == 95 R2 == 34 R3 == 3230
<or: opcode 6>
addimmediate r1 77 (91 4D) addimmediate r2 41 (91 29) or r1 r2 r3 (6 123) interrupt 0 (8000) R1 == 77 //77 -> 0100 1101(2) R2 == 11 //11 -> 0000 1011(2) R3 == 79 //79 <- 0100 1111(2)

<rightshift: opcode 7>

addimmediate r1 15 (910F)

rightshift r1 3 (71 00 1 0 011) : (71 2 3)

interrupt 0 (8000)

R1 == 1

<store: opcode 15>

addimmediate r1 40 (91 28)

store r1 r2 10 (F12 A)

interrupt 0 (8000)

R1 == 40

R2 == 40

<subtract: opcode 5>

addimmediate r1 10 (910A)

addimmediate r2 4 (9204)

subtract r1 r2 r3 (5123)

interrupt 0 (8000)

R1 == 10

R2 == 4

R3 == 6