Laboratory No 5.

Design of a BJT Amplifier

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***Abstract*—This report outlines the design and development of a BJT amplifier using a 2N2222A npn transistor, adhering to specific gain, bandwidth, and input resistance requirements. The amplifier achieves a voltage gain of 50 V/V within a tolerance of ±10% and maintains a 3-dB bandwidth of at least 10 kHz while driving a 10 kΩ load. Designed to operate on a 9 V battery, the amplifier incorporates a bias network and demonstrates stable performance over varying temperature conditions. The report includes the design methodology, experimental setup, and performance evaluation.**

Keywords—BJT amplifier, 2N2222A transistor, voltage gain, temperature characteristics, NI ELVIS-II+

I. Introduction

The design of amplifiers is a fundamental topic in analog electronics, with practical applications in signal processing, communications, and instrumentation. This laboratory exercise focuses on designing and implementing a bipolar junction transistor (BJT) amplifier using a 2N2222A npn transistor to achieve specific design goals. The primary objective is to realize an amplifier with a voltage gain of 50 V/V ±10% and a 3-dB bandwidth of at least 10 kHz, meeting the practical requirements of modern analog systems.

The amplifier is designed to operate on a 9 V battery and drive a 10 kΩ load while maintaining an input resistance of 1 kΩ or greater. To ensure its suitability for real-world applications, the design must also amplify input signals with an RMS level of 1 V and demonstrate stability under varying temperature conditions. The laboratory emphasizes a free-form design approach, encouraging students to solve engineering problems creatively rather than following a prescribed sequence of steps.

II. Experiment Procedures and Analysis

Please note that the β value used throughout the lab experiment is 190, as it was found in a research paper [1].

A. Part 1: BJT Amplifier Circuit Design Calculation and Simulation

First, the following calculations were performed prior to running a simulation on LTspice to obtain the theoretical gain.

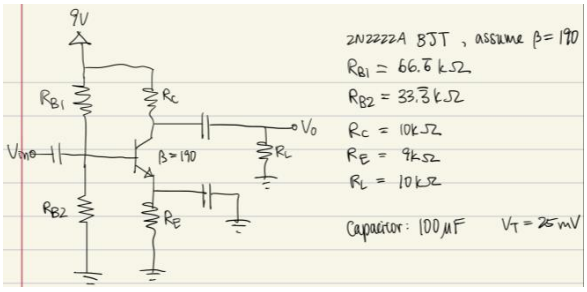

Figure 1.1: BJT amplifier circuit with temporary resistor and capacitor values for gain calculation

We can start the circuit analysis by doing the DC analysis.

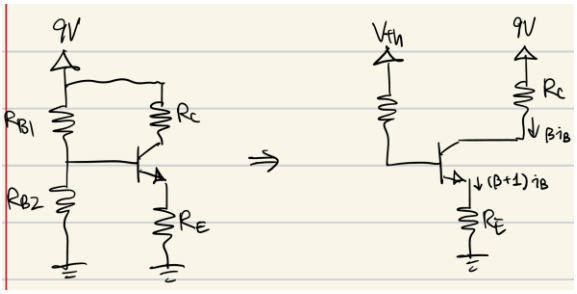

Figure 1.2: Thevenin equivalent circuit for DC analysis

The following calculations can be used to find the R_{th} and V_{th} values indicated in the figure above.

$$R_{th} = R_{B1}//R_{B2} = \frac{66.\bar{6} \times 33.\bar{3}}{66.\bar{6} + 33.\bar{3}} k\Omega = 22.\bar{2} k\Omega$$

$$V_{th} = 9V \times \frac{R_{B2}}{R_{B1} + R_{B2}} = 9V \times \frac{33.\bar{3}}{66.\bar{6} + 33.\bar{3}} = 3V$$

Then, we can proceed to calculate I_B, I_C, g_m and r_π.

$$V_E = (\beta + 1) I_B \times R_E$$

$$V_B = (\beta + 1) I_B \times R_E + 0.7$$

Also, $V_B = V_{th} - R_{th} \times I_B$

Therefore $(\beta + 1) I_B \times R_E + 0.7 = V_{th} - R_{th} \times I_B$

$$(190 + 1) I_B \times 9000 + 0.7 = 3 - 22222.\bar{2} \times I_B$$

$$I_B = 1.321 \mu A$$

Then $I_C = \beta I_B = 190 \times 1.321 \mu A = 251 mA$

$$g_m = \frac{I_C}{V_T} = \frac{251 mA}{0.025 V} = 0.01 \frac{A}{V}$$

$$r_\pi = \frac{V_T}{I_B} = \frac{0.025 V}{1.321 \mu A} = 18.925 k\Omega$$

After, we can continue with the small signal analysis to find the gain of the BJT amplifier circuit.

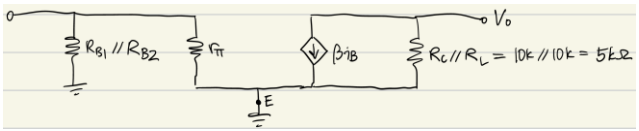

Figure 1.3: Circuit for small signal analysis

$$Gain = \frac{V_o}{V_{in}} = \frac{-\beta i_B (R_C // R_L)}{i_B r_\pi} = \frac{-\beta (R_C // R_L)}{r_\pi}$$

$$= \frac{-190(5000)}{18925} = -50.198 \frac{V}{V}$$

Here, the gain calculated is -50.198V/V. This value falls within 10% tolerance of the magnitude of the gain desired of 50V/V, and thus the capacitor and the resistor values used in the calculation are correct. The negative sign of the gain simply means that the sine wave of the signal is inverted. Note that the input resistance is greater than 1kΩ, which respects the instructions.

Now, the BJT amplifier circuit below was built and simulated on LTspice to verify the theoretical gain calculated of the BJT amplifier circuit designed. The voltage input V_{in} with an amplitude of 10mV and an offset of 0V at 10kHz was provided.

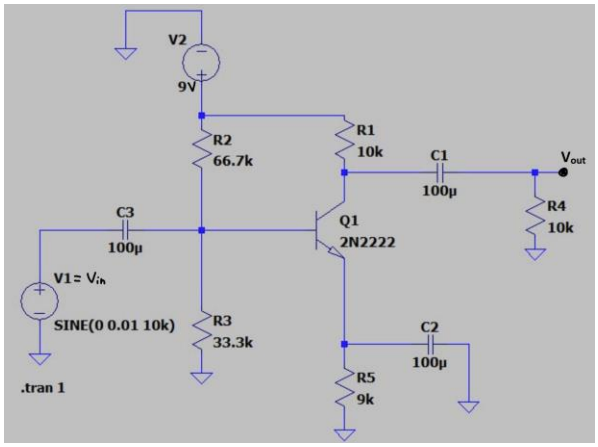

Figure 1.4: BJT amplifier circuit with 50V/V gain on LTspice

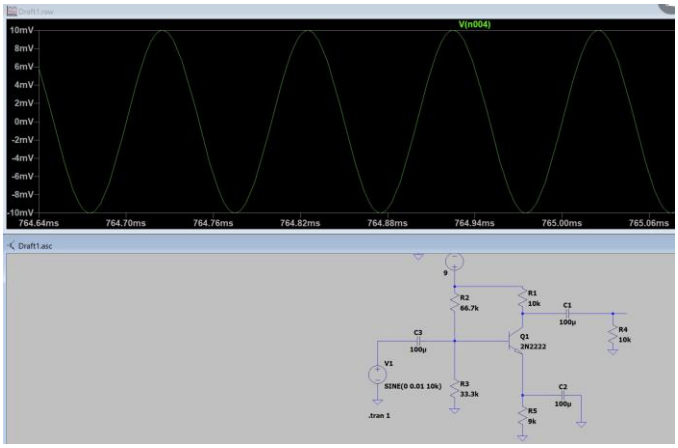

Figure 1.5: Simulation of V_{in} on LTspice

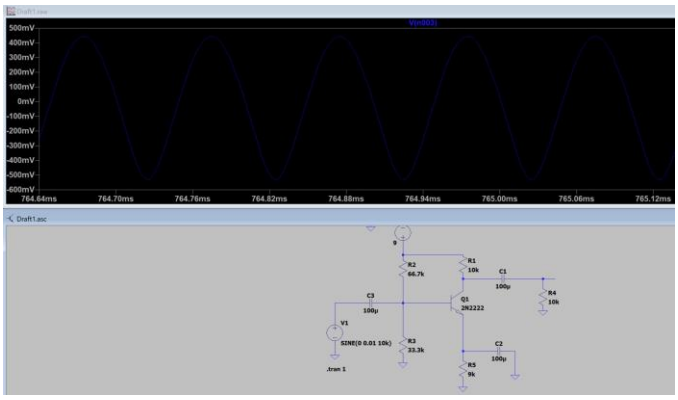

Figure 1.6: Simulation of V_{out} on LTspice

The peak-to-peak voltages of the input and the output signals were noted in the table below to find the gain. Note that the gain obtained from the simulation may differ from the value calculated since the BJT used in the simulation has a β value of 200, compared to the β value used in the earlier calculation of 190.

Table 1.1: V_{in} and V_{out} peak-to-peak values and gain

V_{in} peak-to-peak (in mV)	990
V_{out} peak-to-peak (in mV)	20
$gain = \frac{V_{out}}{V_{in}}$ (in V/V)	49.5

Again, the gain falls within 10% tolerance of the magnitude of the gain desired of 50V/V, and thus the capacitor and the resistor values used in the simulation are correct. We can now start the experiment on the NI ELVIS-II+ board to find the gain from the practical experiment.

B. Part 2: BJT Amplifier Circuit Design Practical Experiment

The original input voltage amplitude of 10 mV used in earlier calculations was insufficient to produce accurate results. Consequently, a slightly larger input voltage was applied using a function generator. The circuit was tested first with a frequency of 1kHz, then with 10kHz to verify that the amplifier is capable of performing amplification over a 10kHz bandwidth. Additionally, a variable power supply replaced the 9V battery for powering the circuit. This substitution was made because the measured voltage of the 9V battery was actually 9.3V once measured, and a variable power supply provided a more precise measurement for determining the amplifier gain.

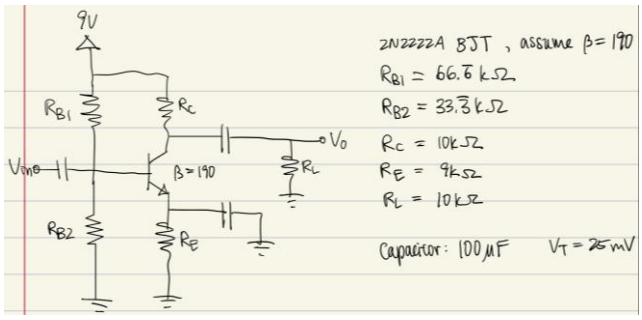

Figure 2.1: BJT amplifier circuit design

CH0 of the oscilloscope was used throughout the lab experiment to measure the input voltage V_{in}, and CH1 of the oscilloscope was used to measure the output voltage V_o. First, the frequency of the input voltage was set to 1kHz with an amplitude of 40mV and an offset voltage of 0V. Then, the frequency of the input voltage was changed to 10kHz.

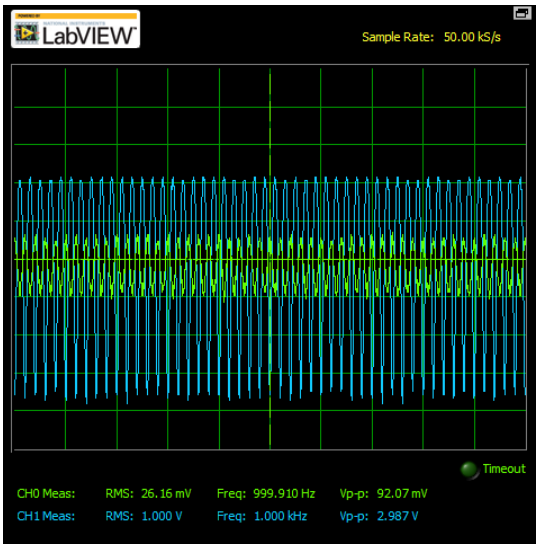

Figure 2.2: Output response of the amplifier circuit at 1kHz

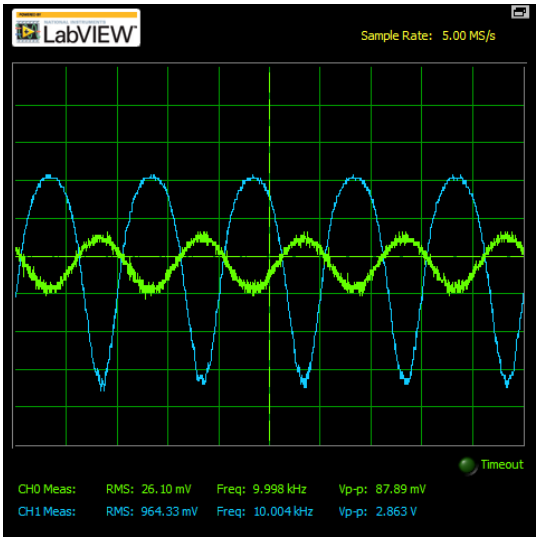

Figure 2.3: Output response of the amplifier circuit at 10kHz

Table 2.1: Gain from practical experiment

Frequency (in kHz)	1	10
RMS (in V)	1.000	0.964
V_{in} peak-to-peak (in mV)	92.07	87.89
V_{out} peak-to-peak (in mV)	2987	2863
$gain = \frac{V_{out}}{V_{in}}$ (in V/V)	32.44	32.57

The RMS level for both frequencies were approximately 1V, which respects the instructions. Notice that for both frequencies, the gain is found to be approximately 32.5 V/V. We can conclude that the change in frequency from 1kHz to 10kHz in our circuit design mas no impact on the gain. However, this gain is not within 10% tolerance of the magnitude of the gain desired of 50V/V.

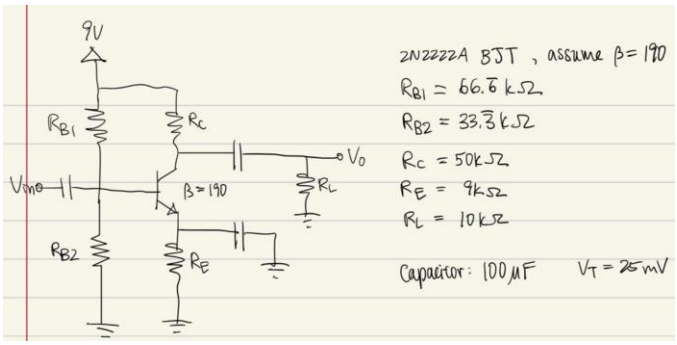

Figure 2.4: Updated BJT amplifier circuit design

According to the gain formula of the circuit amplifying circuit, $Gain = \frac{V_o}{V_{in}} = \frac{-\beta i_B (R_C // R_L)}{i_B r_\pi} = \frac{-\beta (R_C // R_L)}{r_\pi}$, increasing R_C would give a gain of 50V/V given that R_L must be 10kΩ. The old R_C of 10kΩ was thus replaced by a new R_C of 50kΩ, and the results were captured using an oscilloscope.

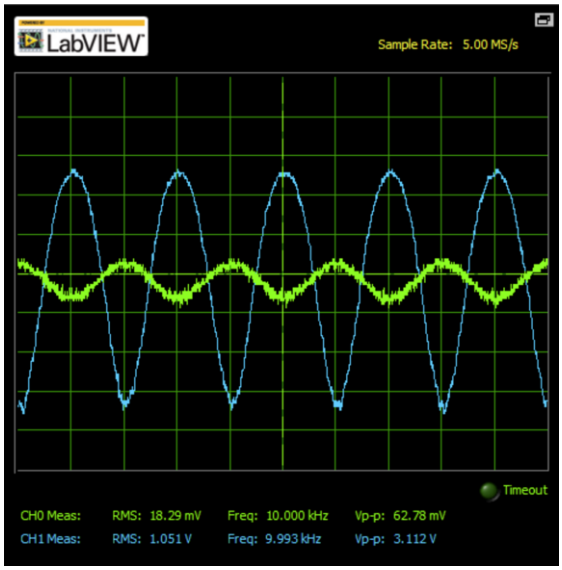

Figure 2.5: Output response of the amplifier circuit at 10kHz with a new R_C of 50kΩ

The discrepancy between the theoretical and practical gain values can be attributed to several real-world factors that are not accounted for in ideal calculations. Theoretical calculations assume perfect components and ideal conditions, while practical experiments involve non-idealities such as parasitic resistances, tolerances in resistor and capacitor values, and variations in the transistor's β (current gain).

Additionally, loading effects caused by the oscilloscope and other connected devices reduce the overall gain by lowering the effective impedance of the circuit. Internal resistances, such as the emitter resistor R_E and the base resistance of the BJT, also contribute to voltage drops, which counteract the amplification.

Furthermore, at higher frequencies, parasitic capacitances within the BJT and other components can affect the gain by introducing reactance, further deviating from theoretical predictions. Replacing the collector resistor R_C with a higher value of 50kΩ increased the output voltage swing by reducing

the collector current, thereby aligning the practical gain more closely with the theoretical value of approximately 50V/V. This highlights the importance of accounting for real-world non-idealities in circuit design and optimization.

Table 2.2: Gain from practical experiment with new R_C of 50kΩ

Frequency (in kHz)	10
RMS (in V)	1.051
V_{in} peak-to-peak (in mV)	62.78
V_{out} peak-to-peak (in mV)	3112
$gain = \frac{V_{out}}{V_{in}}$ (in V/V)	49.57

The RMS level is approximately 1V, and the gain obtained is 49.57V/V, which falls within 10% tolerance of the magnitude of the gain desired of 50V/V.

Lastly, notice how there is a slight distortion in the V_{out} (CH1) waves captured by the oscilloscope in *figure 2.5*. The distortion observed in the output waveform of the BJT amplifier can be attributed to several factors related to the circuit design and the operating characteristics of the transistor. The negative peaks of the output waveform show clipping, while the positive peaks appear to flatten. These effects suggest that the transistor is not operating entirely within the linear active region.

The clipping at the negative peaks of the output is likely due to the BJT entering the cutoff region. When the input voltage becomes sufficiently low, the base-emitter junction of the transistor is no longer forward-biased, causing the transistor to turn off momentarily. As a result, the output voltage cannot track the input voltage during these periods, leading to distortion at the negative peaks.

On the other hand, the flattening observed at the positive peaks of the output waveform indicates that the transistor is entering saturation. In the saturation region, the collector-emitter voltage V_{CE} drops to a very low value, and the output voltage is limited by this saturation condition. This restricts the maximum positive voltage swing of the output signal, resulting in the observed flattening effect.

These distortions can also be influenced by improper biasing of the circuit. If the quiescent operating point (Q-point) of the transistor is not centered in the active region, the transistor may operate closer to cutoff or saturation, causing asymmetry in the output signal. Additionally, the limited voltage swing imposed by the power supply voltage, combined with the chosen values of R_C and R_E, may exacerbate the clipping and flattening effects when the input signal amplitude is too large.

To minimize these distortions, the circuit design could be improved by adjusting the biasing resistors to ensure that the Q-point is properly centered in the active region. This adjustment would allow the transistor to handle larger signal amplitudes without entering cutoff or saturation. Furthermore, reducing the input signal amplitude can ensure that the transistor remains within its linear operating range. If feasible, increasing the power supply voltage could also help accommodate a larger output voltage swing and reduce distortion.

C. Part 3: MOSFET Temperature Effets

In part 3 of the lab, the same BJT amplifier circuit as part 1 and 2 is analyzed. However, the BJT will be under different temperature conditions to analyze how different BJT temperatures affect the gain. The function generator will be set to generate a sinusoidal waveform with peak-to-peak voltage of 60mV with an offset of 0V, at a frequency of 10kHz.

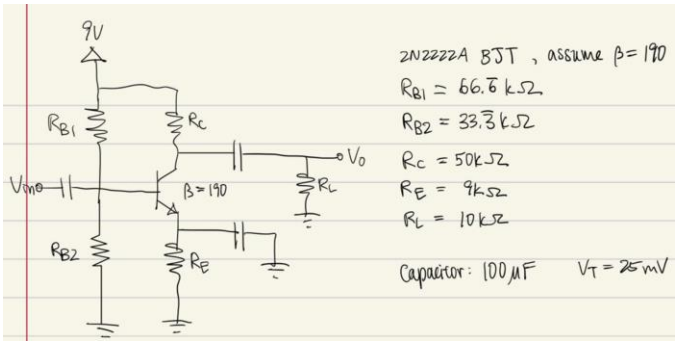

Figure 3.1: Updated BJT amplifier circuit design

The measurements were first taken at room temperature (27 °C), then at cold (3 °C) and hot 50 °C) temperatures using a freeze spray and a hot-air blowgun. The temperature of the BJT was recorded using a hand-held thermal imager. The gain calculations ($gain = \frac{V_{out\ peak-to-peak}}{V_{in\ peak-to-peak}}$) for each temperature are shown in the figure below, obtained using MATLAB.

```
for k = 1:length(files)
    % Read the data from the file
    transData = readTextFile(files(k), "scope");
    vin = transData.ValueCh0; % Vin signal
    vout = transData.ValueCh1; % Vout signal

    % Calculate peak-to-peak values for Vin and Vout
    vin_pp = max(vin) - min(vin); % Peak-to-peak for Vin
    vout_pp = max(vout) - min(vout); % Peak-to-peak for Vout

    % Calculate gain
    gains(k) = vout_pp / vin_pp; % Gain = Vout_pp / Vin_pp
end
```

Figure 3.2: Snippet of MATLAB code for gain calculation

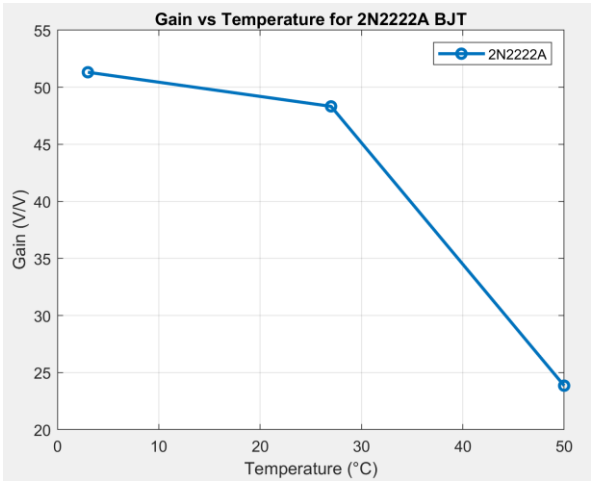

Figure 3.3: Gain vs temperature plot generated from MATLAB

Table 3.1: Data points of the gain vs temperature plot where X represents temperature (in °C) and Y represents gain (in V/V)

3°C	27°C	50°C
X 3 Y 51.313	X 27 Y 48.3246	X 50 Y 23.8525

The measured gain values were 51.313 V/V at 3°C (cold temperature), 48.3246 V/V at 27°C (within the desired range at room temperature), and 23.8525 V/V at 50°C (hot temperature). These results show a clear trend: the gain decreases as the BJT's temperature increases. This behavior aligns with theoretical predictions, as the transistor's thermal characteristics directly affect its performance.

At higher temperatures, the base-emitter voltage V_{BE} required to forward bias the transistor decreases, resulting in a higher collector current for a given base current. This increase in collector current causes a reduction in the small-signal current gain (β) due to increased carrier recombination within the transistor. Consequently, the overall voltage gain, which is proportional to β, diminishes with rising temperature. Additionally, higher temperatures lead to increased thermal noise, which can further degrade the signal-to-noise ratio and reduce the effective gain.

III. Conclusion

This laboratory exercise successfully demonstrated the design, implementation, and evaluation of a BJT amplifier using the 2N2222A npn transistor. The amplifier met the design objective of achieving a voltage gain of 50 V/V within a 10% tolerance after adjusting the collector resistor R_C. The experimental results highlighted the importance of considering real-world factors, such as parasitic resistances, component tolerances, and loading effects, which can cause deviations from theoretical predictions. Additionally, the influence of temperature on the amplifier's performance was analyzed, revealing a clear trend of reduced gain with increased operating temperature due to changes in the transistor's characteristics.

The laboratory also emphasized the practical challenges of biasing and operating point stability to ensure linear amplifier operation. Observations of waveform distortion underscored the necessity of proper biasing and careful input signal management to minimize non-linear effects such as cutoff and saturation. Overall, the experiment provided a comprehensive understanding of BJT amplifier design, including the theoretical principles, practical implementation, and performance optimization under varying conditions.

This lab reinforced critical concepts in analog circuit design and highlighted the importance of balancing theoretical calculations with practical considerations. The results obtained serve as a foundation for future explorations of amplifier applications in real-world systems.

References

[1] D. F. Schroeter, J. S. Franklin, and J. M. Essick, "Determining β for a 2N2222 transistor," Reed College, Portland, OR, Oct. 7, 2010. [Online]. Available: https://studylib.net/doc/18086821/determining-%CE%B2-for-a-2n2222-transistor