Laboratory No 4.

MOSFETs and BJTs DC Characteristics

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***Abstract*—This lab investigates the DC characteristics of MOSFETs and BJTs, including their i-v relationships and temperature-dependent behaviors. Using the NI ELVIS-II+ platform, the iD-vDS characteristics of an NMOS transistor and the iC-vCE characteristics of an npn BJT are analyzed under varying conditions. Temperature effects are explored by applying freeze spray and heat to the transistors, assessing changes in operational parameters. Transconductance and Early voltage are computed to understand device performance. These experiments highlight key principles in designing biasing networks and understanding the influence of thermal variations in semiconductor devices.**

Keywords—electronics, MOSFET, BJT, i-v Characteristics, Transconductance, Early Voltage, Temperature Effects, NI ELVIS-II+, Biasing Networks, Semiconductor Devices

I. Introduction

Transistors, specifically MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) and BJTs (Bipolar Junction Transistors), are fundamental components in modern electronic circuits. Understanding their operational characteristics is crucial for designing reliable and efficient systems. This laboratory aims to explore the DC i-v characteristics of MOSFETs and BJTs, analyze their performance under varying thermal conditions, and calculate essential parameters such as transconductance and Early voltage.

The experiment utilizes the NI ELVIS-II+ platform, a versatile tool integrating multiple instrumentation functionalities. The setup includes a curve tracer for observing iD-vDS and iC-vCE characteristics. Furthermore, temperature effects on these characteristics are examined using a heat gun and freeze spray, providing insights into the thermal behavior of transistors. Such knowledge is essential in real-world applications where environmental conditions can impact circuit performance.

By integrating hands-on circuit building with theoretical analysis, this lab bridges the gap between classroom knowledge and practical application, reinforcing concepts in transistor biasing and semiconductor behavior under different operating conditions.

II. Experiment Procedures and Analysis

A. Part 1: MOSFET i_D-v_{DS} Characteristics Using a Curve Tracer

The following curve tracer circuit was constructed using a 741 op-amp and the BS170 NMOS transistor. A function generator was used to provide a sawtooth waveform ranging from 0V to 10V to the circuit, meaning that the input voltage v_{in} has a peak-to-peak voltage of 10V with an offset voltage of 5V. Furthermore, the wiper of a 10kΩ potentiometer was connected to the gate terminal of the transistor. The circuit is as seen in the diagram below.

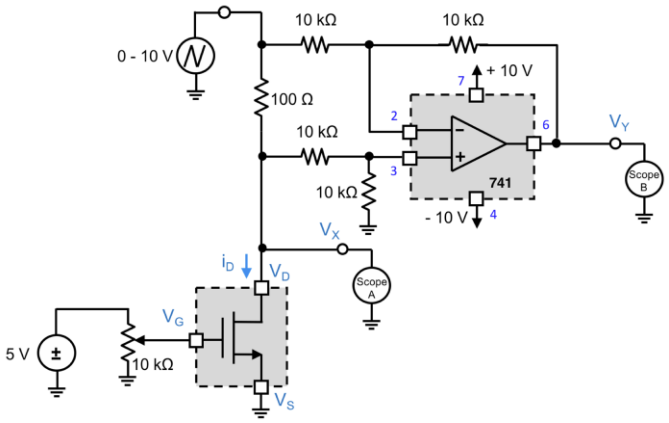

Figure 1.1: Curve tracer circuit for measuring MOSFET i-v characteristics

In the lab, Channel 0 (CH0) of the oscilloscope corresponds to V_x (Scope A), while Channel 1 (CH1) corresponds to V_Y (Scope B). V_X measures the drain-source voltage V_{DS}. Since V_Y is scaled up to be 100 times larger than the actual current (i_D), it must be divided by 100 to obtain the true current value. For example, as shown in *Figure 1.2*, the multimeter measures the gate voltage V_G to be approximately 0.062mV, which is effectively 0V. The CH1 reading on the oscilloscope, after being divided by the scaling factor of 100, results in a drain current of $i_D = \frac{7.20\times10^{-3}}{100} \approx 0A$. This confirms that with the gate voltage V_G set to zero, the drain current i_D is zero while the drain-source sweeps from 0 to 10V.

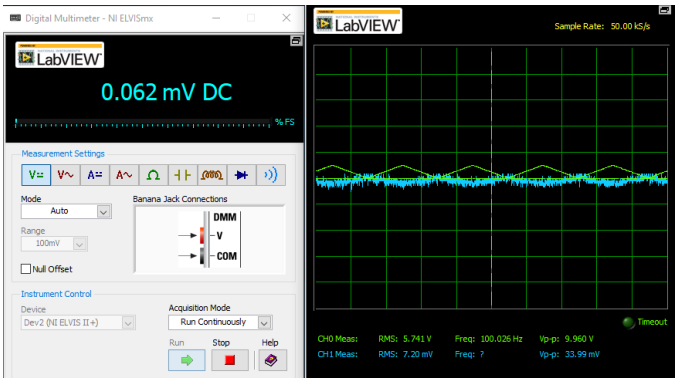

Figure 1.2: Measurement of gate voltage (V_G), V_X (V_{DS}), and V_Y

Next, it was verified that the threshold voltage is approximately 2V. The screw of the potentiometer was adjusted to allow for the current to flow. As seen in *Figure 1.3*, current started to appear at 2.12V, which is approximately 2V. It is

possible to know that the current started flowing at this point because the frequency reading of CH1 of the oscilloscope went from unknown to approximately 100Hz, which is identical to the frequency of the input sawtooth voltage.

The slight difference (100mV) between the expected threshold voltage and the actual threshold voltage could be a result of manufacturing variations, temperature effects, measurement inaccuracies, or parasitic elements in the circuit affecting the applied gate voltage.

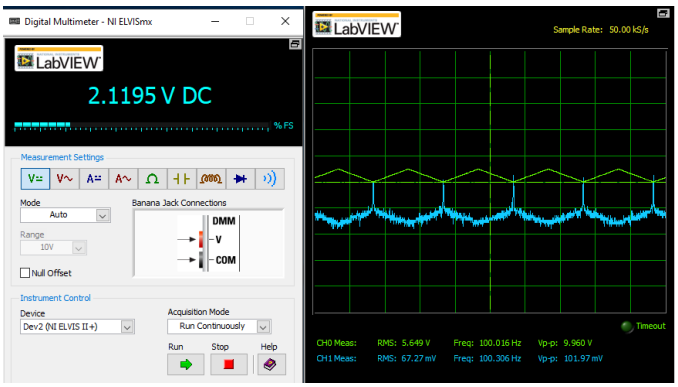

Figure 1.3: Measurement of threshold voltage, V_G=2.12V

Then, the gate voltage V_G was incremented by 0.5V until 5V by adjusting the potentiometer in order to calculate the i_D-v_{DS} characteristics (see *Figure 1.4* to *1.9*). Note that the highest gate voltage measurable was 4.9V.

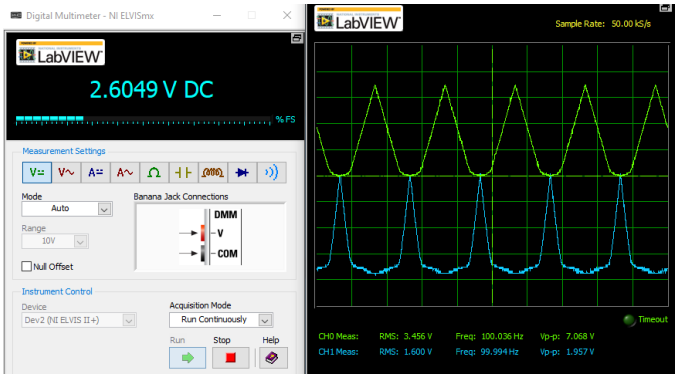

Figure 1.4: Measurement taken at V_G=2.6V

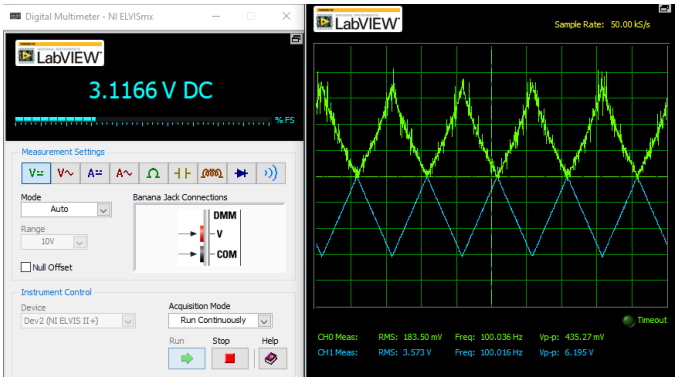

Figure 1.5: Measurement taken at V_G=3.1V

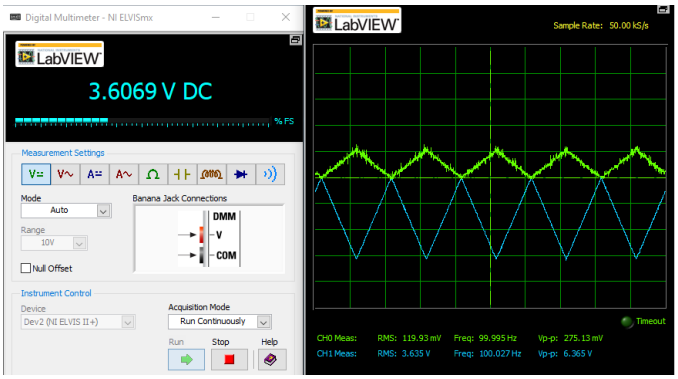

Figure 1.6: Measurement taken at V_G=3.6V

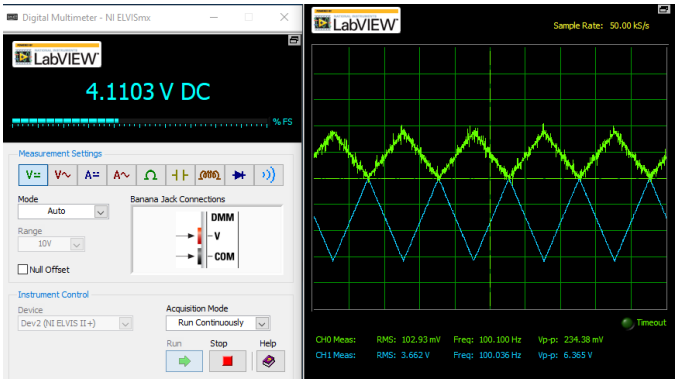

Figure 1.7: Measurement taken at V_G=4.1V

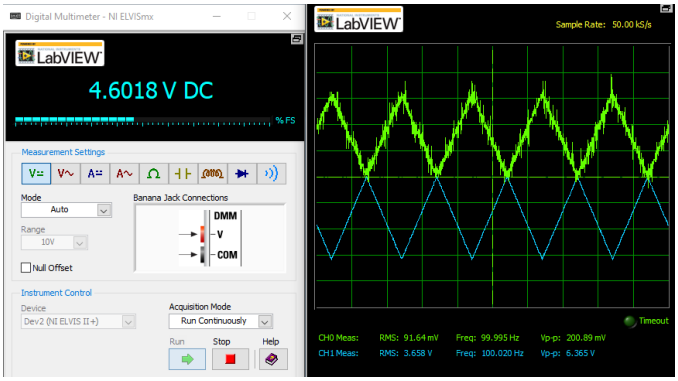

Figure 1.8: Measurement taken at V_G=4.6V

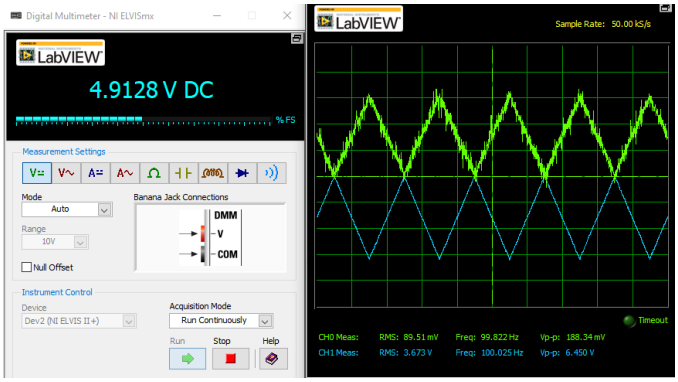

Figure 1.9: Measurement taken at V_G=4.9V

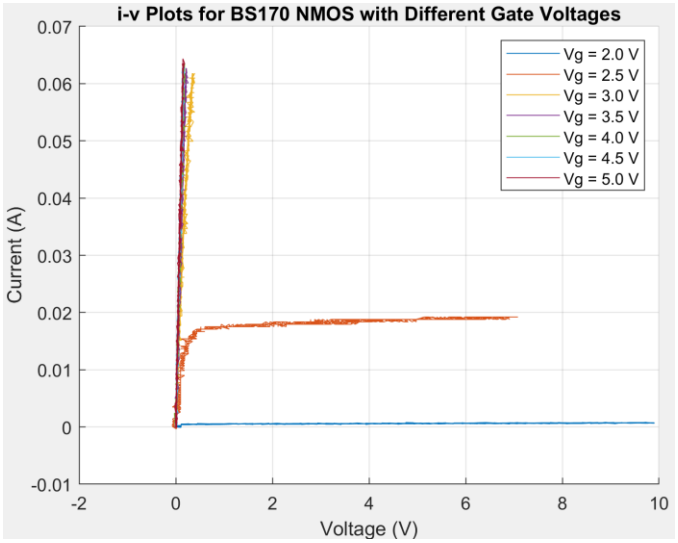

Figure 1.10: i_D-v_{DS} plot generated using Matlab at different gate voltages

The i_D-v_{DS} characteristics of the BS170 NMOS transistor were analyzed at different gate voltages (V_G). For V_G=2.0V, the drain current (i_D) remained negligible throughout the v_{DS} range, indicating that the NMOS was operating below its threshold voltage (note that the threshold voltage measured is 2.1V). As V_G increased to values greater than 2.0 V, the device entered the conduction region. For $V_G \geq$2.5V, i_D increased linearly with v_{DS} at low voltages, signifying operation in the triode region, and will eventually get saturated (flatten out) at higher v_{DS} values. The saturation region exhibited minimal channel-length modulation, as evidenced by the nearly flat curves for i_D versus v_{DS}. This behavior suggests a high effective Early voltage (V_A), which was calculated to quantify the extent of channel-length modulation. We can derive the equation to find V_A using the MOSFET drain current equation in saturation region:

$$I_D = I_{D0}(1 + \lambda V_{DS})$$

where λ is the channel-length modulation parameter, I_D is the actual drain current, and I_{D0} is the ideal drain current without channel length modulation.

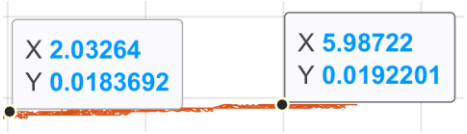

Figure 1.11: Data points of a i_D-v_{DS} plot with V_G=2.5V in saturation region for effective Early voltage calculation

The derived equation is as followed:

$$V_A = \frac{1}{\lambda} = \frac{\Delta V}{\frac{I_2}{I_1} - 1} = \frac{5.98722V - 2.03264V}{\frac{0.0192201A}{0.0183692A} - 1} = 85.4V$$

85.4V falls within the typical range of 10V to 100V for MOSFET devices, where higher values indicate better output resistance. For a general-purpose NMOS transistor like the BS170, this moderate Early voltage value is acceptable and consistent with its intended switching and amplification applications. The corresponding channel length modulation parameter λ = 1/85.4V = 0.0117V^{-1} indicates a reasonable dependence of drain current on drain-source voltage in the saturation region, as evidenced by the moderate slope observed in the i_D-v_{DS} plot.

Finally, the gate voltage was set to 3V by adjusting the potentiometer and the drain voltage to 5V. This required the sawtooth signal source to be replaced by a 5V DC voltage source. The result is shown in *Figure 1.12*. The gate voltage was incremented by approximately 100mV and the result is as shown in *Figure 1.13*.

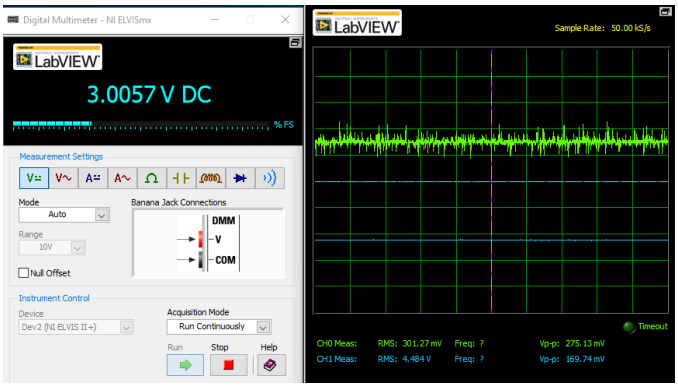

Figure 1.12: Measurement taken at V_G=3V with V_{in}=5V DC

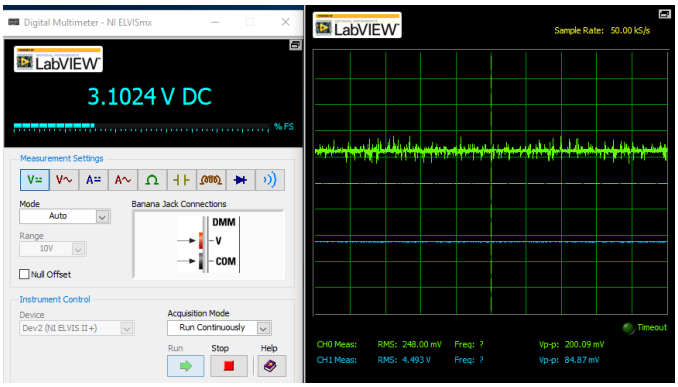

Figure 1.13: Measurement taken at V_G=3.1V with V_{in}=5V DC

Table 1.1: i_D and v_{GS} measurements taken at V_{in}=5V DC

	V_G = 3.0057 V	V_G = 3.1024 V
$V_Y = V_{DS}$	4.484 V	4.493 V
$i_D = \frac{V_Y}{100}$	44.84 mA	44.93 mA

It is now possible to find the transconductance g_m of our device using the following formula:

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}} = \frac{44.93mA - 44.84mA}{3.1024V - 3.0057V} = 0.93mS$$

This value is reasonable for a small-signal NMOS transistor like the BS170 operating at moderate drain currents (~45mA), as typical transconductance values for power MOSFETs range from 0.1 mS to several mS depending on the operating point. The relatively low transconductance indicates that larger gate

voltage changes are needed to effect changes in drain current, which is characteristic of this type of general-purpose NMOS device designed for switching applications.

B. *Part 2: MOSFET Temperature Effets*

In part 2 of the lab, the same curve tracer circuit as part 1 is analyzed. However, the NMOS will be under different temperature conditions to analyze how different MOSFET temperatures affect the output responses. Again, the function generator will be set to generate a sawtooth waveform with peak-to-peak voltage of 10V with an offset of 5V so that V_{in} varies from 0V to 10V.

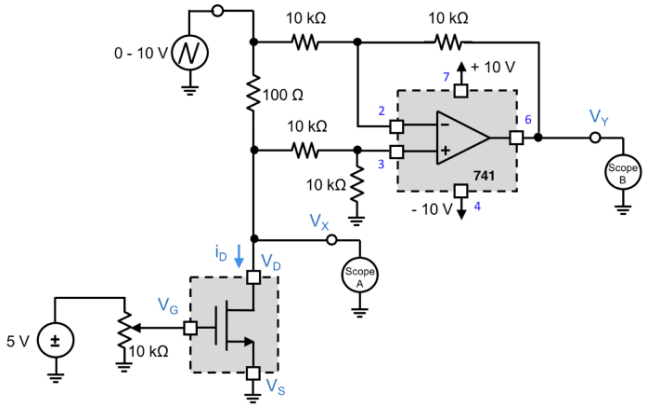

Figure 2.1: Curve tracer circuit for measuring MOSFET i-v characteristics under different temperature conditions

The measurements were first taken at room temperature (27 °C), then at cold (-3 °C) and hot (45 °C) temperatures using a freeze spray and a hot-air blowgun. The temperature of the MOSFET was recorded using a hand-held thermal imager. The i-v plots are shown in the figure below, obtained using MATLAB.

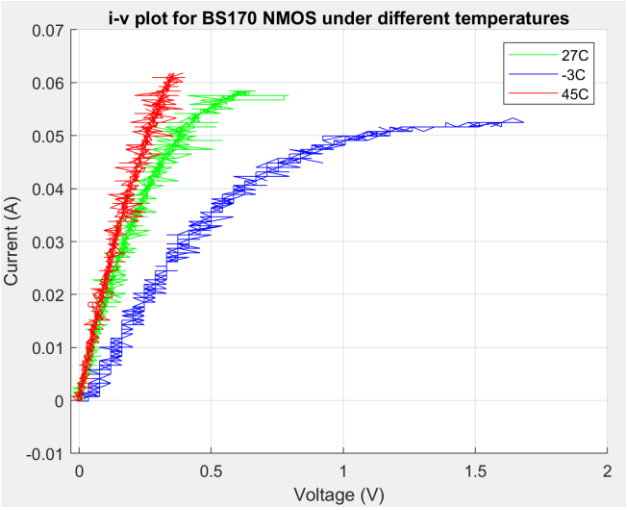

Figure 2.2: i-v plot for BS170 NMOS under different temperatures

The i_D-v_{DS} characteristics of the BS170 NMOS transistor under different temperatures (-3°C, 27°C, and 45°C) show significant variations. At -3°C, the blue curve demonstrates lower drain current for a given voltage compared to the curves at 27°C and 45°C, which exhibit increasing currents, respectively. This behavior is expected, as higher temperatures lead to a decrease in the threshold voltage (V_t) and an increase in thermal carrier generation, resulting in higher drain currents.

The variation in MOSFET conductivity with temperature can be explained by the fact that, at lower temperatures, there are fewer thermally generated charge carriers, resulting in reduced conduction. Conversely, at higher temperatures, an increase in thermally generated charge carriers and a reduction in the threshold voltage (V_t) enhance the MOSFET's conductivity. This increased thermal energy reduces the bandgap energy, allowing electrons to transition more easily, thus boosting current flow through the device. The upward shift in the curves with temperature aligns with the theoretical drain current equation:

$$i_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

where the slight reduction in carrier mobility (μ) at higher temperatures is outweighed by the decrease in V_t. To mitigate the temperature dependence of the MOSFET, temperature compensation circuitry can be employed to adjust the gate voltage dynamically. Additionally, heat sinks or cooling systems can help maintain stable device temperatures, and selecting MOSFETs with built-in temperature compensation can further reduce performance variations. These measures are essential for ensuring consistent MOSFET operation across varying thermal conditions.

C. *Part 3: BJT i_C-v_{CE} Characteristics Using a Curve Tracer*

The following curve tracer circuit was constructed using a 741 op-amp and the 2N2222A npn transistor. A function generator was used to provide a sawtooth waveform ranging from 0V to 10V to the circuit, meaning that the input voltage v_{in} has a peak-to-peak voltage of 10V with an offset voltage of 5V. Furthermore, the wiper of a 10kΩ potentiometer was connected to the base of the transistor. The circuit is as seen in the diagram below.

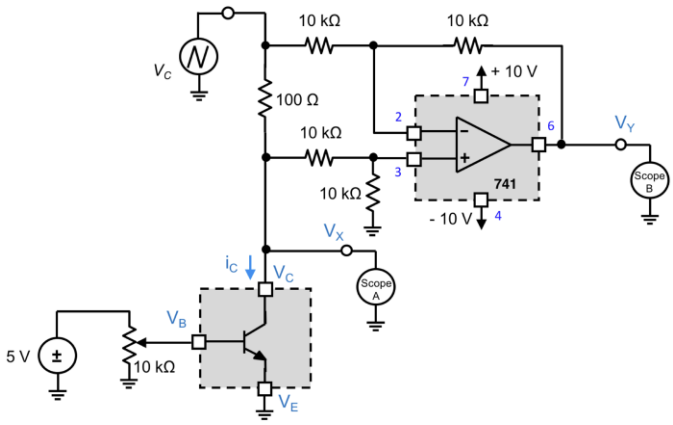

Figure 3.1 Curve tracer circuit for measuring BJT i-v characteristics

In the lab, Channel 0 (CH0) of the oscilloscope corresponds to V_x (Scope A), while Channel 1 (CH1) corresponds to V_Y (Scope B). V_X measures the collector-emitter voltage V_{CE}. Since V_Y is scaled up to be 100 times larger than the actual current (i_C), it must be divided by 100 to obtain the true current value. For example, as shown in *Figure 3.2*, the multimeter measures the base voltage V_B to be approximately 0.035mV, which is effectively 0V. The CH1 reading on the oscilloscope, after being divided by the scaling factor of 100, results in a drain current of $i_C = \frac{7.84\times10^{-3}}{100} \approx 0A$. CH1 also displays a near-flat line on the oscilloscope, which corresponds to what we were expecting. This confirms that with the base voltage V_B set to zero, the collector current i_C is zero while the collector-emitter sweeps from 0 to 10V.

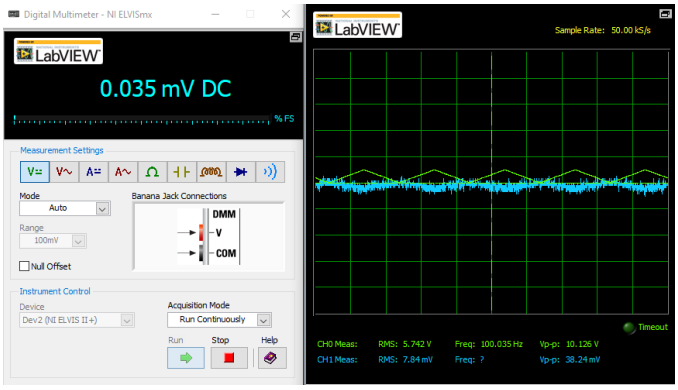

Figure 3.2: Measurement of base voltage (V_B), V_X (V_{CE}), and V_Y

Next, the base voltage was incremented by steps of about 50mV until it reached 750mV by adjusting the screw on the potentiometer in order to calculate the i_C-v_{CE} characteristics (see *Figure 3.3* to *3.17*).

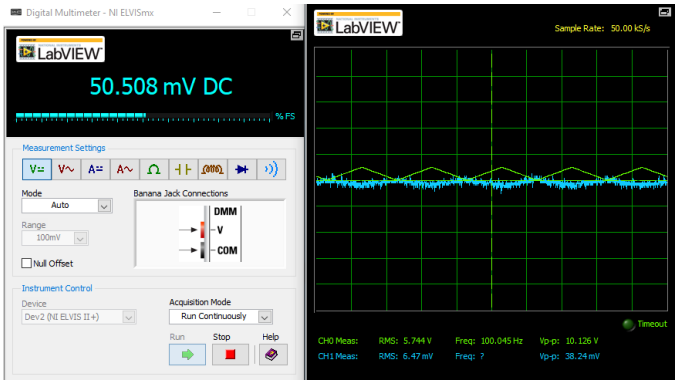

Figure 3.3: Measurement taken at V_B=0.05V

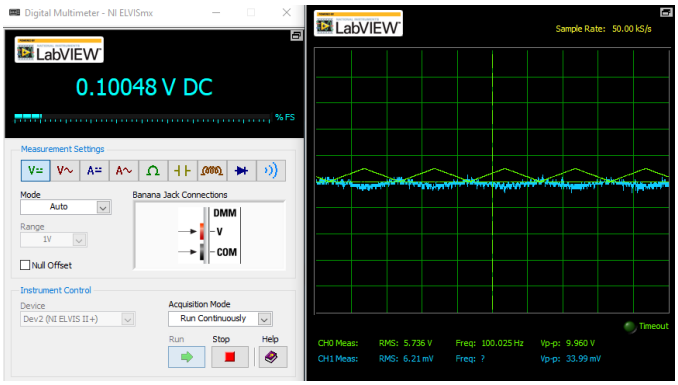

Figure 3.4: Measurement taken at V_B=0.1V

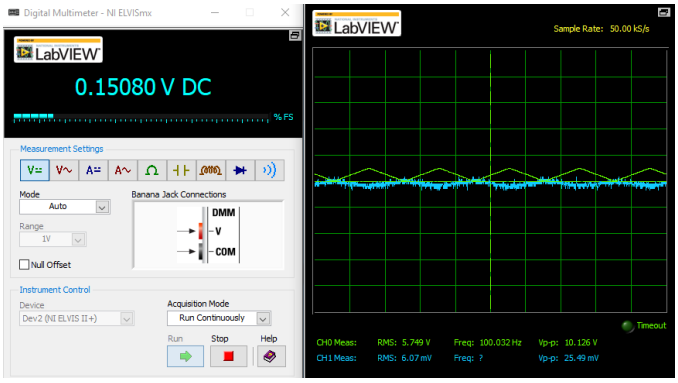

Figure 3.5: Measurement taken at V_B=0.15V

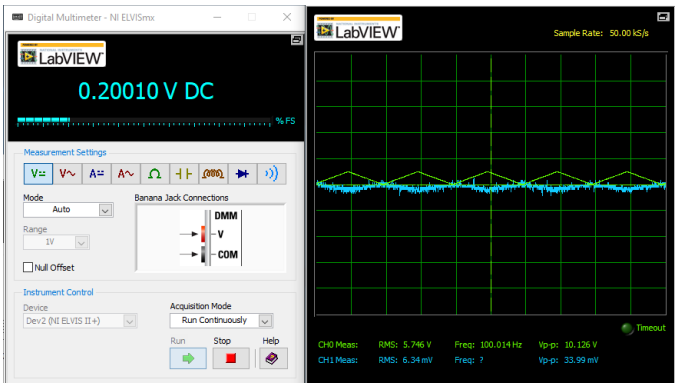

Figure 3.6: Measurement taken at V_B=0.2V

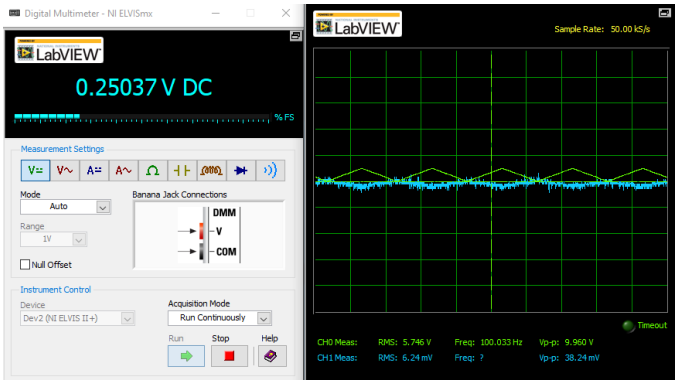

Figure 3.7: Measurement taken at V_B=0.25V

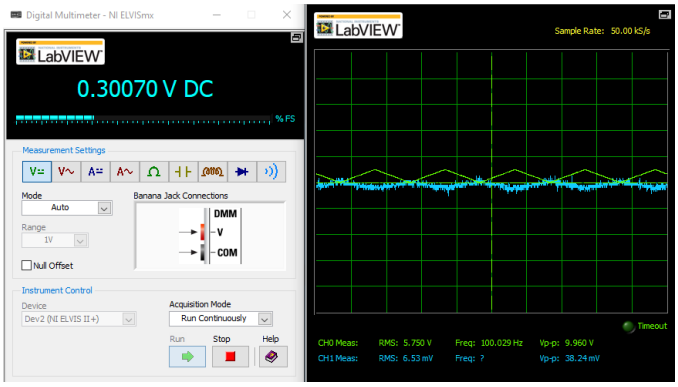

Figure 3.8: Measurement taken at V_B=0.3V

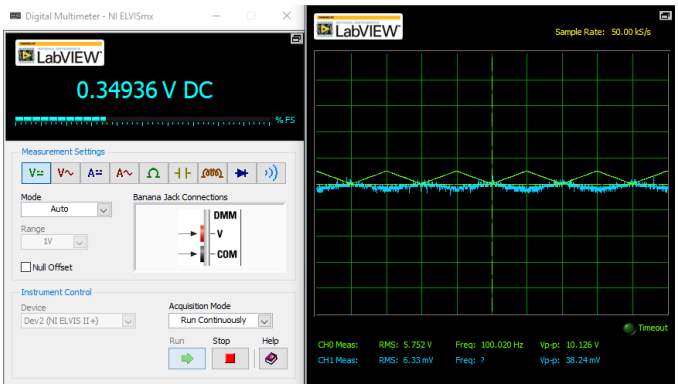

Figure 3.9: Measurement taken at V_B=0.35V

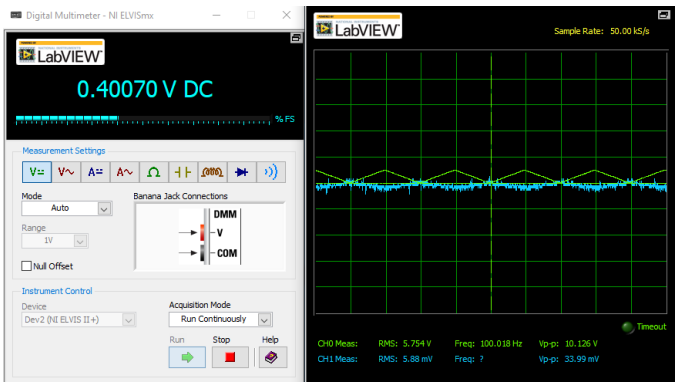

Figure 3.10: Measurement taken at V_B=0.4V

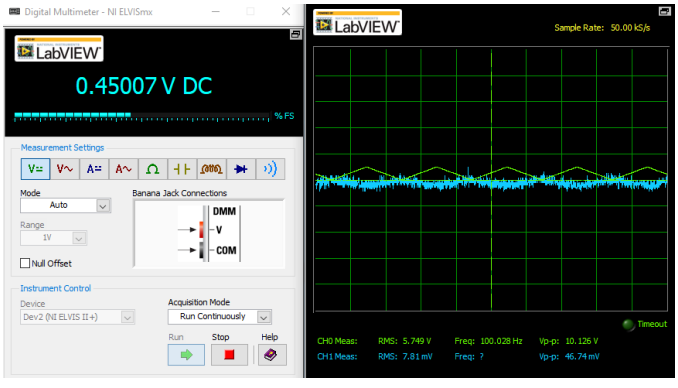

Figure 3.11: Measurement taken at V_B=0.45V

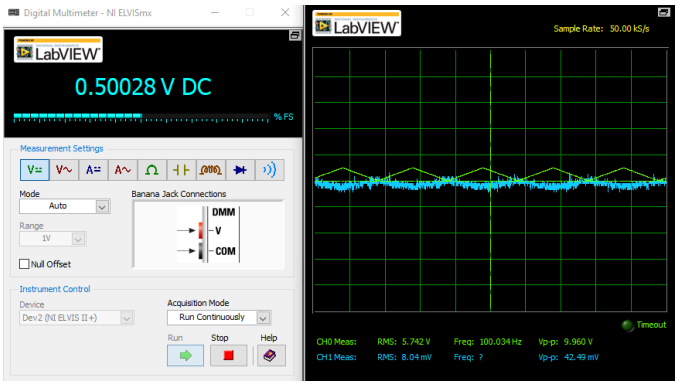

Figure 3.12: Measurement taken at V_B=0.5V

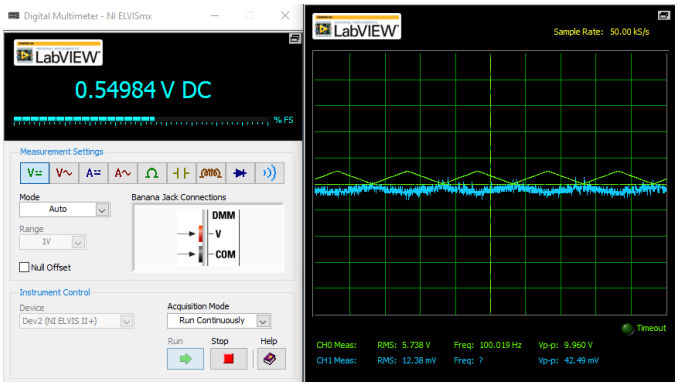

Figure 3.13: Measurement taken at V_B=0.55V

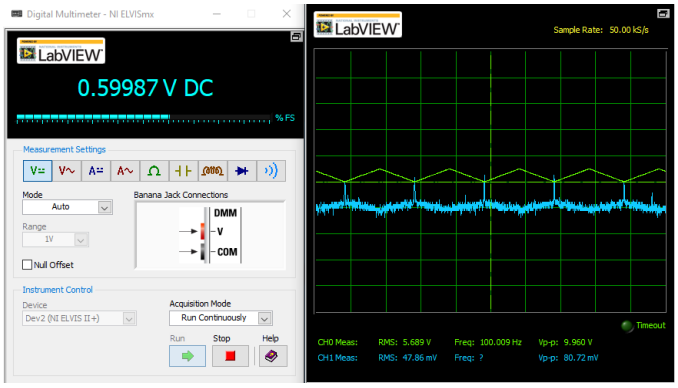

Figure 3.14: Measurement taken at V_B=0.6V

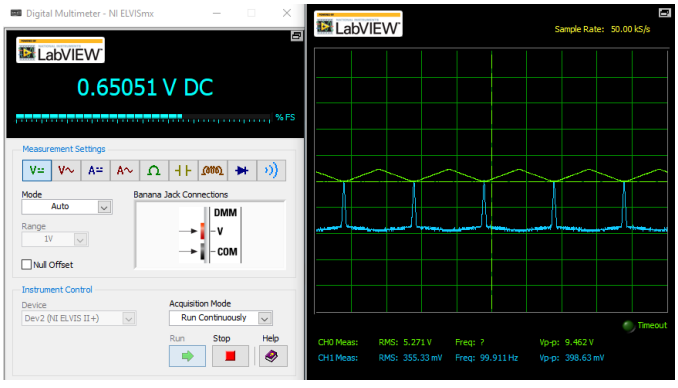

Figure 3.15: Measurement taken at V_B=0.65V

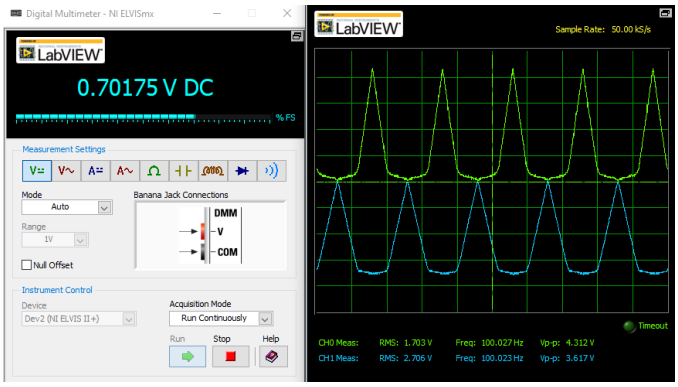

Figure 3.16: Measurement taken at V_B=0.7V

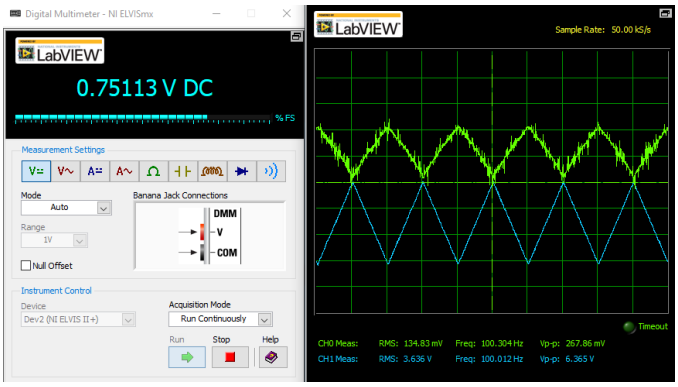

Figure 3.17: Measurement taken at V_B=0.75V

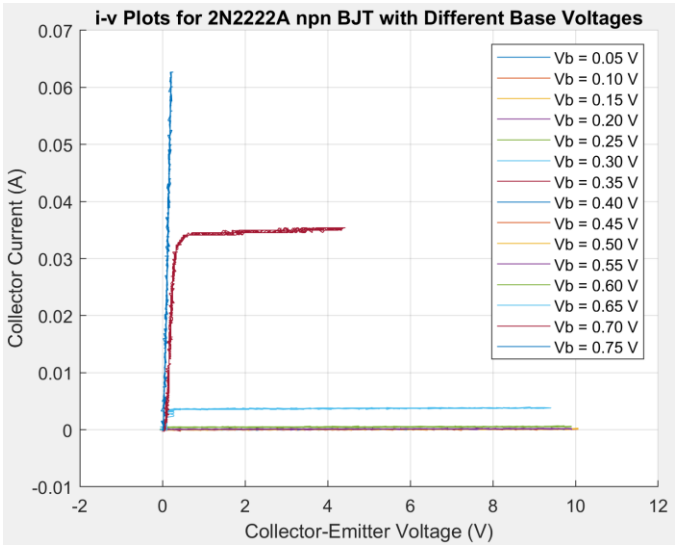

Figure 3.18: i_C-v_{CE} plot generated using Matlab at different base voltages

The i-v characteristics of the 2N2222A npn BJT demonstrate the expected behavior across its three operating regions: cutoff, active, and saturation. In the cutoff region, where $V_B \leq 0.6V$, the collector current (i_C) is negligible for all collector-emitter voltages (V_{CE}), indicating that the transistor is non-conductive.

In the saturation region, at low V_{CE}, i_C increases rapidly with V_{CE}, as both the base-emitter and base-collector junctions are forward-biased.

The active region is characterized by a nearly constant i_C for a fixed base voltage (V_B) once V_{CE} exceeds a certain threshold. Note that the BJT starts conducting current at around 0.65V, which means that the BJT has a turn-on voltage (or base-emitter voltage V_{BE}) of 0.65V. This falls between the typical turn-on voltage region for silicon BJTs which is typically around 0.6-0.7V. In the active region, i_C is primarily governed by V_B, with minimal dependence on V_{CE}, enabling the transistor to function as an amplifier. The slight upward slope in i_C within the active region is attributed to the Early effect, where base-width modulation causes a small increase in i_C with V_{CE}.

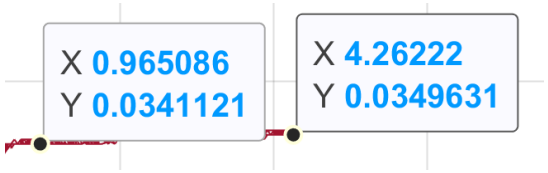

Figure 3.19: Data points of a i_C-v_{CE} plot with V_B=0.7V in active region for effective Early voltage calculation

Similar to the effective Early voltage calculation in part 1 of the lab, the derived equation is as followed:

$$V_A = \frac{1}{\lambda} = \frac{\Delta V}{\frac{I_2}{I_1} - 1} = \frac{4.26222V - 0.965086V}{\frac{0.0349631A}{0.0341121A} - 1} = 132.15V$$

where λ is the channel-length modulation parameter. This is a reasonable value for a BJT, as typical Early voltages for BJTs range from 50V to 150V, with higher values indicating better output resistance in the active region. The high Early voltage of 132V suggests that this transistor has good output resistance characteristics, which is expected for a BJT like 2N2222A npn.

Finally, the base voltage was set to 0.65V by adjusting the potentiometer and the collector voltage to 5V. This required that the sawtooth function generator v_{in} to be replaced by a 5V DC source. The result is shown in *Figure 3.20*. The gate voltage was incremented by approximately 50mV to 0.7V and the result is as shown in *Figure 3.21*.

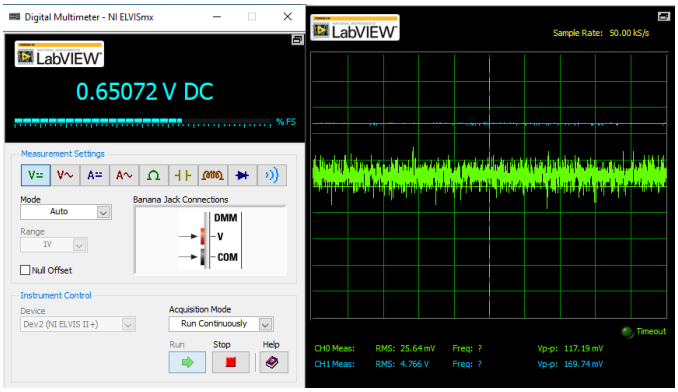

Figure 3.20: Measurement taken at V_B=0.65V with V_{in}=5V DC

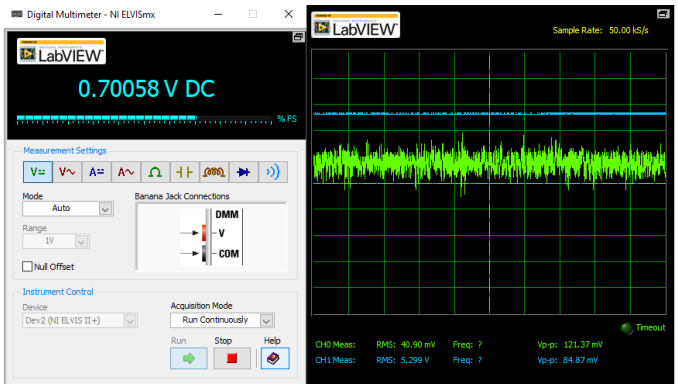

Figure 3.21: Measurement taken at V_B=0.7V with V_{in}=5V DC

Table 3.1: i_C and v_{CE} measurements taken at V_{in}=5V DC

	V_B = 0.65072 V	V_B = 0.70058 V
$V_Y = V_{CE}$	4.766 V	5.299 V
$i_C = \frac{V_Y}{100}$	47.66 mA	52.99 mA

It is now possible to find the transconductance g_m of our device using the following formula:

$$g_m = \frac{\Delta i_c}{\Delta v_{BE}} = \frac{52.99mA - 47.66mA}{0.70058V - 0.65072V} = 22.299mS$$

The calculated transconductance falls within the expected range of 10-100 mS for BJTs operating in their active region, indicating proper device operation. This moderate transconductance value suggests that the transistor provides reasonable current gain and voltage-to-current conversion efficiency, which is typical for a general-purpose BJT like the 2N2222A operating at collector currents in the milliamp range.

D. Part 4: BJT Temperature Effects

In part 4 of the lab, the same curve tracer circuit as part 3 is analyzed. However, the 2N2222A BJT will be under different temperature conditions to analyze how different BJT temperatures affect the output responses. Again, the function generator will be set to generate a sawtooth waveform with peak-to-peak voltage of 10V with an offset of 5V so that V_{in} varies from 0V to 10V. The base voltage was set to be 0.7V using a digital multimeter.

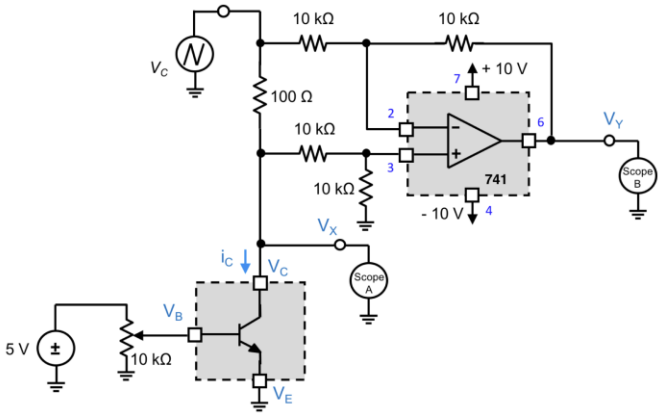

Figure 4.1: Curve tracer circuit for measuring BJT i-v characteristics under different temperature conditions

The measurements were first taken at room temperature (27 °C), then at cold (-3 °C) and hot (40 °C) temperatures using a freeze spray and a hot-air blowgun. The temperature of the BJT was recorded using a hand-held thermal imager. The i-v plots are shown in the figure below, obtained using MATLAB.

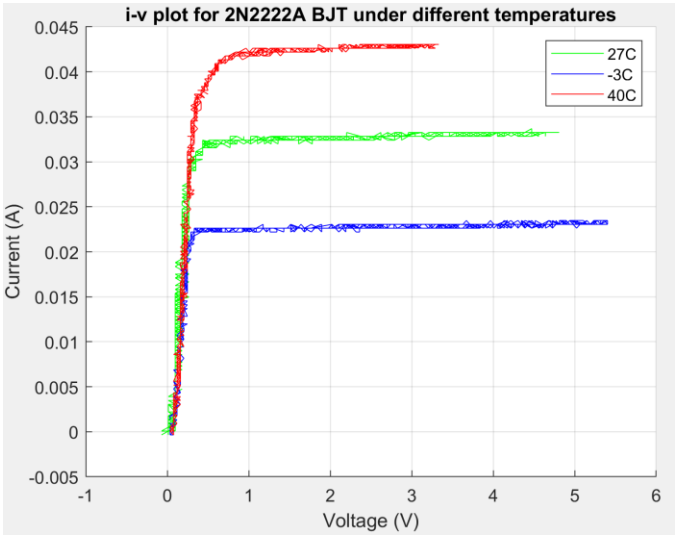

Figure 4.2: i-v plot for 2N2222A BJT under different temperatures

The i_C-v_{CE} characteristics of the 2N2222A BJT show significant variations with temperature. At -3°C, the collector current (i_C) is the lowest (22.5mA) for a given v_{CE}, while at 27°C and 40°C, the collector current increases progressively (32.5mA), with the highest current observed at 40°C (42.5mA). This behavior can be attributed to the thermal dependence of the base-emitter junction. As temperature increases, the base-emitter voltage (v_{BE}) required to maintain a given collector current decreases by approximately 2 mV/°C, leading to higher current conduction.

Additionally, increased thermal generation of minority carriers and exponential growth of the reverse saturation current (I_{CBO} – collector-base leakage current) contribute to the rise in collector current with temperature. I_{CBO} represents the small amount of current that flows from the collector to the base in a bipolar junction transistor (BJT) when the collector-base

junction is reverse-biased. This current arises due to the thermal generation of minority carriers in the depletion region of the collector-base junction. The fact that increased thermal generation of minority carriers and exponential growth of the reverse saturation current contribute to the rise in collector current with temperature is consistent with the theoretical equation:

$$i_C = i_S e^{\frac{V_{BE}}{V_T}}$$

where the saturation current (I_S) increases exponentially with temperature, and the thermal voltage (V_T) also rises. To mitigate these temperature effects, thermal stabilization techniques such as heat sinks or cooling systems can be employed. Furthermore, thermal compensation circuits or components with lower temperature sensitivity can be used to ensure stable BJT performance under varying thermal conditions.

III. Conclusion

This laboratory experiment provided a comprehensive analysis of the DC characteristics of MOSFETs and BJTs. Through various experiments, the i-v relationships were observed under different conditions, including varying gate/base voltages and temperatures. The experiments successfully demonstrated the impact of temperature on the conductivity of both transistors, highlighting their sensitivity to thermal fluctuations.

The MOSFET's behavior was explored through its i_D-v_{DS} characteristics, showcasing saturation when v_{DS} exceeded the overdrive voltage. Similarly, the i_C-v_{CE} characteristics of the BJT illustrated the device's response to incremental changes in base voltage. Additionally, temperature dependence was characterized using cooling and heating methods, confirming theoretical expectations about mobility and recombination rate changes.

Overall, the lab reinforced theoretical concepts through practical implementation, emphasizing the importance of biasing design, thermal considerations, and operating regions in modern transistor applications. Future experiments could further investigate methods to mitigate temperature-induced variations, enhancing the stability of transistor-based circuits.