Design and verification of Three Current Mirror OTA

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1 Design of Biasing Circuit of 250 μA

In this design, the starting point for the Three Current Mirror OTA design is the biasing circuit, guided by the specifications provided in Table 1.

Table 1: Design specifications of biasing circuit cell of 250 μA

Parameter	Value
$\lvert V_{D,sat}\rvert$	100 mV
I_B	250 μA
V_{bnH},$\lvert V_{bpH}\rvert$	≈790 mV
V_{bnL},$\lvert V_{bpL}\rvert$	≈550 mV

The topology to be employed is illustrated in Figure 1. It involves the replication of the current i_B (assumed to originate from an external source) for the generation of bias voltages for each cascode stage. The sizing methodology carried out is as follows, proposing an L = 180nm:

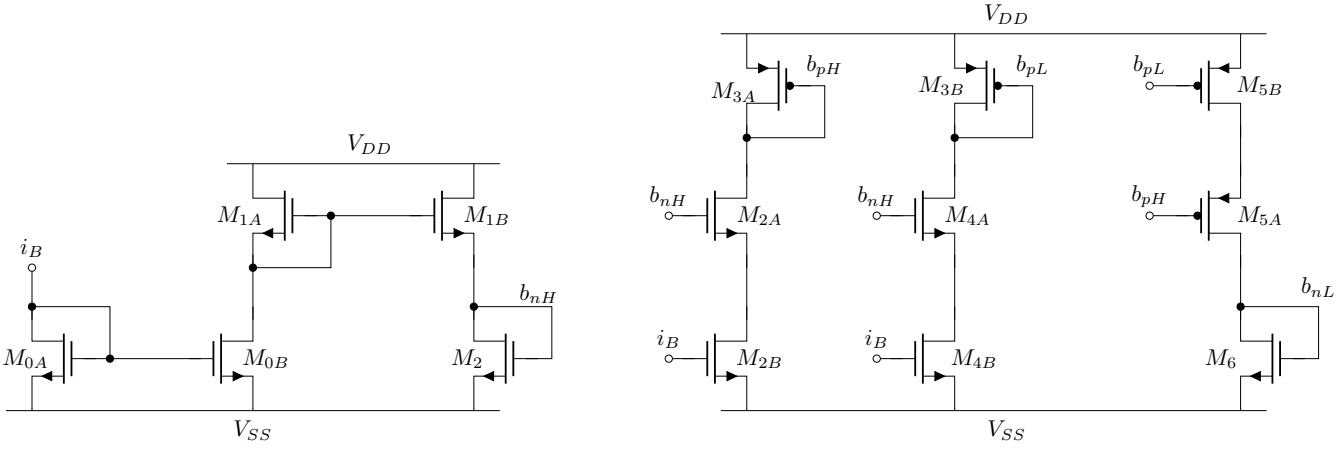

Figure 1: Schematic of polarization circuit of 250 μA

- Transistors M_{0A}, M_{0B}, M_{1A}, and M_{1B}: The selection of W for transistor M_{0A} was carried out by sweeping until the defined $V_{D,sat}$ was achieved. Ideally, transistor M_{0B} would have an exact copy of the current i_B. However, due to short-channel effects (λ) and mismatch, the current is not the same. In order to eliminate this effect, the width (W) of transistor M_{0B}

was modified until achieving a copy of 250 μA. Similarly, this procedure was applied to the current mirror copy of the pMOS transistors (M_{1A} and M_{1B}).

- Transistor M_2: The function of this transistor is to generate the bias voltage V_{bnH} as defined in Table 1. To achieve this, the width (W) of M_2 was modified.

- Transistors M_{2A} and M_{2B}: They were sized with the objective of conducting a current i_D = 250 μA at 20% higher than the previously defined $|V_{D,sat}|$. The widths (W) of the transistors are the same in this cascode stage.

- Transistors M_{3A} and M_{3B}: The value of W for these transistors was designed with the objective of obtaining the bias voltages V_{bnL} and $|V_{bpL}|$ at V_{DS}.

- Transistors M_{5A} and M_{5B}: They are sized with the objective of obtaining a pMOS mirror at 250 μA. At this stage, the sizing was done in such a way that the copy is as faithful as possible to 250μA, thus ensuring that M_6 copies the same current and generates a V_{GS} equal to that generated by the source i_B.

The procedure results in the dimensions shown in Table 2, where the operating point of each transistor is summarized:

Table 2: Design specifications of biasing circuit cell of 250 μA

Transitor	W_F [m]	L [nm]	NF	g_m [S]	i_{ds} [A]	$\|v_{gs}\|$ [V]
M_{0A}	3.75μ	180	8	3.66 m	250 μ	543 m
M_{0B}	2.58μ	180	8	3.33 m	250.8 μ	543 m
M_{1A},M_{1B}	12.95μ	180	8	250.8 μ	4.64m	-544.3 m
M_2	350n	180	8	1.206 m	302.6 μ	787.5 m
M_{2A}, M_{2B}	4.7μ	180	8	4.013 m	254.4 μ	550.4 m
M_{3A}	1.4μ	180	8	1.436m	254.4 μ	-790.4 m
M_{3B}	12.95μ	180	8	4m	256.5 μ	-545.7 m
M_{4A}, M_{4B}	4.8μ	180	8	4.063 m	256.6 μ	542.8 m
M_{5A}, M_{5B}	14.9μ	180	8	4.158 m	250.8 μ	579.2 m
M_6	3.75μ	180	8	3.673 m	250.8 μ	543.2 m

With the aim of verifying the designed circuit, a testbench was conducted for the biasing circuit by parametrizing the dimensions of the nMOS and pMOS cascode mirrors. The resulting plots are shown in Figure 2.

Figure 2: DC Transfer Function of nMOS (blue) and pMOS cascodes (green)

This allows for a minimal offset level in the cascodes of the output stages because there is a balance between both transfer functions for both types of mirrors.

2 Design of nMOS 3-Current Mirror OTA

Considering the design of the biasing stage, it is possible to parameterize the resulting cascode mirrors and implement the 3-Current Mirror OTA, the structure of which is illustrated in Figure 3.

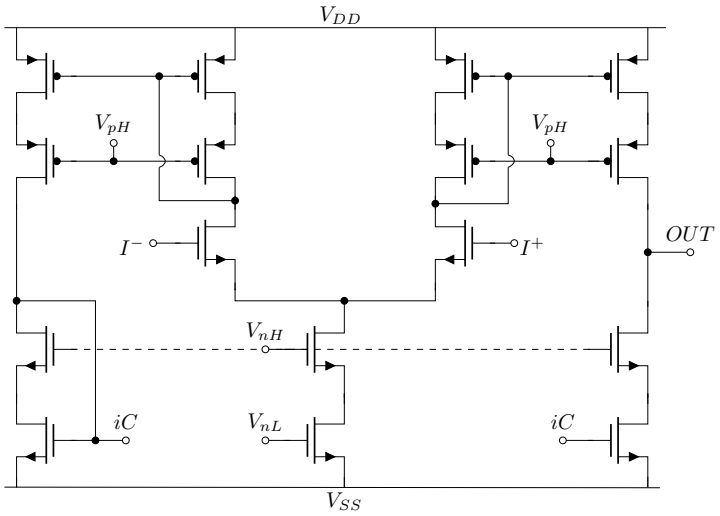

Figure 3: Schematic of 3-Current Mirror OTA with 250 μA bias

Table 3 summarizes the dimensions considered for the designed OTA.

Table 3: Design specifications of biasing circuit cell of 250 μA

Transitor	W_F [m]	L [nm]	NF
M_{B0}, M_{B1}	9.6μ	180	4
M_0, M_1	42.3μ	180	2
M_{P1}, M_{P2}	59.6μ	180	2
M_{N1}, M_{N2}	19.2μ	180	2

In this exercise, the nMOS current mirror has the same dimensions as the cascode composed of transistors M_{4A} and M_{4B}, defining the number of fingers (NF) of the biasing stage as NF = 4 and adjusting the W_F so that the total width is the same across the transistors. Similarly, for the cascodes composed of pMOS transistors M_{5A} and M_{5B} from the polarization circuit of 250 μA, initially, a width (W) approximately 4 times that of the nMOS transistor's W_F was proposed for the differential pair. This allowed achieving a closed-loop gain of 52.4 dB.
From the closed-loop analysis to ensure system stability, the measurements shown in Figure 4 were obtained.

Table 4: Closed Loop Simulations Results

Parameter	Value
Gain	52.4 dB
GBP	313.9 MHz
Phase Margin	52.47°

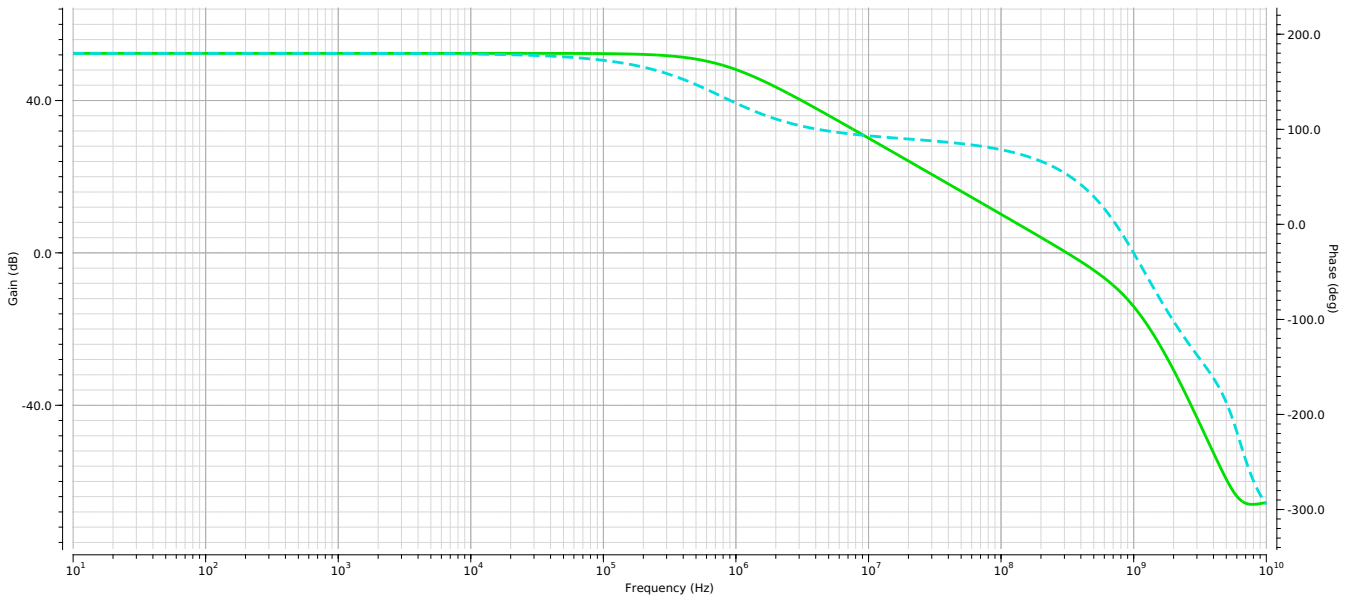

Figure 4: Closed Loop Gain (green) and Phase (blue dashed) frequency responses

From the designs conducted previously, an improvement in CMRR was noted due to the implementation of the cascode mirror in the biasing stage. Thus, the virtual ground node generated at the input differential pair is optimized. By definition, CMRR is the ratio of the differential mode gain (A_{DM}) to the common mode gain (A_{CM}). Figure 5 illustrates the frequency response of the aforementioned gains as well as CMRR.

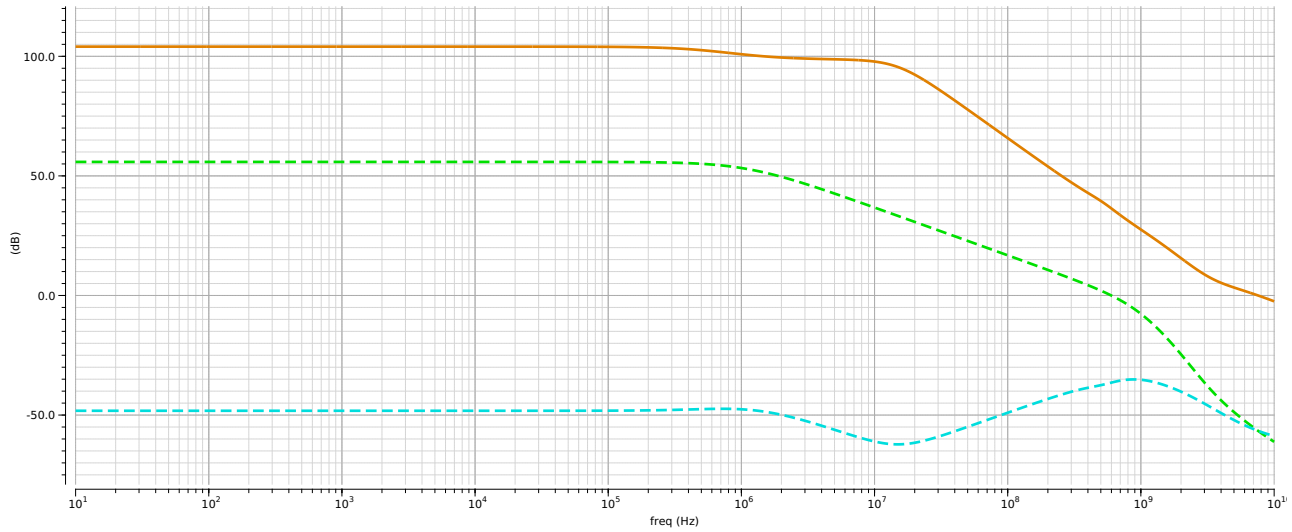

Figure 5: A_{DM} (green dashed), A_{CM} (blue dashed) and CMRR (orange) frequency responses

The response of the offset referred to the input measurement is shown in Figure 6, with $V_{off} = 9.45$ mV for frequencies below 1 MHz.

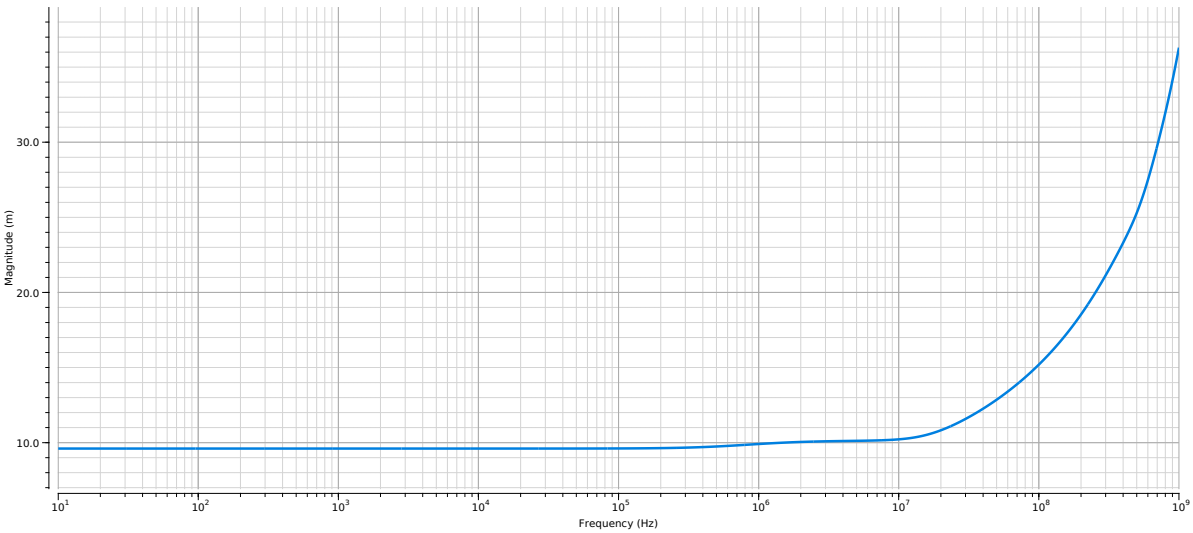

Figure 6: A_{DM} (green dashed), A_{CM} (blue dashed) and CMRR (orange) frequency responses

The noise analysis was conducted on the designed OTA, with the noise response referred to the input considered as the average power of V_n in 1 Hz. In order to account for the contribution of flicker noise (also known as $1/f$ noise), the frequency sweep considered ranges from 1 mHz to 10 GHz. Thus, the integration to obtain the average power is obtained as the integral of the response shown in Figure 7.

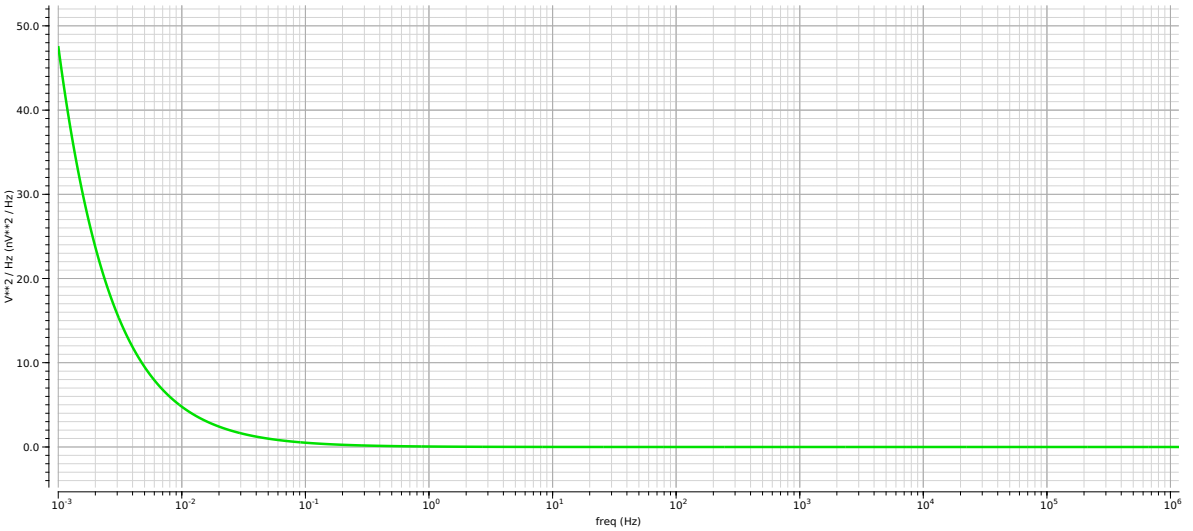

Figure 7: Input referred noise frequency response

The total calculated PSD is $V_n^2 = 959.1$ pV, which means that signals with amplitudes smaller than this value are very difficult to detect because they get lost within it. **Therefore, it can be concluded that to ensure the integrity of the input signal throughout the amplification process, it should be at least 10 times greater than the PSD calculated (≈9.591 nV).**

The Cadence simulation tool allows a summary of the noise contribution by transistors to be obtained, as depicted in the following figure. The summary emphasizes pMOS transistors composing current mirrors, particularly those directly connecting the Source terminal to V_{DD}, as the major contributors to input-referred noise.

Device	Param	Noise Contribution	% Of Total
I18.M67	id	3.12911e-09	14.65
I18.M63	id	2.91872e-09	13.67
I18.M69	id	2.72104e-09	12.74

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 2.13548e-08
Total Input Referred Noise = 3.36019e-08
The above noise summary info is for noise data

Figure 8: Noise summary results

Finally, the responses of $PSRR^+$ and $PSRR^-$ (due to variations in V_{DD} and V_{SS} respectively) are shown in Figure 9.

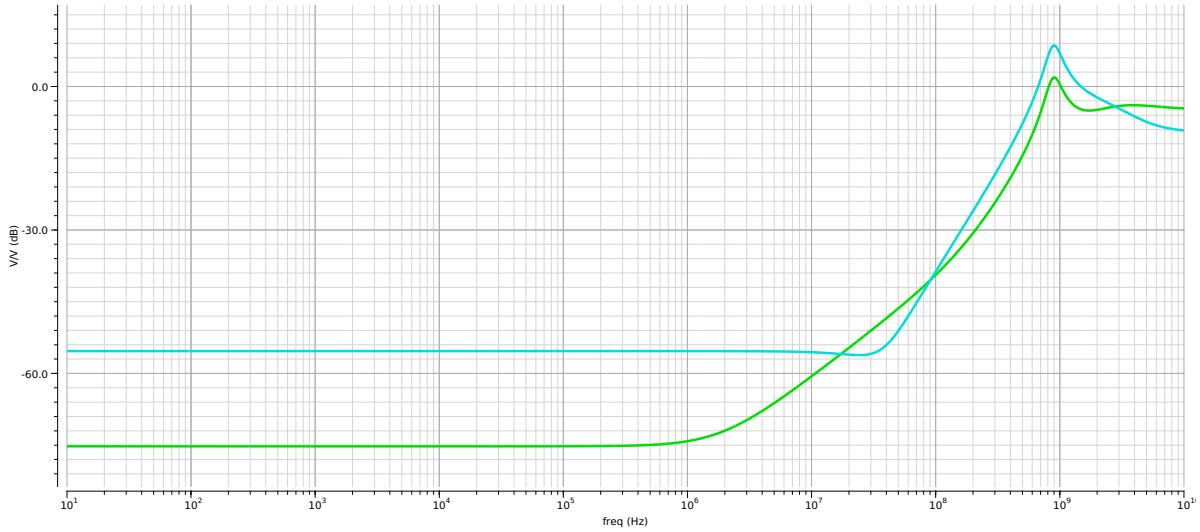

Figure 9: $PSRR^+$ (green) and $PSRR^-$ (blue dashed) responses

2.1 Modification

As a suggestion (and design experimentation), the decision was made to modify the length (L) of all transistors in the OTA (while keeping the same widths as shown in Table 3) to L = 360 nm. This resulted in an increase in AC gain of 13 dB, yielding a closed-loop gain of 65 dB at the cost of a significantly reduced phase margin (35°). The response can be observed in Figure 10.

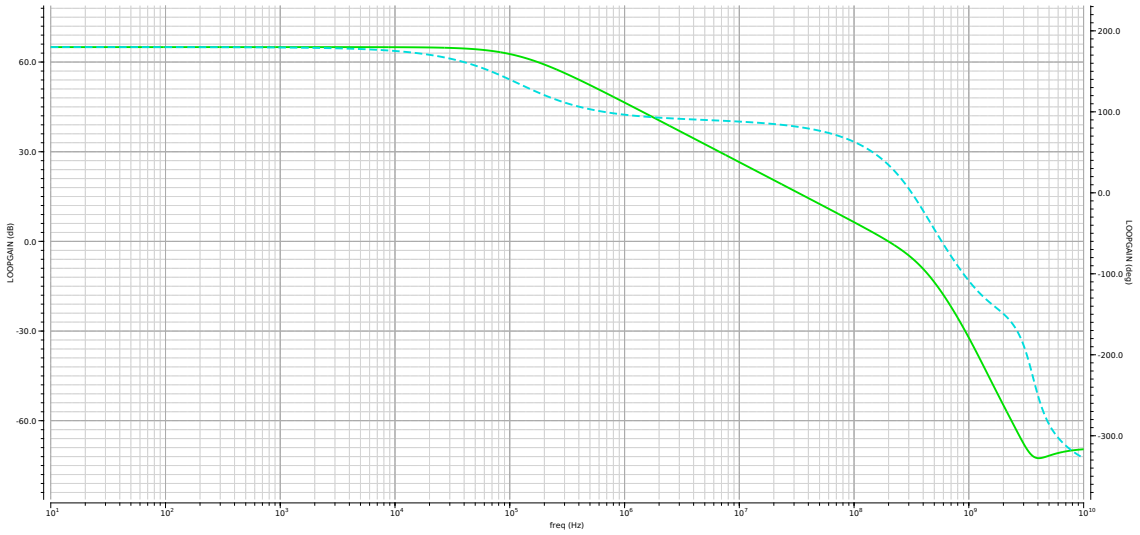

Figure 10: Closed Loop Gain (green) and Phase (blue dashed) frequency responses

This design could be considered; however, due to its reduced phase margin, its implementation could lead to instability in the system if used in a closed-loop configuration.