Homework VIII.
Statistical Design and Corner Design

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For the development of this project, the logical path of 6 inverters designed symmetrically with an N_{fin}=2 is considered, whose delay target should be 80 ps. Each inverter has a FO (fanout) of 8. The positions of the gates along the chip are shown in Fig. 1.

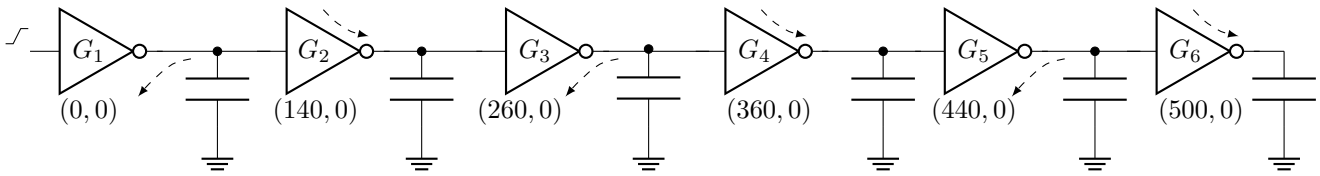
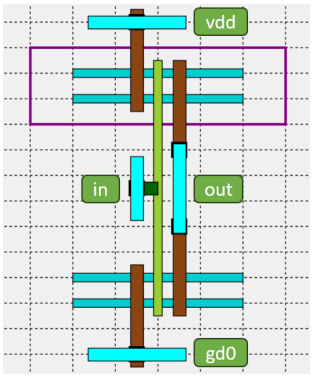


Figure 1: Inverter Chain

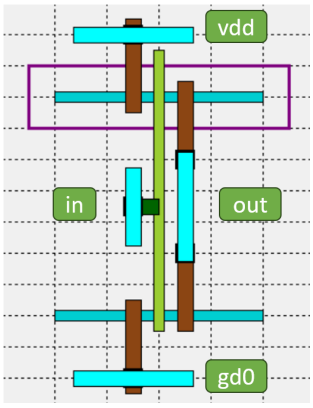
The technology used for this design is Intel's 14-nm process, employing a predictive model for multi-gate transistors (PTM-MG).

1 Tipical Response

With the aim of meeting the 80 ps target for the delay of the logical path, two subcircuits are defined. One is associated with the 1x inverter, allowing the definition of FO = 8. Another subcircuit will define the load fanout, and a subcircuit is associated with the gates of the logical path. Figures 2b and 2a show the layouts associated with a unitary gate for each case.



(a) Inverter Layout with 2 Fin and 1 Finger



(b) Inverter Layout with 1 Fin and 1 Finger

Figure 2: Layout proposal for each inverter

The Raphael RC3 tool is used to extract the parasitic capacitances from each layout. In this way, the parasitic effect of each design is individually considered in each subcircuit. The description of the subcircuit associated with the inverter in Figure 2b is shown in the box below, the associated terminals are as described in the figure: **in, out, vdd, gd0**.

```
.subckt inv1X in out vdd gd0

xp_a1 out in vdd vdd finfet_pmos numfin=1
xn_a1 out in gd0 gd0 finfet_nmos numfin=1

C_0_1 out gd0 1.713094e-17
C_0_2 out vdd 1.481918e-17
C_0_3 out in 1.689425e-16
C_1_2 gd0 vdd 1.676389e-18
C_1_3 gd0 in 4.723737e-17
C_2_3 vdd in 6.320916e-17

.ends inv1X
```

The code described above allows defining a subcircuit associated with the Fan Out of each output. This way, it is possible to make variations independently of the load. Additionally, it allows modifying (if necessary) the number of load capacitance in terms of Fan Out (FO).

```
.subckt FO inA vddA gd0A

Xfo1 inA outA1 vdda 0 inv1x
cl1 outA1 gd0A 1f
Xfo2 inA outA2 vdda 0 inv1x
cl2 outA2 gd0A 1f
Xfo3 inA outA3 vdda 0 inv1x
cl3 outA3 gd0A 1f
Xfo4 inA outA4 vdda 0 inv1x
cl4 outA4 gd0A 1f
Xfo5 inA outA5 vdda 0 inv1x
cl5 outA5 gd0A 1f
Xfo6 inA outA6 vdda 0 inv1x
cl6 outA6 gd0A 1f
Xfo7 inA outA7 vdda 0 inv1x
cl7 outA7 gd0A 1f
Xfo8 inA outA8 vdda 0 inv1x
cl8 outA8 gd0A 1f

.ends FO
```

Finally, for the definition of the subcircuit associated with the inverters, the capacitances extracted from the layout in Figure 2a were used. This allows instantiating an inverter that will be repeated along the entire logical path to be analyzed.

```
.subckt inv in out vdd gd0

xp_b1 out in vdd vdd finfet_pmos numfin=2
xn_b1 out in gd0 gd0 finfet_nmos numfin=2

C_0_1 out in 2.286025e-16
C_0_2 out vdd 3.044704e-17
C_0_3 out gd0 3.096189e-17
C_0_4 out gd0 9.918963e-17
C_0_5 out vdd 5.027649e-17
C_1_2 in vdd 1.036297e-16
C_1_3 in gd0 1.036487e-16
C_1_4 in gd0 7.461482e-17
C_1_5 in vdd 3.300460e-17
C_2_3 vdd gd0 1.998977e-18
C_2_4 vdd gd0 4.749832e-17
C_2_5 vdd vdd 5.047028e-17
C_3_4 gd0 gd0 9.748517e-17
C_3_5 gd0 vdd 1.713151e-19
C_4_5 gd0 vdd 1.144488e-16

.ends inv
```

The description of the logic path in the SPICE code is shown below. The previously used subcircuits make the code more understandable and easier to handle.

```
**** DESCRIPTION OF THE LOGIC PATH *****

Xinv1 in1 out1 vdda 0 inv
xfo1 out1 vdda 0 FO
Xinv2 out1 out2 vdda 0 inv
xfo2 out2 vdda 0 FO
Xinv3 out2 out3 vdda 0 inv
xfo3 out3 vdda 0 FO
Xinv4 out3 out4 vdda 0 inv
xfo4 out4 vdda 0 FO
Xinv5 out4 out5 vdda 0 inv
xfo5 out5 vdda 0 FO
Xinv6 out5 out6 vdda 0 inv
xfo6 out6 vdda 0 FO

vdd vdda 0 dc 0.8
vva in1 0 dc 0.8 pulse(0.8 0 5p 1p 1p 49p 100p)
```

The following Table 1 summarizes the results using nominal values and without considering variations in either process or correlated variations, this simulation allows us to determine that the optimal number of Fins that meets the propagation time target is 2.

Table 1: Gate delay for the logic path

Gate	t_{pHL} [ps]	t_{pLH} [ps]
G_1	7.49	8.78
G_2	14.1	14.4
G_3	13.8	15.2
G_4	14.9	15.2
G_5	13.8	15.5
G_6	12.9	13.7
Path	**82.4**	**79.2**

2 Design using SS Corner

With the aim of identifying the effects of H_{fin}, T_{fin}, and L_g variations, the sensitivities were characterized at the gate level and along the logical path. This helps identify the variation parameters to define in the future the SS simulation corner (indicating the worst-case scenario for each parameter variation), the variations considered are in accordance with Table 2.

Table 2: Parameters Values of Intel Technology

Parameter	Value [nm]	Parameter	Value [nm]	Parameter	Value [nm]
H_g	76	H_{fin}	42	H_{CB}	35
T_{ox}	1.1	H_{rsd}	51	H_{STI}	80
T_{fin}	8	H_{epi}	9	H_{V0}	45
W_{rsd}	26	H_{TS}	25	H_{M1}	45
W_{TS}	34	H_{CA}	35		

The results of the delay sensitivities at the gate are summarized in Tables 3 and 4. In this way, the analysis of delay times for changes from H$\longrightarrow$L and L$\longrightarrow$H is conducted.

Table 3: Gate delay sensitivities for the logic path at H$\longrightarrow$L input

Gate	$S_{D,Tfin}$ [s/m]	$S_{D,Hfin}$ [s/m]	S_{D,L_g} [s/m]
G_1	-0.625e-4	-0.25e-4	0.5e-4
G_2	-0.625e-4	-0.25e-4	0.5e-4
G_3	-0.25e-4	-0.1786e-4	0.5714e-4
G_4	-0.5e-4	-0.25e-4	0.5e-4
G_5	-0.5e-4	-0.2857e-4	0.5714e-4
G_6	-0.25e-4	-0.3571e-4	0.25e-4

Table 4: Gate delay sensitivities for the logic path at L⟶H input

Gate	$S_{D,Tfin}$ [s/m]	$S_{D,Hfin}$ [s/m]	S_{D,L_g} [s/m]
G_1	-0.25e-4	-0.25e-4	0.4286E-4
G_2	-0.375e-4	-0.25e-4	0.4286e-4
G_3	-0.125e-4	-0.1786e-4	0.2857e-4
G_4	-0.625e-4	-0.2857e-4	0.4286e-4
G_5	-0.25e-4	-0.1429e-4	0.2857e-4
G_6	-0.125e-4	-0.25e-4	0.2914e-4

According to Figure 7 in Appendix A, the sensitivities of the logical path are shown, where it can be noted that there is a negative slope for variations σ of H_{fin} and T_{fin}. This allows us to identify which parameters are considered the worst case. On the other hand, the trend of the sensitivity of the logical path is positive for variations in L_g. Thus, the parameters for the SS design corner are defined in Table 5.

Table 5: Parameters defined for the SS corner.

Parameter	3σ Variation
$d_x\phi_g$	120 mV
d_xT_{fin}	-2.4 nm
d_xL_g	3.5 nm
d_xH_{fin}	-4.2 nm

The simulation results with the SS corner are summarized in Table 6. These simulations are under the same design conditions in the inverters ($N_{fin} = 2$) and the same parasitic capacitances.

Table 6: SS Corner gate delay for the logic path

Gate	t_{pHL} [ps]	t_{pLH} [ps]
G_1	12.3	10.95
G_2	26.2	22.4
G_3	25.1	24.7
G_4	27.6	25.95
G_5	23.6	23.5
G_6	125	104
Path	**215**	**200**

With the aim of meeting the delay target in the logical path, the inverter was increased from $N_{fin} = 2$ to $N_{fin} = 4$, the results of the obtained measurements are summarized in Table 7. For this optimization, the layout was performed (using the Sketch tool), and the associated parasitic capacitances were extracted using Raphael RC3 tool. This ensures that the overall response is as realistic as possible according to the proposed design.

Table 7: SS Corner (Optimized) gate delay for the logic path

Gate	t_{pHL} [ps]	t_{pLH} [ps]
G_1	6.74	8.08
G_2	12.69	13.25
G_3	12.42	13.98
G_4	13.41	13.45
G_5	12.42	14.26
G_6	11.61	12.60
Path	**74.16**	**72.86**

3 Statistical Design

For the statistical design proposal, the variations shown in Table 8 were considered.

Table 8: Process Parameter Variation

Parameter	WID_r (3σ)	D2D,WID_c (3σ)
ϕ_M	90 mV	-
T_{fin}	0.35 nm	0.8 nm
H_{fin}	-	4.2 nm
L_g	0.6 nm	1.4 nm

From the positions of each inverter in Figure 1, the distance matrix from expression (1) is obtained.

$$d_{G_i,G_j} = \begin{bmatrix} 0 & 140 & 260 & 360 & 440 & 500 \\ 140 & 0 & 120 & 220 & 300 & 360 \\ 260 & 120 & 0 & 100 & 180 & 240 \\ 360 & 220 & 100 & 0 & 80 & 140 \\ 440 & 300 & 180 & 80 & 0 & 60 \\ 500 & 360 & 240 & 140 & 60 & 0 \end{bmatrix} \tag{1}$$

The contribution of inter-die and intra-die variations present is assumed to be 20 % (i.e. $K_{D2D} = 0.2$), correlated inter-die variations constitute 80 % of the total at $K_{WID} = 0.8$. The die width (W_{chip}) in this case is 400 μm and is used to compute CD_{WID} ($CD_{WID} = W_{chip}/2$) resulting in 200 μm, the resulting correlation matrix is as shown in expression (2).

$$\rho_{G_i,G_j} = \begin{bmatrix} 1 & 0.5972 & 0.4180 & 0.3322 & 0.2886 & 0.2656 \\ 0.5972 & 1 & 0.6390 & 0.4662 & 0.3785 & 0.3322 \\ 0.4180 & 0.6390 & 1 & 0.6852 & 0.5252 & 0.4409 \\ 0.3322 & 0.4662 & 0.6852 & 1 & 0.7362 & 0.5972 \\ 0.2886 & 0.3785 & 0.5252 & 0.7362 & 1 & 0.7926 \\ 0.2656 & 0.3322 & 0.4409 & 0.5972 & 0.7926 & 1 \end{bmatrix} \tag{2}$$

Applying the Cholesky algorithm to the correlation matrix resulted in the new matrix obtained in expression (3).

$$Chol = \begin{bmatrix} 1 & 0.5972 & 0.4180 & 0.3322 & 0.2886 & 0.2656 \\ 0 & 0.8020 & 0.4854 & 0.3339 & 0.2569 & 0.2164 \\ 0 & 0 & 0.7678 & 0.5003 & 0.3644 & 0.2928 \\ 0 & 0 & 0 & 0.7264 & 0.5123 & 0.3994 \\ 0 & 0 & 0 & 0 & 0.6747 & 0.5171 \\ 0 & 0 & 0 & 0 & 0 & 0.6081 \end{bmatrix} \tag{3}$$

The above is added to the SPICE code as shown in the following text box. This allows generating spatial correlation for the six inverters along the entire chip.

```
**** CORRELATED VARIABLES GENERATION ******

.param uncorrelated_Hfin = agauss(0, '42n*0.2', 3)
.param Z1H = uncorrelated_Hfin
.param Z2H = uncorrelated_Hfin
.param Z3H = uncorrelated_Hfin
.param Z4H = uncorrelated_Hfin
.param Z5H = uncorrelated_Hfin
.param Z6H = uncorrelated_Hfin
.param Zc1H = 'Z1H + 0.5972*Z2H + 0.418*Z3H + 0.3322*Z4H + 0.2886*Z5H + 0.2656*Z6H'
.param Zc2H = '0.8020*Z2H + 0.4854*Z3H + 0.3339*Z4H + 0.2569*Z5H + 0.2164*Z6H'
.param Zc3H = '0.7678*Z3H + 0.5003*Z4H + 0.3644*Z5H + 0.2928*Z6H'
.param Zc4H = '0.7264*Z4H + 0.5123*Z5H + 0.3994*Z6H'
.param Zc5H = '0.6747*Z5H + 0.5171*Z6H'
.param Zc6H = '0.6081*Z6H'

.param uncorrelated_Tfin = agauss(0, '8n*0.2', 3)
.param Z1T = uncorrelated_Tfin
.param Z2T = uncorrelated_Tfin
.param Z3T = uncorrelated_Tfin
.param Z4T = uncorrelated_Tfin
.param Z5T = uncorrelated_Tfin
.param Z6T = uncorrelated_Tfin
.param Zc1T = 'Z1T + 0.5972*Z2T + 0.418*Z3T + 0.3322*Z4T + 0.2886*Z5T + 0.2656*Z6T'
.param Zc2T = '0.8020*Z2T + 0.4854*Z3T + 0.3339*Z4T + 0.2569*Z5T + 0.2164*Z6T'
.param Zc3T = '0.7678*Z3T + 0.5003*Z4T + 0.3644*Z5T + 0.2928*Z6T'
.param Zc4T = '0.7264*Z4T + 0.5123*Z5T + 0.3994*Z6T'
.param Zc5T = '0.6747*Z5T + 0.5171*Z6T'
.param Zc6T = '0.6081*Z6T'

.param uncorrelated_Lg = agauss(0, '14n*0.2', 3)
.param Z1Lg = uncorrelated_Lg
.param Z2Lg = uncorrelated_Lg
.param Z3Lg = uncorrelated_Lg
.param Z4Lg = uncorrelated_Lg
.param Z5Lg = uncorrelated_Lg
.param Z6Lg = uncorrelated_Lg
.param Zc1Lg = 'Z1Lg + 0.5972*Z2Lg + 0.418*Z3Lg + 0.3322*Z4Lg + 0.2886*Z5Lg +
0.2656*Z6Lg'
.param Zc2Lg = '0.8020*Z2Lg + 0.4854*Z3Lg + 0.3339*Z4Lg + 0.2569*Z5Lg + 0.2164*Z6Lg'
.param Zc3Lg = '0.7678*Z3Lg + 0.5003*Z4Lg + 0.3644*Z5Lg + 0.2928*Z6Lg'
.param Zc4Lg = '0.7264*Z4Lg + 0.5123*Z5Lg + 0.3994*Z6Lg'
.param Zc5Lg = '0.6747*Z5Lg + 0.5171*Z6Lg'
.param Zc6Lg = '0.6081*Z6Lg'
```

Figures 3 and 4 show the responses of the Monte Carlo analysis performed under the variations from Table 8, as well as spatial variations with the coefficients of the Cholesky matrix shown in expression (3).

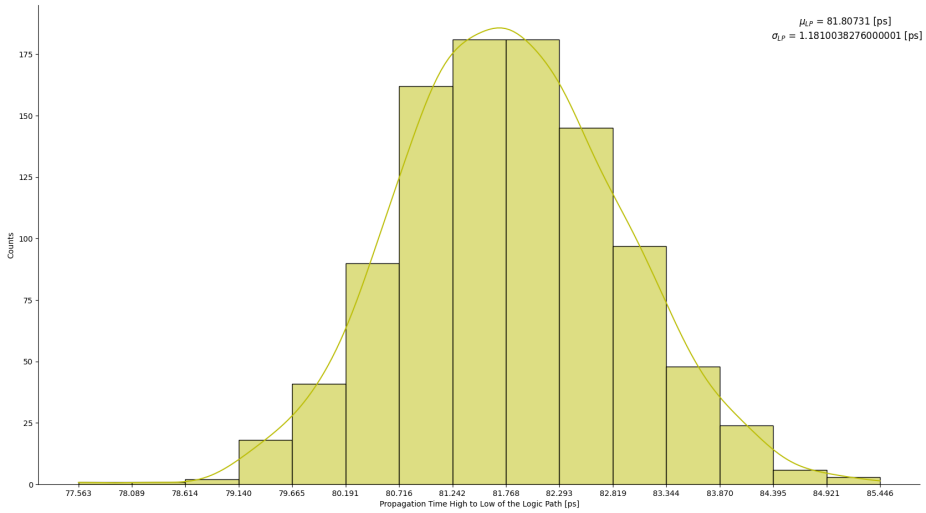


Figure 3: Monte Carlo results for t_{pHL} measurements at logic path

From Figures 3 and 4, it can be observed that $\mu_{t_{pHL}} = 81.9$ ps and $\mu_{t_{pLH}} = 78.59$ ps, with $\sigma_{t_{pHL}} = 1.181$ ps and $\sigma_{t_{pLH}} = 1.862$ ps.

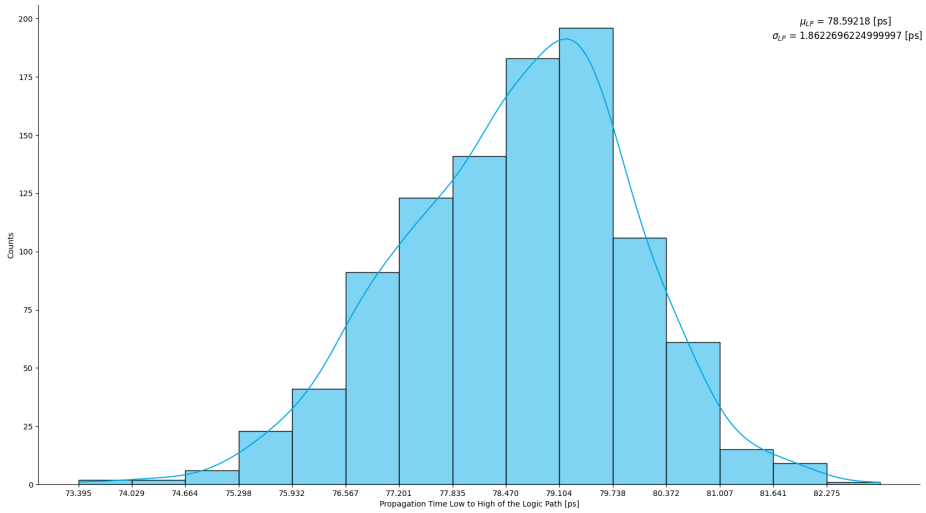


Figure 4: Monte Carlo results for t_{pLH} measurements at logic path

4 Comparison

Once both designs are completed, a comparison is made between using the SS design corner and considering statistical analysis. In this case, the impact of the SS corner on an already optimized design, as shown in Figure 5, is considered. There is an increase in propagation time (both for t_{pLH} and t_{pHL}) of more than 100 ps, resulting in more than double the estimated delay time.

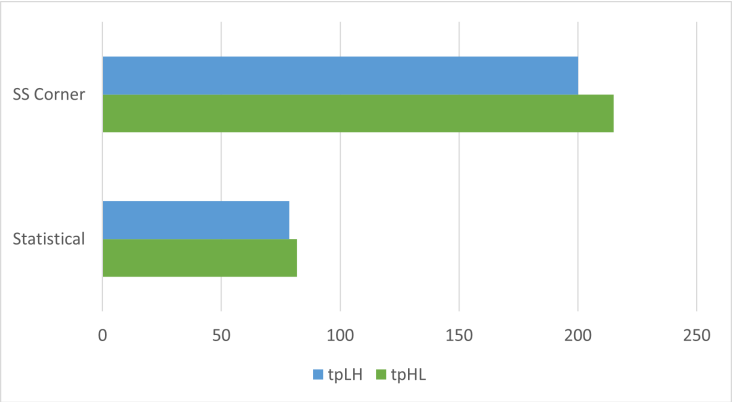


Figure 5: Monte Carlo results for t_{pLH} measurements at logic path

One consequence of considering a SS corner design is the over-sizing due to taking worst-case scenarios for the variation of H_{fin}, T_{fin}, and L_g, leading to an increase in both area consumption (at the layout level) and the total logic path current consumption. As mentioned earlier, to compensate for the SS corner, N_{fin} had to be increased to 4, as shown in Figure 6.

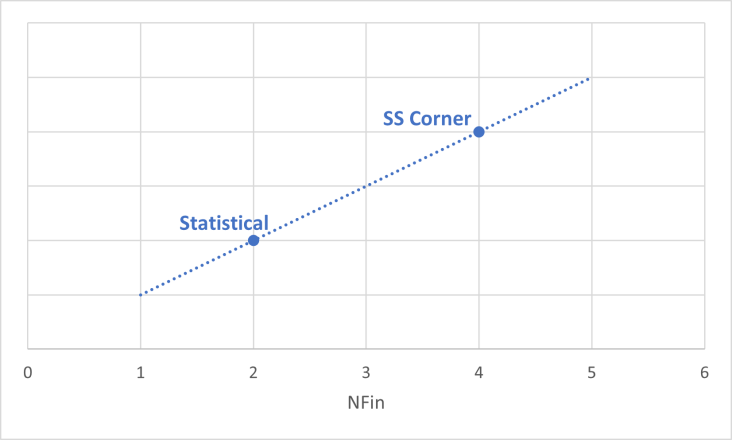


Figure 6: Monte Carlo results for t_{pLH} measurements at logic path

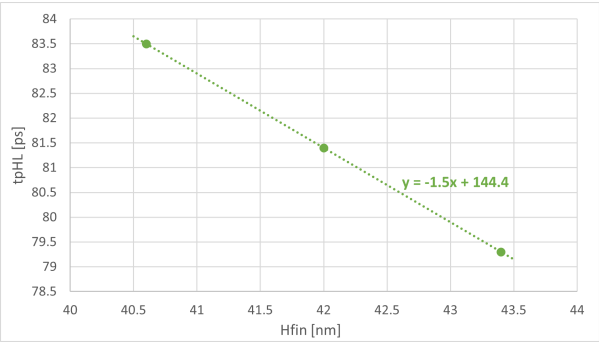
References

[1] Forero, F., Galliere, JM., Renovell, M. et al. *Detectability Challenges of Bridge Defects in FinFET Based Logic Cells.*, J Electron Test 34, 123–134 (2018).

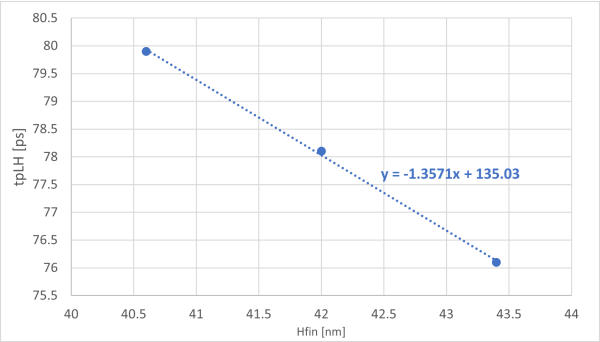
[2] Champac, V., & Garcia Gervacio, J.(2019), *Timing performance of nanometer digital circuits under process variations.*, Springer Nature.

5 Appendix A

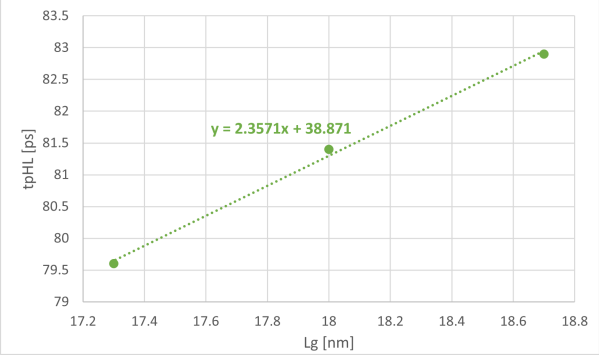
In this section, the results of sensitivity measurements for each parameter are shown. Similarly, these measurements were obtained for each of the six gates that make up the logical path in Figure 1.
The strategy involved creating a variable for each parameter and varying it by $\pm\sigma$, measuring the delay times for each. This way, it was possible to associate each time with the variation parameter, and by the slope value of the linear interpolation, measure the sensitivities.



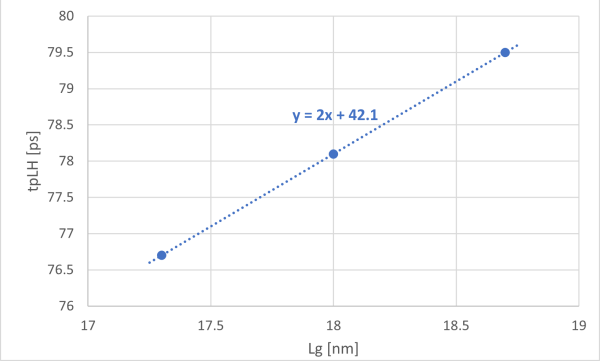
(a) t_{pHL} response due to H_{fin} variations



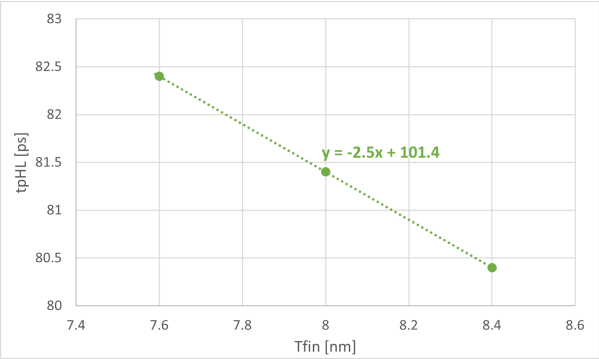
(b) t_{pLH} response due to H_{fin} variations



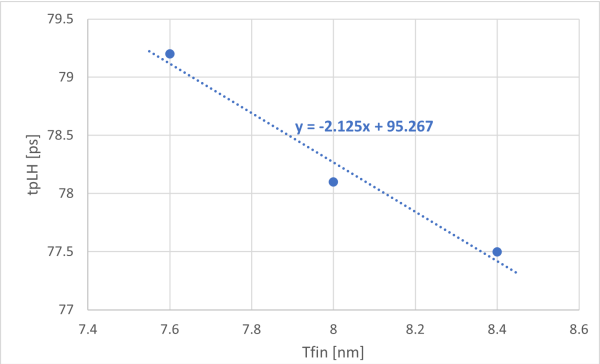
(c) t_{pHL} response due to L_g variations



(d) t_{pLH} response due to L_g variations



(e) t_{pHL} response due to T_{fin} variations



(f) t_{pLH} response due to T_{fin} variations

Figure 7: Sensitivities response due to H_{fin}, T_{fin} and L_g variations

Below is the SPICE code used for the statistical design in Section 3.

```
***** MONTE CARLO SIMULATION WITH SPATIAL CORRELATION *****

.option post=2 nomod brief MEASDGT=7 ingold=2 measform=1

.include 'FIN_Procces.lib'

**** PROCESS VARIATIONS *****

.param dxphig=gauss(0,90e-3,3)

.param dxtfinl=agauss(0,0.35e-9,3)
.param dxtfin=agauss(0,0.8e-9,3)

.param dxlgl=agauss(0,0.6e-9,3)
.param dxlg=agauss(0,1.4e-9,3)

.param dxhfin_n=agauss(0,4.2e-9,3)
.param dxhfin_p=agauss(0,4.2e-9,3)

**** CORRELATED VARIABLES GENERATION ******

.param uncorrelated_Hfin = agauss(0, '42n*0.2', 3)
.param Z1H = uncorrelated_Hfin
.param Z2H = uncorrelated_Hfin
.param Z3H = uncorrelated_Hfin
.param Z4H = uncorrelated_Hfin
.param Z5H = uncorrelated_Hfin
.param Z6H = uncorrelated_Hfin
.param Zc1H = 'Z1H + 0.5972*Z2H + 0.418*Z3H + 0.3322*Z4H + 0.2886*Z5H + 0.2656*Z6H'
.param Zc2H = '0.8020*Z2H + 0.4854*Z3H + 0.3339*Z4H + 0.2569*Z5H + 0.2164*Z6H'
.param Zc3H = '0.7678*Z3H + 0.5003*Z4H + 0.3644*Z5H + 0.2928*Z6H'
.param Zc4H = '0.7264*Z4H + 0.5123*Z5H + 0.3994*Z6H'
.param Zc5H = '0.6747*Z5H + 0.5171*Z6H'
.param Zc6H = '0.6081*Z6H'

.param uncorrelated_Tfin = agauss(0, '8n*0.2', 3)
.param Z1T = uncorrelated_Tfin
.param Z2T = uncorrelated_Tfin
.param Z3T = uncorrelated_Tfin
.param Z4T = uncorrelated_Tfin
.param Z5T = uncorrelated_Tfin
.param Z6T = uncorrelated_Tfin
.param Zc1T = 'Z1T + 0.5972*Z2T + 0.418*Z3T + 0.3322*Z4T + 0.2886*Z5T + 0.2656*Z6T'
.param Zc2T = '0.8020*Z2T + 0.4854*Z3T + 0.3339*Z4T + 0.2569*Z5T + 0.2164*Z6T'
.param Zc3T = '0.7678*Z3T + 0.5003*Z4T + 0.3644*Z5T + 0.2928*Z6T'
.param Zc4T = '0.7264*Z4T + 0.5123*Z5T + 0.3994*Z6T'
.param Zc5T = '0.6747*Z5T + 0.5171*Z6T'
.param Zc6T = '0.6081*Z6T'
```

```
.param uncorrelated_Lg = agauss(0, '14n*0.2', 3)
.param Z1Lg = uncorrelated_Lg
.param Z2Lg = uncorrelated_Lg
.param Z3Lg = uncorrelated_Lg
.param Z4Lg = uncorrelated_Lg
.param Z5Lg = uncorrelated_Lg
.param Z6Lg = uncorrelated_Lg
.param Zc1Lg = 'Z1Lg + 0.5972*Z2Lg + 0.418*Z3Lg + 0.3322*Z4Lg + 0.2886*Z5Lg + 0.2656*Z6Lg'
.param Zc2Lg = '0.8020*Z2Lg + 0.4854*Z3Lg + 0.3339*Z4Lg + 0.2569*Z5Lg + 0.2164*Z6Lg'
.param Zc3Lg = '0.7678*Z3Lg + 0.5003*Z4Lg + 0.3644*Z5Lg + 0.2928*Z6Lg'
.param Zc4Lg = '0.7264*Z4Lg + 0.5123*Z5Lg + 0.3994*Z6Lg'
.param Zc5Lg = '0.6747*Z5Lg + 0.5171*Z6Lg'
.param Zc6Lg = '0.6081*Z6Lg'

**** SUBCIRCUIT DEFINITION *****

.subckt inv1X in out vdd gd0
xp_a1 out in vdd vdd finfet_pmos numfin=1
xn_a1 out in gd0 gd0 finfet_nmos numfin=1

C_0_1 out gd0 1.713094e-17
C_0_2 out vdd 1.481918e-17
C_0_3 out in 1.689425e-16
C_1_2 gd0 vdd 1.676389e-18
C_1_3 gd0 in 4.723737e-17
C_2_3 vdd in 6.320916e-17

.ends inv

.subckt inv in out vdd gd0
xp_b1 out in vdd vdd finfet_pmos numfin=2 dxphigp=dxphig dxtfinp='dxtfin+dxtfinl' dxlgp='dxlg+dxlgl' dxhfinp=dxhfin_p
xn_b1 out in gd0 gd0 finfet_nmos numfin=2 dxphign=dxphig dxtfinn='dxtfin+dxtfinl' dxlgn='dxlg+dxlgl' dxhfinn=dxhfin_n

C_0_1 out in 2.286025e-16
C_0_2 out vdd 3.044704e-17
C_0_3 out gd0 3.096189e-17
C_0_4 out gd0 9.918963e-17
C_0_5 out vdd 5.027649e-17
C_1_2 in vdd 1.036297e-16
C_1_3 in gd0 1.036487e-16
C_1_4 in gd0 7.461482e-17
C_1_5 in vdd 3.300460e-17
C_2_3 vdd gd0 1.998977e-18
C_2_4 vdd gd0 4.749832e-17
C_2_5 vdd vdd 5.047028e-17
C_3_4 gd0 gd0 9.748517e-17
C_3_5 gd0 vdd 1.713151e-19
C_4_5 gd0 vdd 1.144488e-16
```



```
.ends inv
```

```
.subckt FO inA vddA gd0A
Xfo1 inA outA1 vdda 0 inv1x
cl1 outA1 gd0A 1f
Xfo2 inA outA2 vdda 0 inv1x
cl2 outA2 gd0A 1f
Xfo3 inA outA3 vdda 0 inv1x
cl3 outA3 gd0A 1f
Xfo4 inA outA4 vdda 0 inv1x
cl4 outA4 gd0A 1f
Xfo5 inA outA5 vdda 0 inv1x
cl5 outA5 gd0A 1f
Xfo6 inA outA6 vdda 0 inv1x
cl6 outA6 gd0A 1f
Xfo7 inA outA7 vdda 0 inv1x
cl7 outA7 gd0A 1f
Xfo8 inA outA8 vdda 0 inv1x
cl8 outA8 gd0A 1f
.ends FO


**** DESCRIPTION OF THE LOGIC PATH *****

Xinv1 in1 out1 vdda 0 inv
+ dxhfin=Zc1H dxtfin=Zc1T dxlg=Zc1Lg
xfo1 out1 vdda 0 FO
Xinv2 out1 out2 vdda 0 inv
+ dxhfin=Zc2H dxtfin=Zc2T dxlg=Zc2Lg
xfo2 out2 vdda 0 FO
Xinv3 out2 out3 vdda 0 inv
+ dxhfin=Zc3H dxtfin=Zc3T dxlg=Zc3Lg
xfo3 out3 vdda 0 FO
Xinv4 out3 out4 vdda 0 inv
+ dxhfin=Zc4H dxtfin=Zc4T dxlg=Zc4Lg
xfo4 out4 vdda 0 FO
Xinv5 out4 out5 vdda 0 inv
+ dxhfin=Zc5H dxtfin=Zc5T dxlg=Zc5Lg
xfo5 out5 vdda 0 FO
Xinv6 out5 out6 vdda 0 inv
+ dxhfin=Zc6H dxtfin=Zc6T dxlg=Zc6Lg
xfo6 out6 vdda 0 FO

vdd vdda 0 dc 0.8
vva in1 0 dc 0.8 pulse(0.8 0 5p 1p 1p 49p 100p)
```

```
***** DELAY MEASUREMENTS ******

** GATE 1 ***
.meas tran tpHL_G1 trig v(in1) val=0.4 td=0 rise=1 targ v(out1) val=0.4 fall=1
.meas tran tpLH_G1 trig v(in1) val=0.4 td=0 fall=2 targ v(out1) val=0.4 rise=2
** GATE 2 ***
.meas tran tpHL_G2 trig v(out1) val=0.4 td=0 rise=1 targ v(out2) val=0.4 fall=1
.meas tran tpLH_G2 trig v(out1) val=0.4 td=0 fall=2 targ v(out2) val=0.4 rise=2
** GATE 3 ***
.meas tran tpHL_G3 trig v(out2) val=0.4 td=0 rise=1 targ v(out3) val=0.4 fall=1
.meas tran tpLH_G3 trig v(out2) val=0.4 td=0 fall=2 targ v(out3) val=0.4 rise=2
** GATE 4 ***
.meas tran tpHL_G4 trig v(out3) val=0.4 td=0 rise=1 targ v(out4) val=0.4 fall=1
.meas tran tpLH_G4 trig v(out3) val=0.4 td=0 fall=2 targ v(out4) val=0.4 rise=2
** GATE 5 ***
.meas tran tpHL_G5 trig v(out4) val=0.4 td=0 rise=1 targ v(out5) val=0.4 fall=1
.meas tran tpLH_G5 trig v(out4) val=0.4 td=0 fall=2 targ v(out5) val=0.4 rise=2
** GATE 6 ***
.meas tran tpHL_G6 trig v(out5) val=0.4 td=0 rise=1 targ v(out6) val=0.4 fall=1
.meas tran tpLH_G6 trig v(out5) val=0.4 td=0 fall=2 targ v(out6) val=0.4 rise=2

** PATH ***
.meas tran tpHL_path trig v(in1) val=0.4 td=0 fall=1 targ v(out6) val=0.4 fall=1
.meas tran tpLH_path trig v(in1) val=0.4 td=0 rise=2 targ v(out6) val=0.4 rise=2

***** TRANSIENT ANALYSIS ******
.tran 0 400p sweep monte=1000
.end
```