Design of a four-quadrant multiplier in TSMC 65nm CMOS technology

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June 19, 2023

In this document, a four-quadrant multiplier topology is presented using the Gilbert cell as the main block. The design is carried out using the gm over ID technique, allowing the precise definition of the operating regions of the transistors for correct operation. The supply is 1.2 V and dissipates a power of X, with a linear input region of X. The multiplier has been simulated in the CADENCE Virtuoso environment using different waveforms, as well as the verification of the harmonic components through spectral analysis using a Hanning window as a delimiter in order to delimit the harmonics that could be added.

1 Double balanced Gilbert cell mixer

The conventional architecture of a double balanced Gilbert cell mixer shown in Figure 1 is composed of three distinct stages. A differential transconductance stage (TS) composed by the transistors pair M1 and M2 converts the RF voltages at the input ports in current signals for the switching stage (SS) composed by the transistors M3-M6. Finally, the switching stage is driven by the Local Oscillator (LO) to reverse the polarity of the RF inputs at the LO frequency rate.

Given the desired value of the load resistance RL, the mixer conversion gain (Av) is determined by the transconductance value (gm) of the transistors M1 and M2 [1]:

$$A_V \approx \left(\frac{2}{\pi}\right) g_m R_L \tag{1}$$

For this design, we use the inversion level of the transistor to select the best tradeoff between speed (f_T), intrinsic gain and power efficiency, thus, we define that strong inversion occurs for values of gm/ID in the 5-8 S/A range, while for values, in the 20-25 S/A range, the transistor operates in weak inversion.

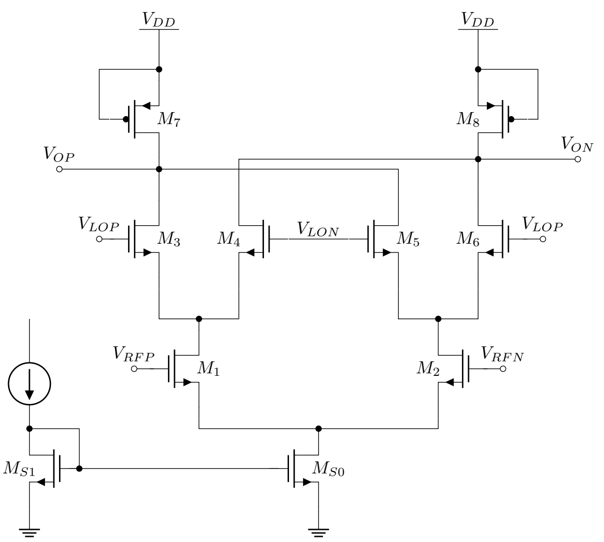

Figure 1: *Architecture of a conventional double balanced Gilbert cell mixer*

In order to know the regions of operation in the transistor (using the gm/ID parameter), Figure 2 is used, in this case, the maximum point of transconductance efficiency occurs in weak inversion (WI), and the minimum point of transconductance it happens in strong inversion (SI), the intermediate region is known as moderate inversion (MI) and at this point a maximum tradeoff is obtained between the gain and the transition frequency.

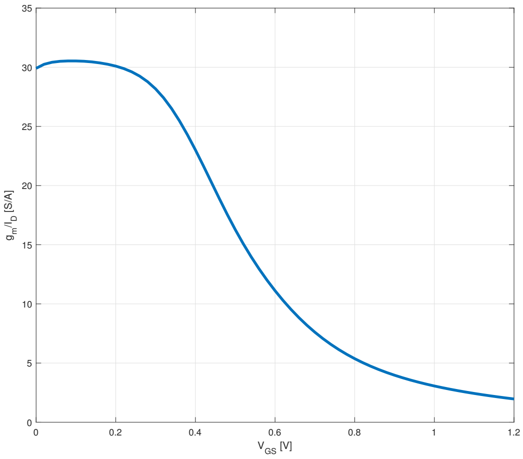

Figure 2: *Transconductance efficiency parameter for nMOS TSMC @ L = 130 nm*

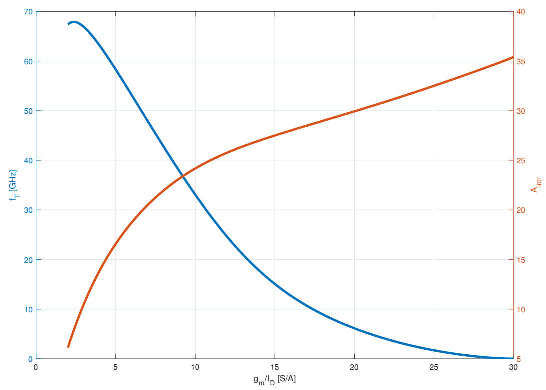

Figure 3: *Intrinsic Gain and Frequency Transition for nMOS TSMC @ L = 130 nm*

2 Design

As previously mentioned, gm/ID is used as a design parameter, and since the differential transconductance stage allows a greater voltage gain (expression 1), a value of 20 S/A is assigned, this also allows a greater input signal range (TS does not need to operate in saturation), for its part, the switching stage needs optimization in frequency, this is reflected in a much lower value of gm/ID (without reaching velocity saturation). Table 1 summarizes the proposed values of gm/ID.

Table 1: *gm/ID proposal*

RF and LO Stages		
Transistors	Operation Region	gm/ID
$M_{1,2}$	Moderate Invertion	20
M_{4-8}	Strong Invertion	10

It's well known that the gm/ID methodology results in imprecise dimensions for a future layout, which is why the method is used as the first approach to define the parameters. For this case, Table 2 shows the estimation of the parameters for the design of the multiplier.

Table 2: *Estimated parameters to design the Gilbert Cell*

Symbol	Design parameter description	Value
L	Gate length of the transistors	0.13 μm
W_{RF}	Width of the RF stage transistors	130 μm
W_{LO}	Width of the LO stage transistors	65 μm
$V_{OV,RF}$	Overdrive voltage for RF stage	60 mV
$V_{OV,LO}$	Overdrive voltage for LO stage	120 mV

3 Results obtained

The following parameters were used in the Cadence Virtuoso environment to simulate.

- V_{DD} = 1.2 V
- V_{LO}: V_a = 100 mV, f = 100 MHz
- V_{RF}: V_a = 10 mV, f = 10 MHz
- R_L = 200 Ω

Table 3 shows the summary of the operating points as well as its transconductance characteristics to determine the region of operation of each stage of the multiplier.

Table 3: *Summary of the operating points of the MOSFETs used in the design*

Notation	RF stage transistors	LO stage transistors
I_{DS}	953.7 μA	477.4 μA
g_m	14.08 mS	6.86 μS
V_{th}	549.4 mV	548.6 mA
V_{ds}	86 mV	936.8 mA
V_{gs}	563.5 mV	527 mA

4 Conclusions

In conclusion, this document presents a four-quadrant multiplier topology based on the Gilbert cell. The design employs the gm over ID technique to accurately define the operating regions of the transistors, ensuring proper functionality. Operating with a 1.2 V supply, the multiplier's power dissipation and linear input region are specified as X. Simulations in the CADENCE Virtuoso environment, using various waveforms and spectral analysis with a Hanning window, confirm the performance and harmonic component verification of the multiplier.

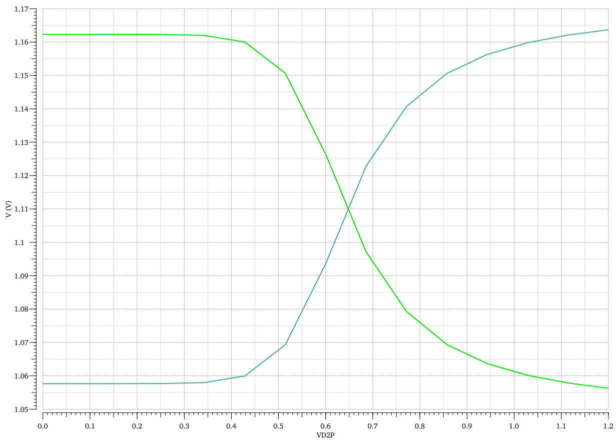

Figure 4: *CD Voltage Response*

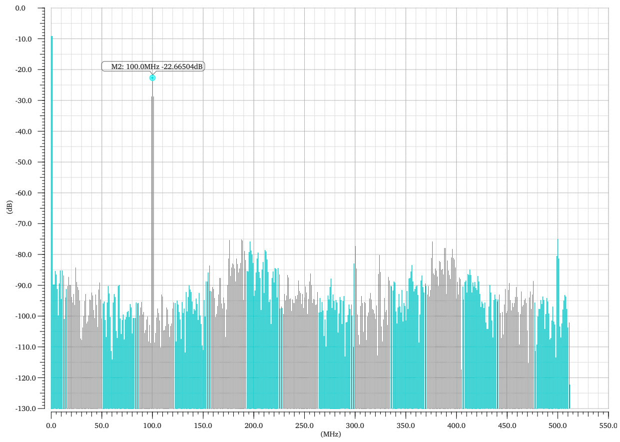

Figure 7: *Frequency spectrum of the LO signal*

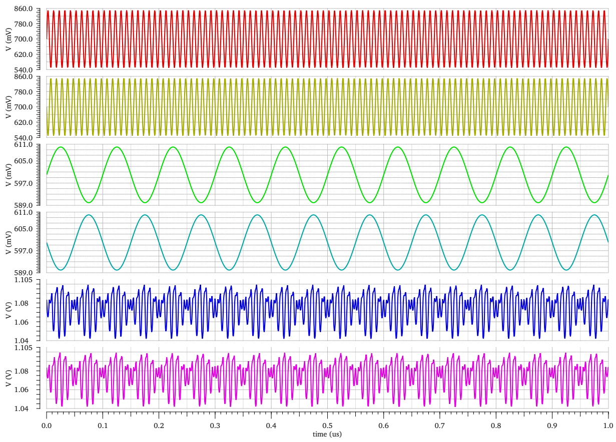

Figure 5: *Transient response*

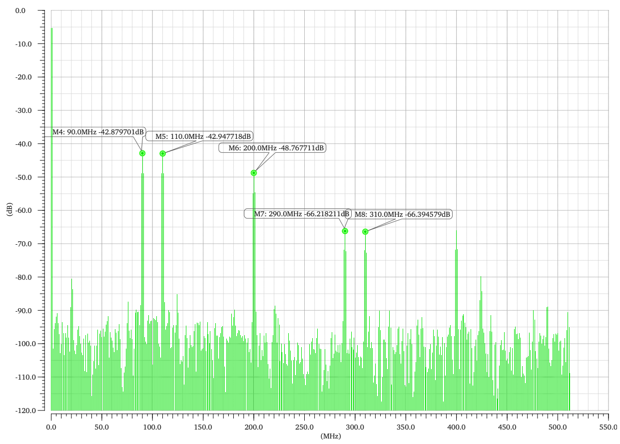

Figure 8: *Frequency spectrum of the FN signal*

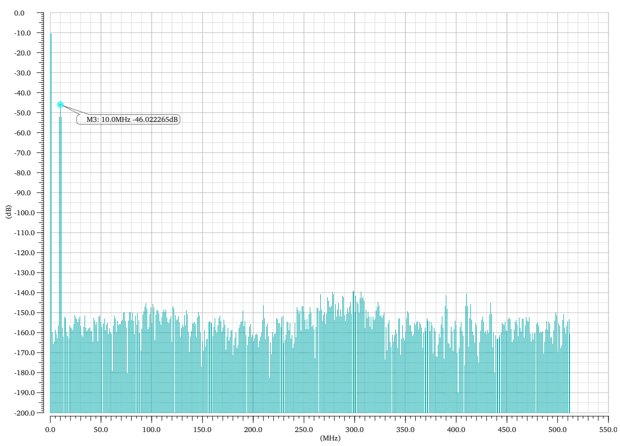

Figure 6: *Frequency spectrum of the RF signal*