Compensation Methods for Two-Stage Amplifiers

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1 Driving Point Impedance Analysis

Impedance-based modeling methods (such as the Driving Point Impedance technique) are a convenient way to generate the transfer function of a linear system directly from its block diagram. This method divides the analysis problem into two subproblems, one for finding the current into an AC ground and the other for finding the port impedance. In this way, the voltage response of a node 'x' is given as the product of two components:

$$V_{out,x} = I_{SC,x} DPI_{out,x} \tag{1}$$

where $I_{SC,x}$ is the Short Circuit Current at the node 'x' and $DPI_{out,x}$ is the impedance measured at the same node, taking into account the passive equivalent of the independent sources. The general structure of the two-stage miller amplifier to be analized is shown in Fig. 1.

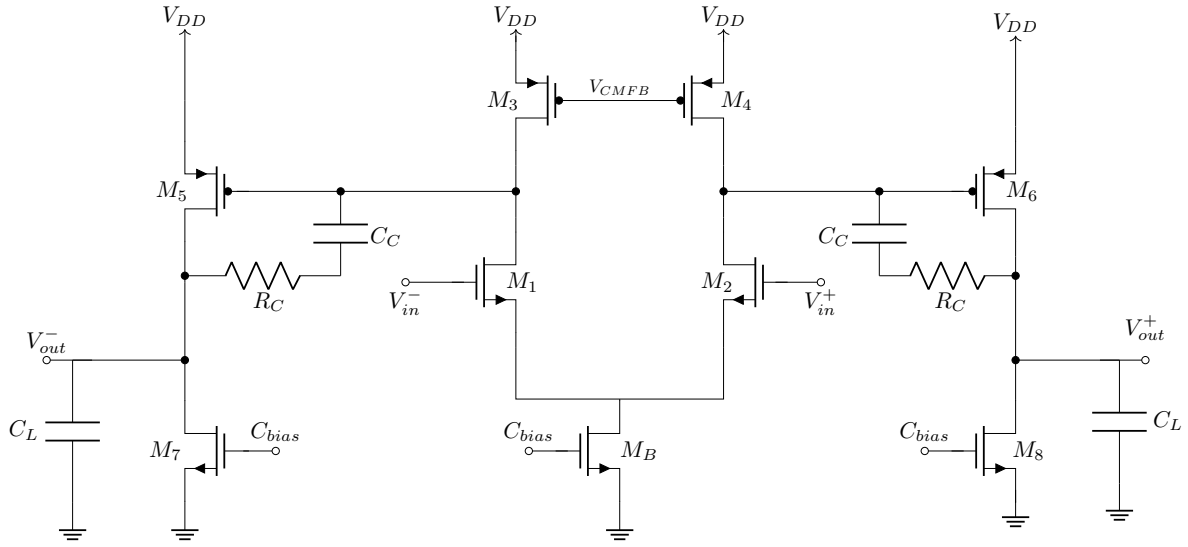


Figure 1: Architecture of a conventional Two Stages Miller Amplifier

For the DPI analysis, we start from the small signal model associated with the amplifier and since it is a totally differential amplifier, it is possible to analyze only half of the circuit (without considering the CMFB stage), the equivalent circuit is shown in Fig. 2.
In this model, it is assumed that any parasitic poles in the first stage are at frequencies much higher so that can be ignored, where R_1 is the output resistance of the first stage ($R_{ds2}||R_{ds4}$), C_1=$C_{db2} + C_{db4}$, $R_2 = R_{ds6}||R_{ds8}$ and $C_2 = C_{db6} + C_{db8} + C_L$.

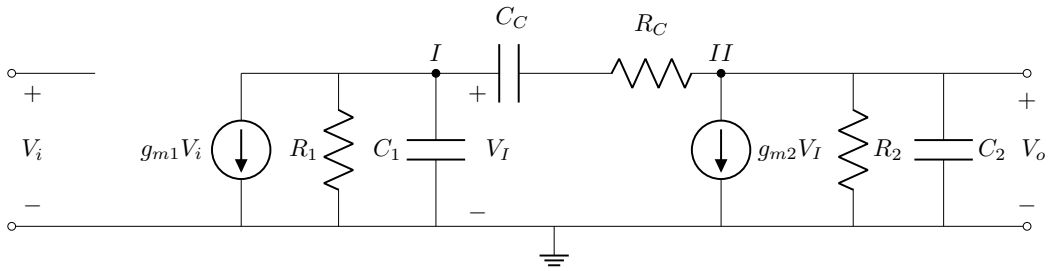


Figure 2: Small signal model of amplifier shown in Fig. 1

For the analysis we can consider two DPI associated to each node (I and II), applying KCL to each node results

$$g_{m1}V_i + g_1V_I + sC_1V_I + (V_I - V_o)(sC_C + g_C) = 0 \tag{2}$$

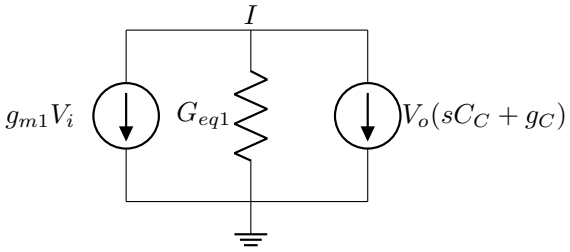
Reordering, the Eq. (2) results in

$$g_{m1}V_i + [g_1 + g_C + s(C_1 + C_C)]V_I - V_o(sC_C + g_C) = 0 \tag{3}$$

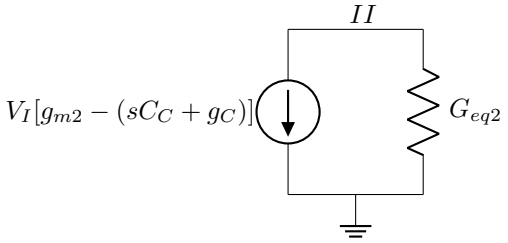
Similarly for node II:

$$V_I[g_{m2} - (sC_C + g_C)] + V_o[g_2 + g_C + s(C_2 + C_C)] = 0 \tag{4}$$

From the Eq. (3) we can notice that the feedback is modeled as a current source of value $V_o(sC_c + g_C)$ where g_C is the conductance associated with the compensation resistor (R_C) .The equivalent circuits associated with Eq. (3) and (4) are shown in Fig. 3.



(a) Equivalent circuit associated to node I



(b) Equivalent circuit associated to node II

Figure 3: DPI analysis to each node

Where

$$G_{eq1} = g_1 + g_C + s(C_1 + C_C) \tag{5}$$

$$G_{eq2} = g_2 + g_C + s(C_2 + C_C) \tag{6}$$

From the Eq. (5) and (6) we can notice that the DPI value at node I can be denoted as the inverse of G_{eq1} and similarly for node II, in this way it is possible to obtain the Signal Flow Diagram (SFD) associated with the circuit in the Fig. 2.

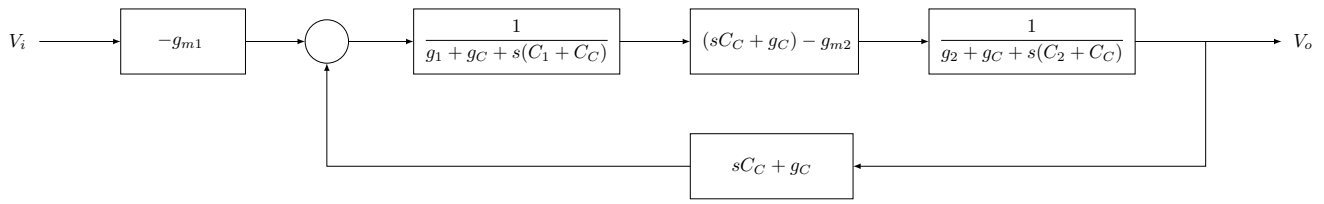


Figure 4: Signal Flow Diagram resulting from DPI analysis

1.1 Function Transfer Analysis

The open loop gain is obtained as the direct path of the SFD shown in Fig. 4

$$\frac{V_o}{V_i} = \frac{-g_{m1}[sC_C + g_C - g_{m2}]}{[g_1 + g_C + s(C_1 + C_C)][g_2 + g_C + s(C_2 + C_C)] - (sC_C + g_C)(sC_C + g_C - g_{m2})} \tag{7}$$

Solving the numerator, it's observed that there is a zero of value

$$s = \frac{g_{m2} - g_C}{C_C} \tag{8}$$

Reordering the expressions of the denominator, we have

$$D(s) = [(C_1+C_2)C_C+C_1C_2]s^2+[(g_1+g_2+g_{m2})C_C+(C_1+C_2)g_C+C_1g_2+g_1C_2]s+(g_1+g_2+g_{m2})g_C+g_1g_2 \tag{9}$$

From Eq. (9) it's observed that there are two poles in the transfer function.In this work, a previous design (under NEF optimization) will be analyzed, the characteristics are summarized in the Table 1.

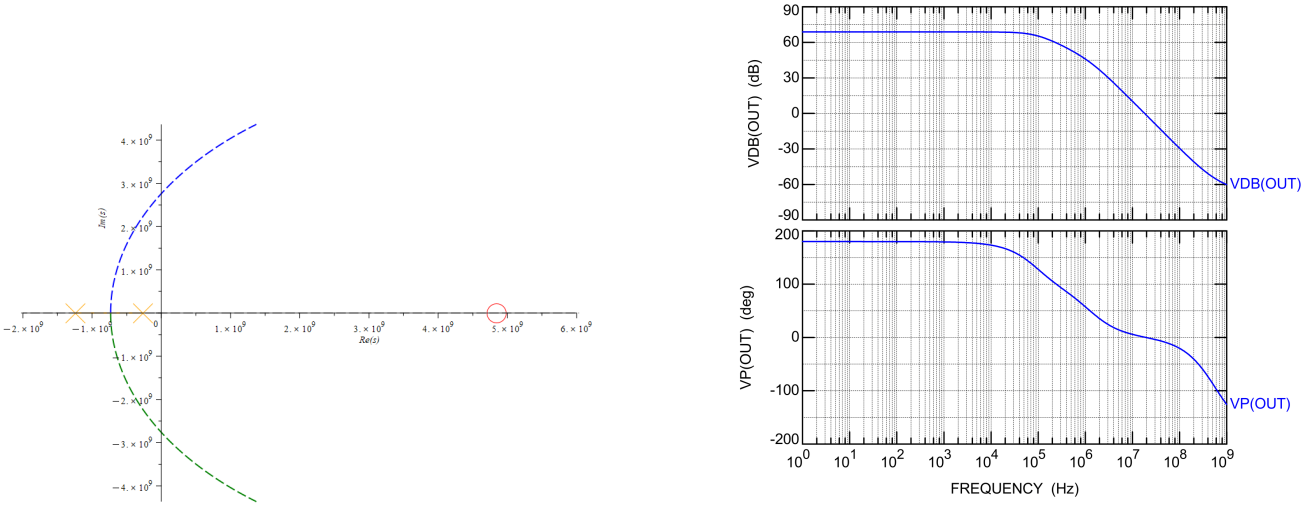
Table 1: Open-loop characterization

Transistor	W/L [μm/μm]	I_D [μA]	g_m [μS]	g_{ds}[μS]	C_{db}[fF]
$M_{1,2}$	60/0.54	4.95	134.9	2.06	48.9
$M_{3,4}$	50/0.54	4.95	104.8	48.07	39.31
$M_{5,6}$	50/10	21.6	96.9	37.79	25.08
$M_{7,8}$	20/10	21.6	168	3.62	17.24

The objective of this work is to analyze the location of the poles and zeros found in the amplifier using an alternative technique (DPI), which has the advantage of graphically showing each of the stages of the amplifier using a Signal Flow Diagram, so any modification that is made later can be added in the form of a block in the corresponding stage.

1.2 Root Locus Plots

According to Table [1] and the above mentioned, in this design C_1=88.21 fF, C_2=42.32 fF, $R_1 \approx 20$ kΩ and $R_2 \approx 24$ kΩ.
Figure 5 shows the location of the poles and the zero of the amplifier without compensation that is summarized in a case of instability if the loop is closed in its application (because zero is in the right region of the plane), this parameter is measured by means of the phase margin (PM) at the unity gain frequency.

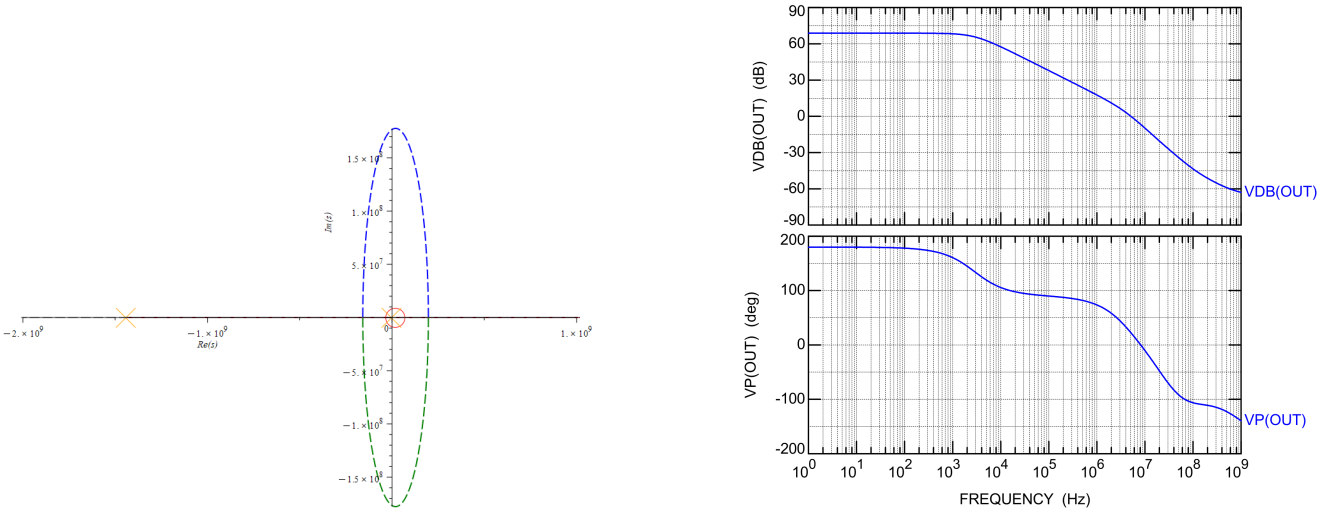


(a) Root Locus for no compensated case

(b) Frequency response for first case

Figure 5: Two-stages Amplifier no compensated

Figure 6 shows the result of canceling the zeal with one pole and thus achieving a PM = 50°, in this way knowing the exact location of each of the poles it is possible to compensate the circuit for an appropriate phase margin for the particular application.



(a) Root Locus for no compensated case

(b) Frequency response for second case

Figure 6: Two-stages Amplifier compensated

2 Bulk Feedback Compensation

In this section, we discuss a very basic two-stage amplifier (shown in Fig. 7) that uses the Bulk terminal of the first stage load transistor (M_2) to compensate for phase margin.
It is based on the injection of current in the output node of the first stage using a resistive and capacitive network that allows to vary the Source-Bulk Voltage, the feedback network is reflected in the transfer function as a zero, the operation of this terminal is limited to a certain voltage range to avoid turning on the parasitic diodes found in the transistor.

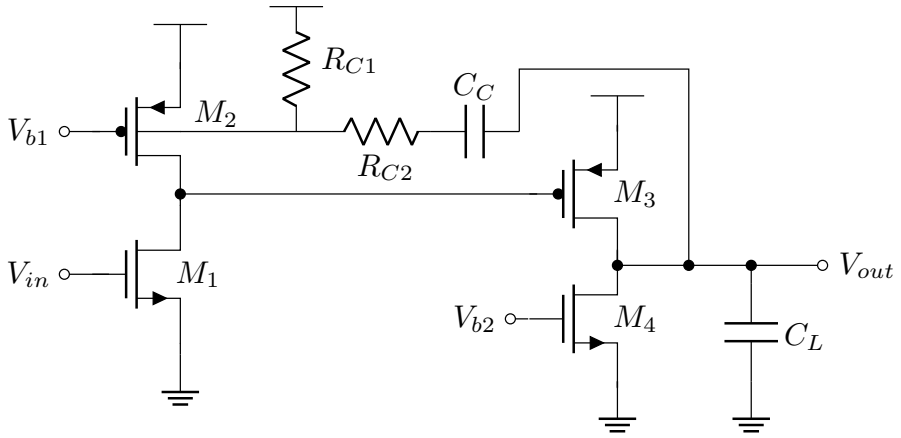


Figure 7: Two Stages Amplifier with Bulk Compensation

In a second order approximation, we have the following small signal equivalent circuit

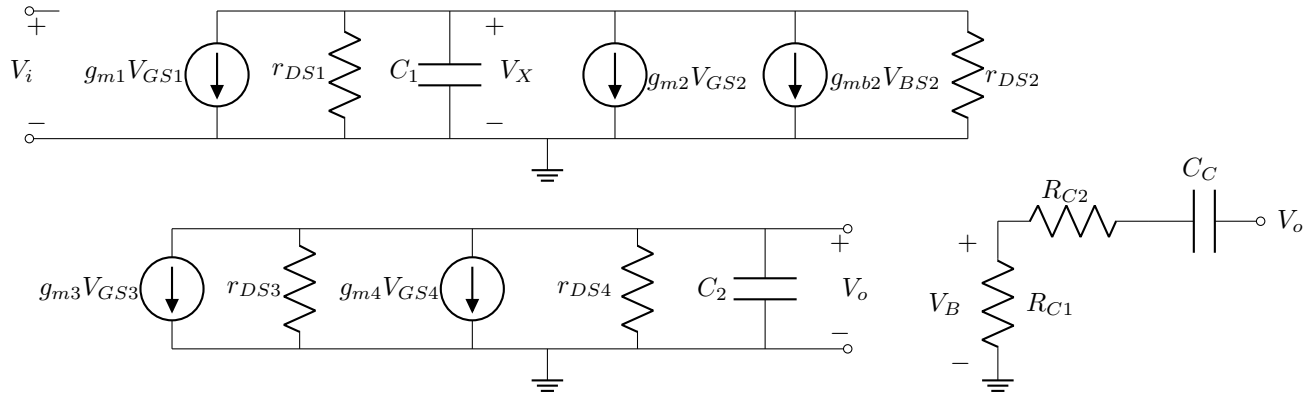


Figure 8: Small signal equivalent circuit of Fig. 7

Where $V_{GS1} = V_i$, $V_{GS3} = V_x$, $V_{BS2} = V_B$, $V_{GS2} = V_{GS4} = 0$, the simplified equivalent circuit is shown in Fig. 9. The equivalent resistances are $R_1 = r_{DS1}||r_{DS2}$ and $R_2 = r_{DS3}||r_{DS2}$, it should be noted that the feedback network is given by the factor voltage divider

$$V_B = V_o \frac{sC_C R_{C1}}{1 + s(R_{C1} + R_{C2})C_C} = V_o K \tag{10}$$

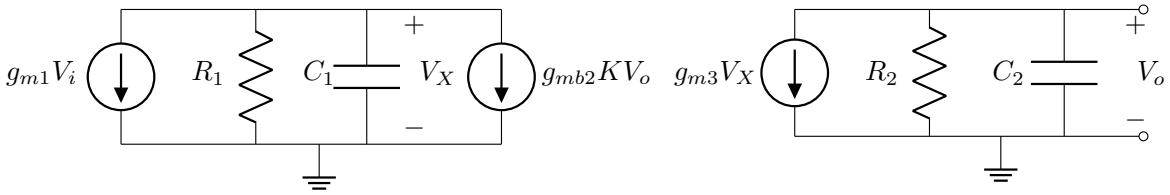


Figure 9: Simplified equivalent circuit (feedback network not shown)

Simplifying, we obtain the equivalent circuit shown in Fig. 9, and applying KCL in each node we have

$$g_{m1}V_i + g_{mb2}V_oK + V_X sC_1 + \frac{V_X}{R_1} = 0 \tag{11}$$

$$g_{m3}V_X + \frac{V_o}{R_2} + V_o sC_2 = 0 \tag{12}$$

In this way solving the Eq. (11) and (12), the function transfer results in a 3 pole system

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m3}R_1R_2(1 + s(R_{C1} + R_{C2})C_C)}{\alpha_1 s^3 + \alpha_2 s^2 + \alpha_3 s + 1} \tag{13}$$

where

$$\alpha_1 = C_1C_2C_CR_1R_2(R_{C1} + R_{C2}) \tag{14}$$

$$\alpha_2 = (R_{C1} + R_{C2})(C_1R_1 + C_2R_2)C_C + C_1C_2R_1R_2 \tag{15}$$

$$\alpha_3 = (-R_1R_2R_{C1}g_{m3}g_{mb2} + R_{C1} + R_{C2})C_C + C_1R_1 + C_2R_2 \tag{16}$$

We can notice that the feedback network add a zero in the transfer function located in

$$s = \frac{-1}{C_C(R_{C1} + R_{C2})} \tag{17}$$

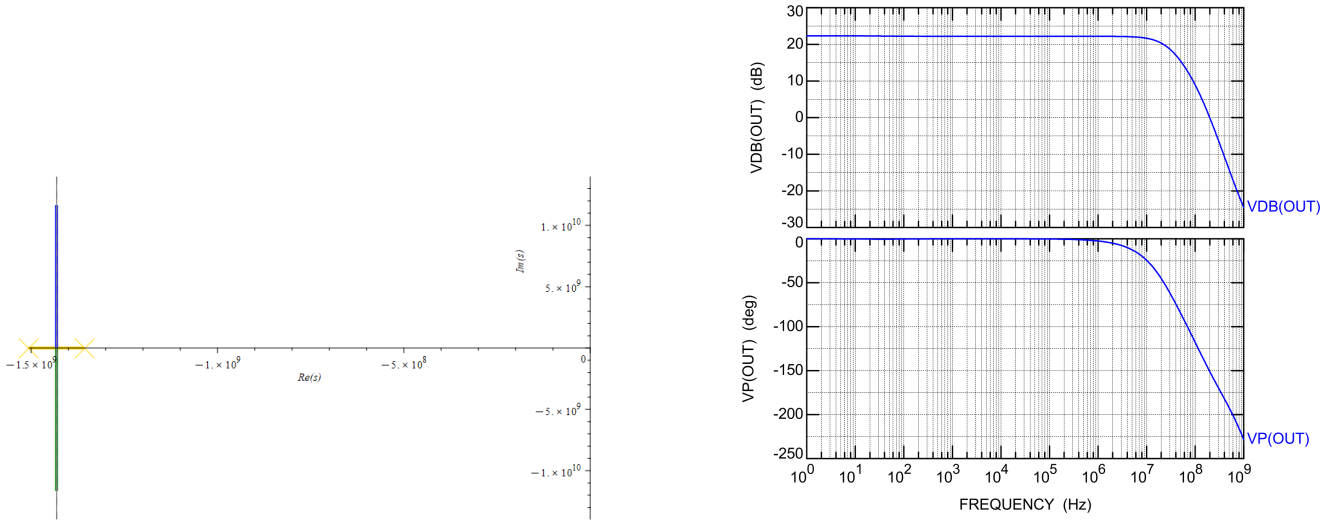
2.1 Root Locus Plots

In this work, the implemented design has the characteristics shown in Table 2, obtaining an open loop gain of 25 dB.

Table 2: Open-loop characterization

Transistor	W/L [μm/μm]	I_D [μA]	g_m [μS]	g_{ds}[μS]	C_{db}[fF]
M_1	15/4	154.1	478.4	38.08	13.8
M_2	20.2/0.9	154.1	536.07	4.92	14.74
M_3	20.2/0.9	281.1	428.23	35.95	17.81
M_4	15/4	281.1	686.03	6.1	11.23

The response of the uncompensated two-stage amplifier was analyzed (assuming $R_{C1} = R_{C2} = C_C = 0$), and figure 10 shows the results where it can be seen that although the gain is lower than that obtained in the previous configuration, the phase margin is approximately 15°, the objective is analyse the effect of using the transconductance due to the Bulk (g_{mb2}) as feedback current sum point and its compensation in the output stage.



(a) Root Locus for no compensated case

(b) Frequency response for no compensated case

Figure 10: Two-stages Amplifier no compensated

The value of the transconductance of the Bulk of the transistor M_2 that works as feedback is 173.3 μS, this factor will allow to inject a current to the first stage depending on the output signal.
The first feedback network proposed has as a compensation network $R_{C1} = 200\Omega$, $R_{C1} = 5\text{k}\Omega$ $C_C = 1\text{pF}$, resulting in poles of values

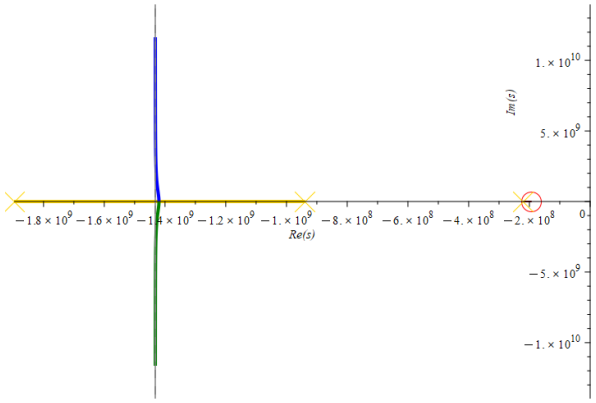
$$P_1 = -0.22GHz \tag{18}$$

$$P_2 = -0.94GHz \tag{19}$$

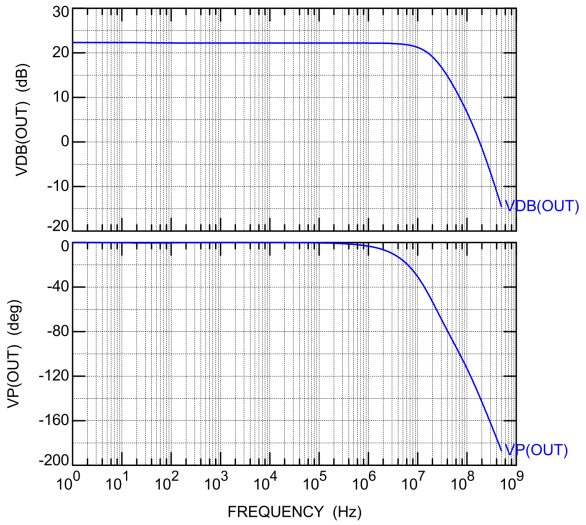
$$P_3 = -1.89GHz \tag{20}$$

In the Fig. 11, the root locus plots and the AC response of the amplifier are shown, the measured phase margin from the first proposal is approximately 45°.

The disadvantage of using the Bulk as a feedback stage is that the maximum factor must be less than the threshold voltage of the parasitic transistor, which further limits the phase margin improvement, however, depending on the application a PM = 45° is a good compensation option.



(a) Root Locus for compensated case I



(b) Frequency response for compensated case I

Figure 11: Two-stages Amplifier compensated (Case I)

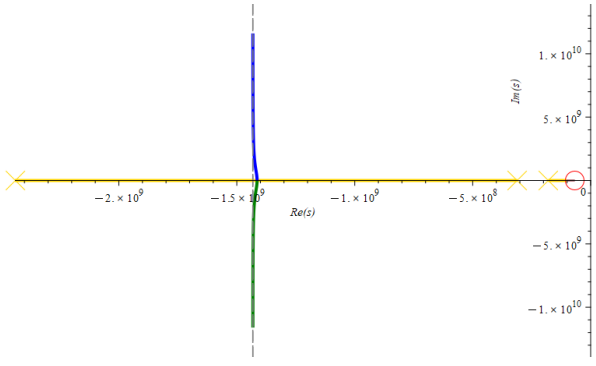
The second compensation proposal is using $R_{C1} = 500\Omega$, $R_{C1} = 2\text{k}\Omega$ $C_C = 6\text{pF}$, resulting in poles of values

$$P_1 = -0.18GHz \tag{21}$$

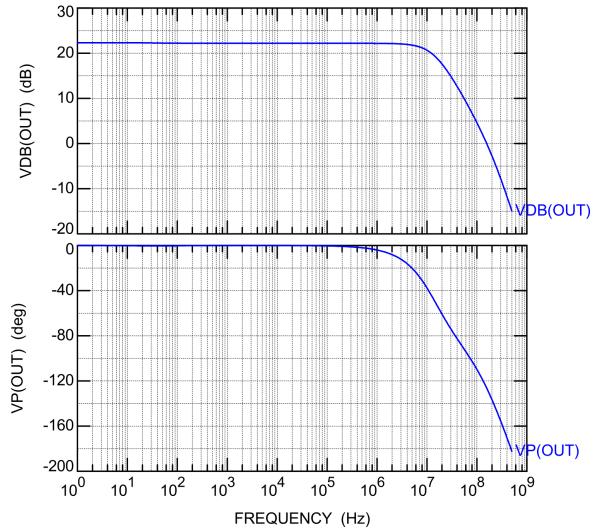
$$P_2 = -0.31GHz \tag{22}$$

$$P_3 = -2.44GHz \tag{23}$$

As seen in the Fig. 12, the compensation proposal allows obtaining a PM = 56° approximately.



(a) Root Locus for compensated case II



(b) Frequency response for compensated case II

Figure 12: Two-stages Amplifier compensated (Case II)

3 Conclusions

In this project, an impedance analysis method (DPI Method) was studied, which allowed obtaining the Signal Flow Diagram and thus obtaining the transfer function of the Miller amplifier more quickly and, seen as a system, analyzing the location of the poles. and zeros from a previously made design.
In the bulk compensation section, it would be a good practice to analyze the implemented circuit using the DPI Method and to analyze using the SFD of the circuit and through blocks to deepen whether a more complex configuration would allow improving the phase margin of the complete system.

References

[1] D. Johns and K. Martin, *Analog Integrated Circuit Design*, ed Wiley, 1st e., 1997.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill International edition, 2001.

[3] A. Ochoa, *Feedback in Analog Circuits*, Springer, 2016.