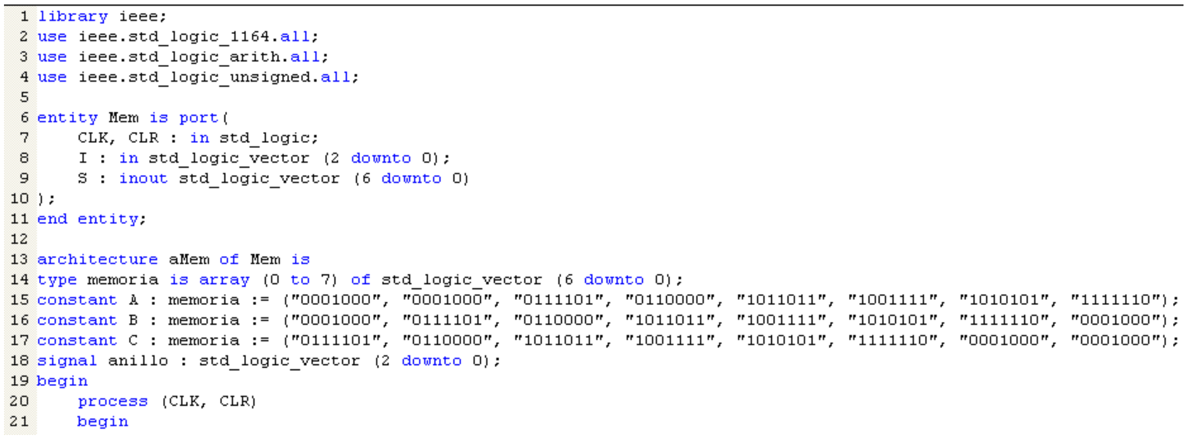
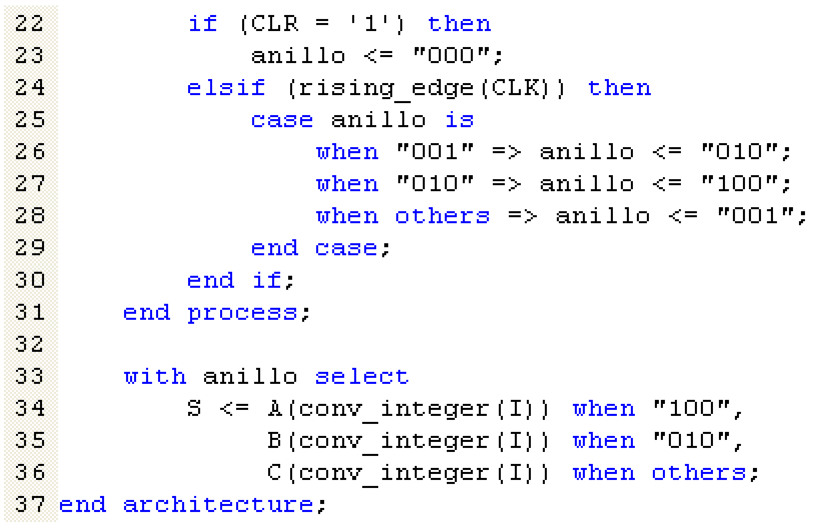
Martínez Coronel Brayan Yosafat

## CÓDIGO FUENTE

### PRIMERA MEMORIA

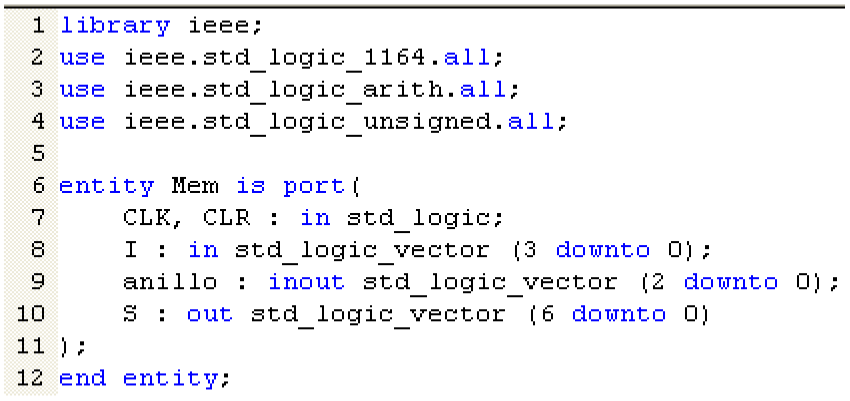


```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity Mem is port(
    CLK, CLR : in std_logic;
    I : in std_logic_vector (2 downto 0);
    S : inout std_logic_vector (6 downto 0)
);
end entity;

architecture aMem of Mem is
type memoria is array (0 to 7) of std_logic_vector (6 downto 0);
constant A : memoria := ("0001000", "0001000", "0111101", "0110000", "1011011", "1001111", "1010101", "1111110");
constant B : memoria := ("0001000", "0111101", "0110000", "1011011", "1001111", "1010101", "1111110", "0001000");
constant C : memoria := ("0111101", "0110000", "1011011", "1001111", "1010101", "1111110", "0001000", "0001000");
signal anillo : std_logic_vector (2 downto 0);
begin
    process (CLK, CLR)
    begin
```

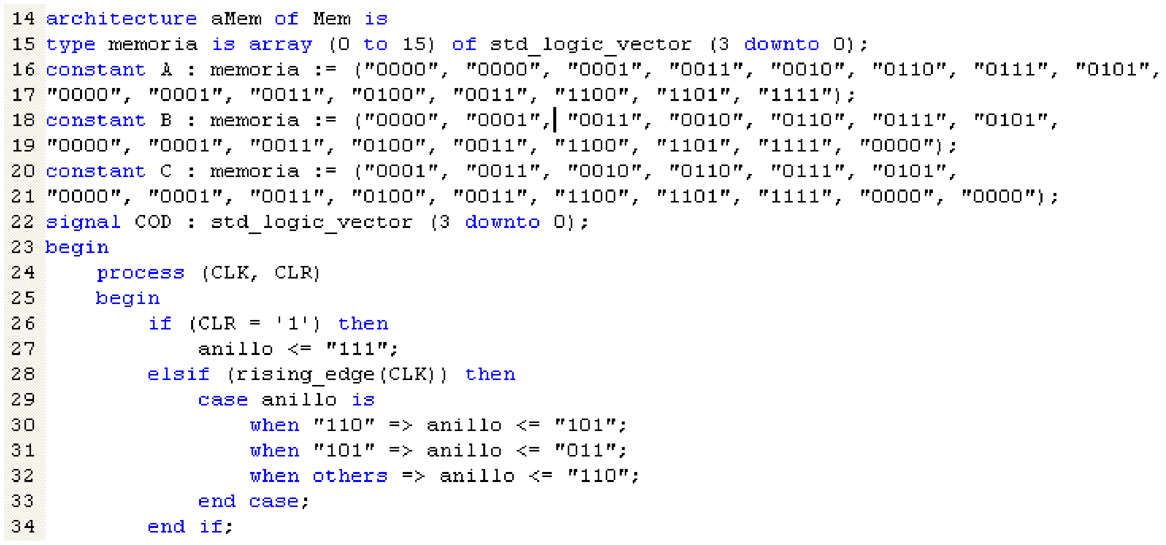


```vhdl
        if (CLR = '1') then
            anillo <= "000";
        elsif (rising_edge(CLK)) then
            case anillo is
                when "001" => anillo <= "010";
                when "010" => anillo <= "100";
                when others => anillo <= "001";
            end case;
        end if;
    end process;

    with anillo select
        S <= A(conv_integer(I)) when "100",
             B(conv_integer(I)) when "010",
             C(conv_integer(I)) when others;
end architecture;
```

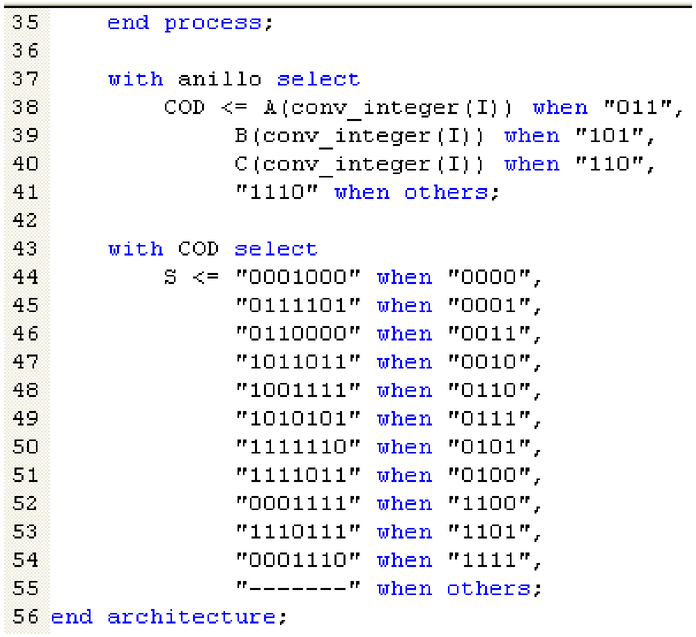
### SEGUNDA MEMORIA



```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity Mem is port(
    CLK, CLR : in std_logic;
    I : in std_logic_vector (3 downto 0);
    anillo : inout std_logic_vector (2 downto 0);
    S : out std_logic_vector (6 downto 0)
);
end entity;
```

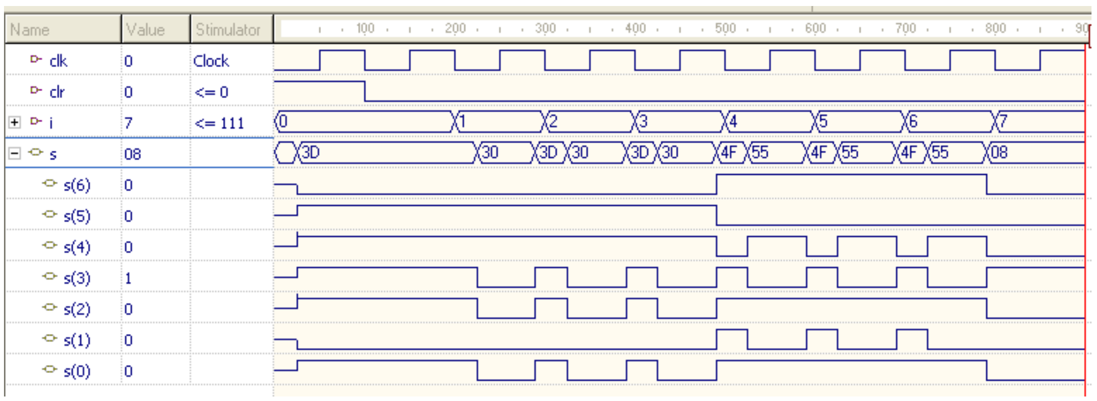


```
architecture aMem of Mem is
type memoria is array (0 to 15) of std_logic_vector (3 downto 0);
constant A : memoria := ("0000", "0000", "0001", "0011", "0010", "0110", "0111", "0101",
"0000", "0001", "0011", "0100", "0011", "1100", "1101", "1111");
constant B : memoria := ("0000", "0001", "0011", "0010", "0110", "0111", "0101",
"0000", "0001", "0011", "0100", "0011", "1100", "1101", "1111", "0000");
constant C : memoria := ("0001", "0011", "0010", "0110", "0111", "0101",
"0000", "0001", "0011", "0100", "0011", "1100", "1101", "1111", "0000", "0000");
signal COD : std_logic_vector (3 downto 0);
begin
    process (CLK, CLR)
    begin
        if (CLR = '1') then
            anillo <= "111";
        elsif (rising_edge(CLK)) then
            case anillo is
                when "110" => anillo <= "101";
                when "101" => anillo <= "011";
                when others => anillo <= "110";
            end case;
        end if;
```



```
    end process;

    with anillo select
        COD <= A(conv_integer(I)) when "011",
             B(conv_integer(I)) when "101",
             C(conv_integer(I)) when "110",
             "1110" when others;

    with COD select
        S <= "0001000" when "0000",
             "0111101" when "0001",
             "0110000" when "0011",
             "1011011" when "0010",
             "1001111" when "0110",
             "1010101" when "0111",
             "1111110" when "0101",
             "1111011" when "0100",
             "0001111" when "1100",
             "1110111" when "1101",
             "0001110" when "1111",
             "-------" when others;
end architecture;
```

## SIMULACIONES EN GALAXY



| Name | Value | Stimulator |
|---|---|---|
| clk | 0 | Clock |
| clr | 0 | <= 0 |
| i | 7 | <= 111 |
| s | 08 | |
| s(6) | 0 | |
| s(5) | 0 | |
| s(4) | 0 | |
| s(3) | 1 | |
| s(2) | 0 | |
| s(1) | 0 | |
| s(0) | 0 | |

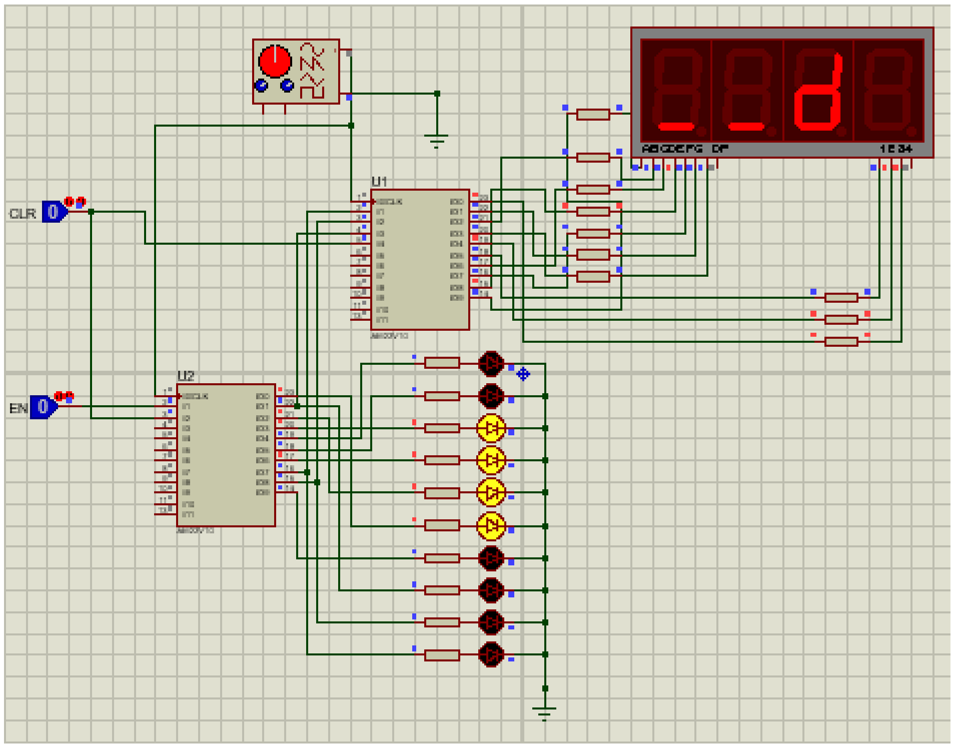
## SIMULACIÓN EN PROTEUS

### CONTADOR

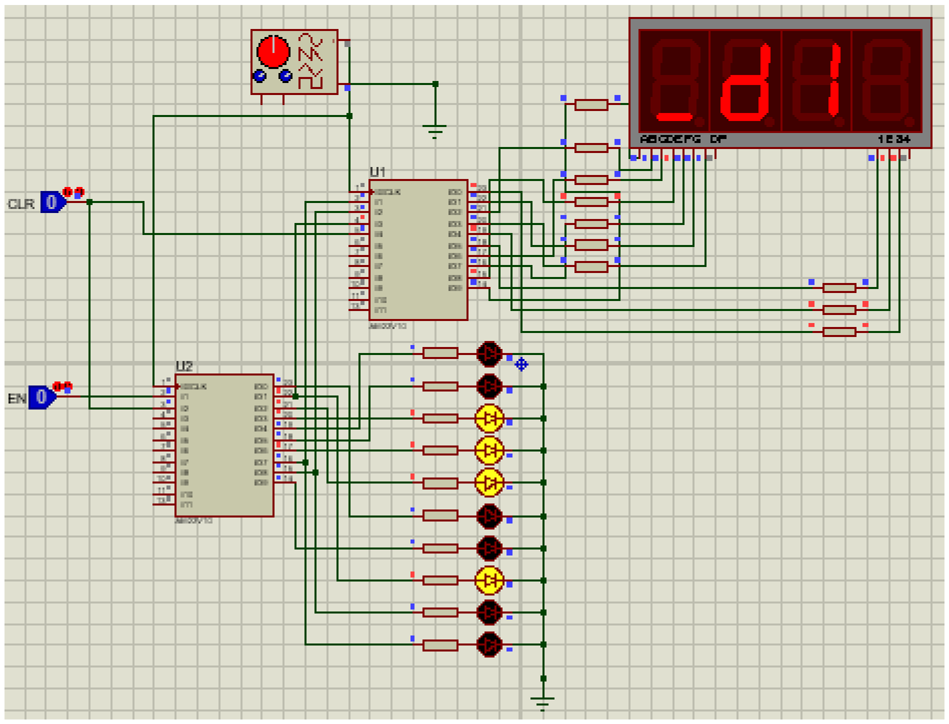
```
                                 C22V10

                  __________________________________________
        clk =|  1|                                      |24|* not used
         en =|  2|                                      |23|= s(5)
        clr =|  3|                                      |22|= s(7)
   not used *|  4|                                      |21|= s(4)
   not used *|  5|                                      |20|= s(2)
   not used *|  6|                                      |19|= s(0)
   not used *|  7|                                      |18|= s(1)
   not used *|  8|                                      |17|= s(3)
   not used *|  9|                                      |16|= s(9)
   not used *|10|                                       |15|= s(8)
   not used *|11|                                       |14|= s(6)
   not used *|12|                                       |13|* not used
                  __________________________________________
```

### PRIMER MEMORIA

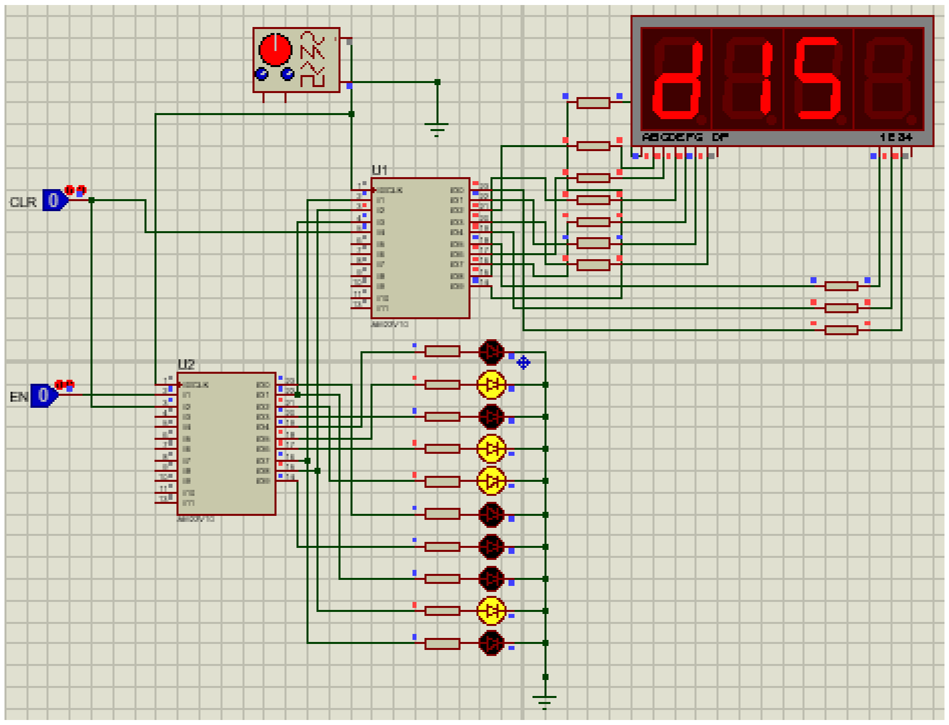
```
                                 C22V10

                  __________________________________________
        clk =|  1|                                      |24|* not used
       i(2) =|  2|                                      |23|= anillo(0)
       i(1) =|  3|                                      |22|= s(1)
       i(0) =|  4|                                      |21|= s(5)
        clr =|  5|                                      |20|= s(0)
   not used *|  6|                                      |19|= anillo(1)
   not used *|  7|                                      |18|= anillo(2)
   not used *|  8|                                      |17|= s(4)
   not used *|  9|                                      |16|= s(2)
   not used *|10|                                       |15|= s(3)
   not used *|11|                                       |14|= s(6)
   not used *|12|                                       |13|* not used
                  __________________________________________
```



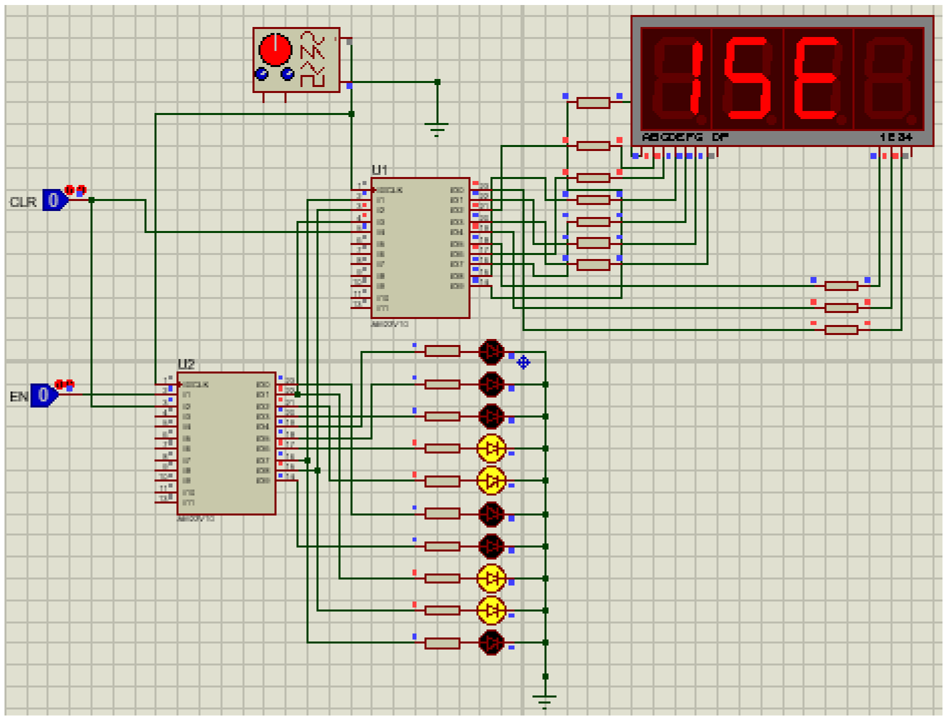
CLR
EN
U1
U2
ABCDEFG DP
1234



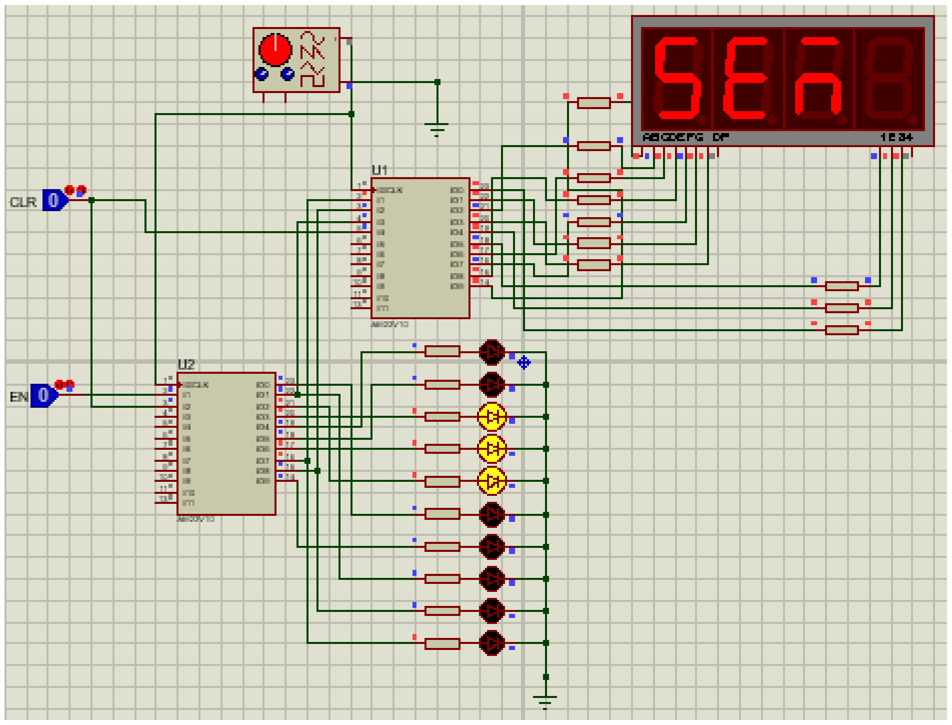
CLR
EN
U1
U2
ABCDEFG DP
1234



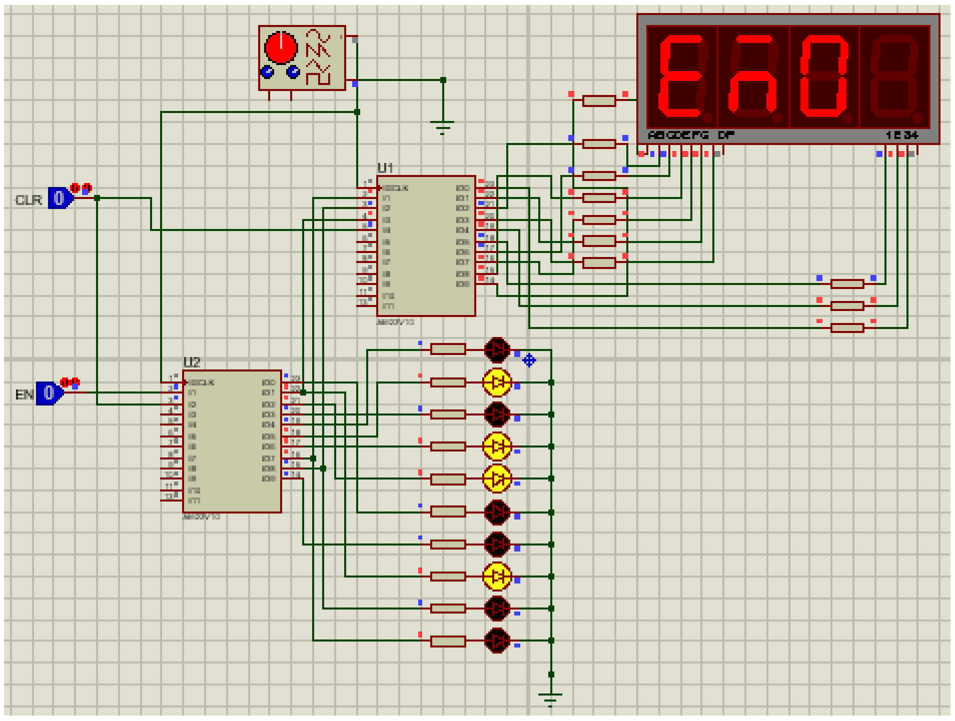
U1
U2
CLR
EN
0
0
ABCDEFG DP
1 2 3 4



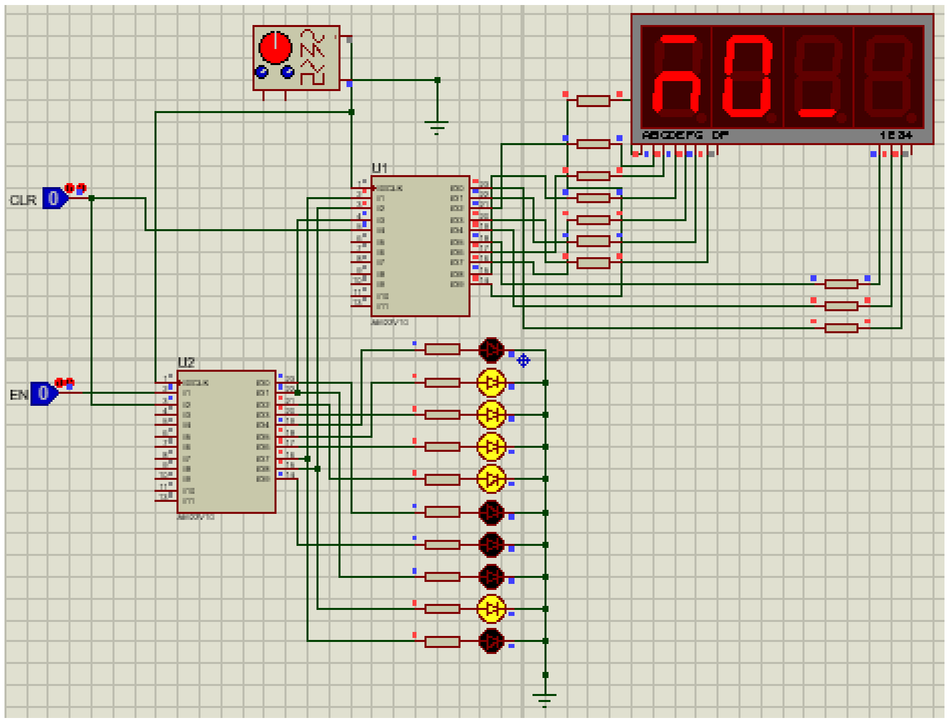
U1
U2
CLR
EN
0
0
ABCDEFG DP
1 2 3 4



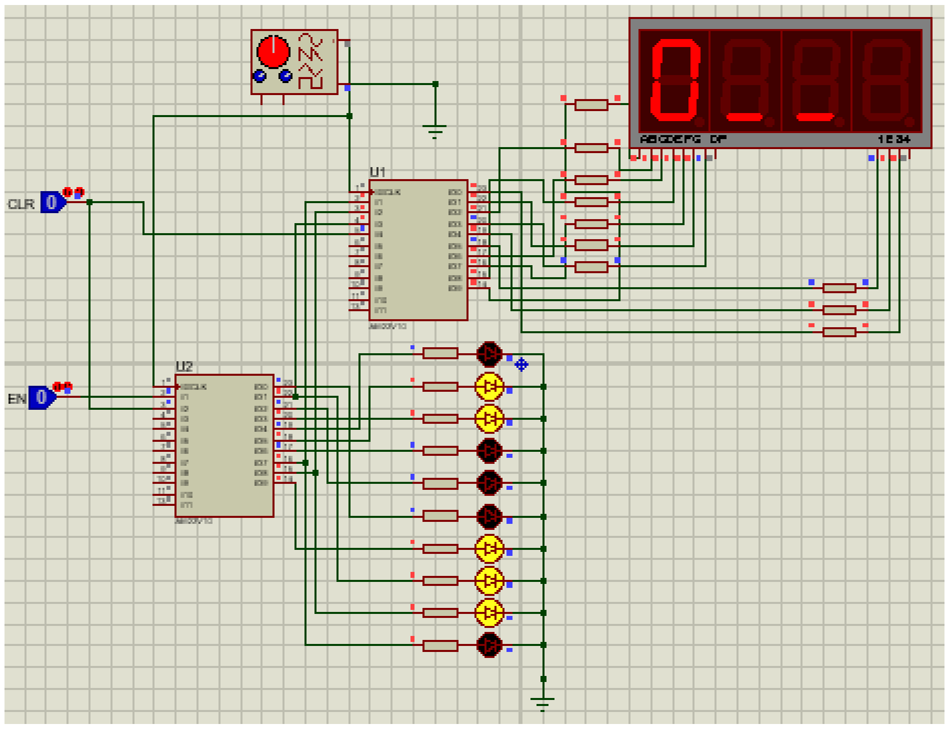
CLR
EN
U1
U2
ABCDEFG DP
1234



CLR
EN
U1
U2
ABCDEFG DP
1234



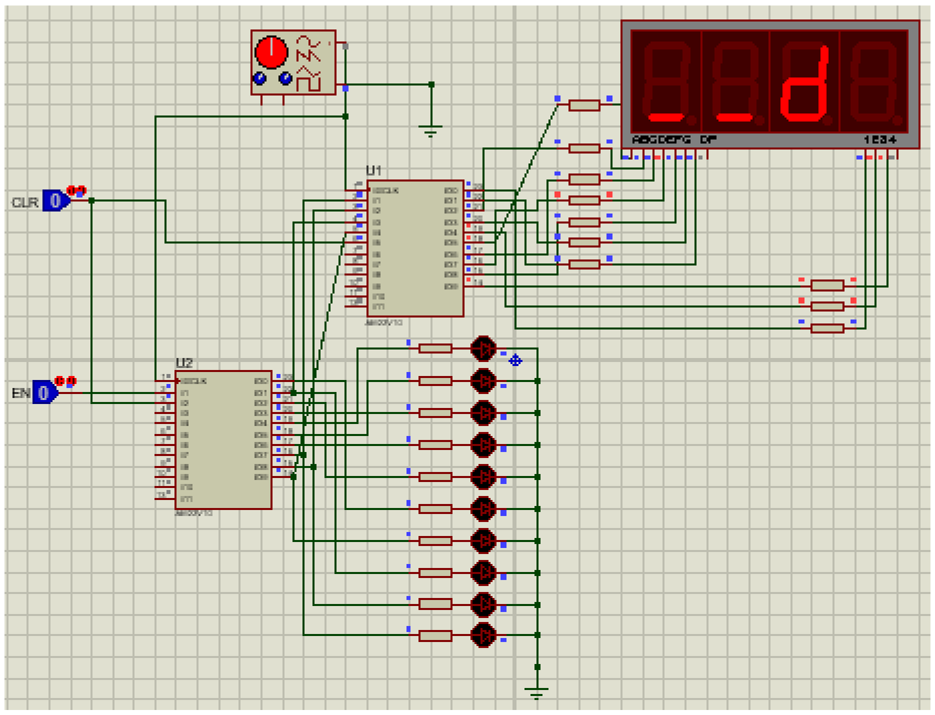
U1
U2
CLR
EN
ABCDEFG DP
1 2 3 4

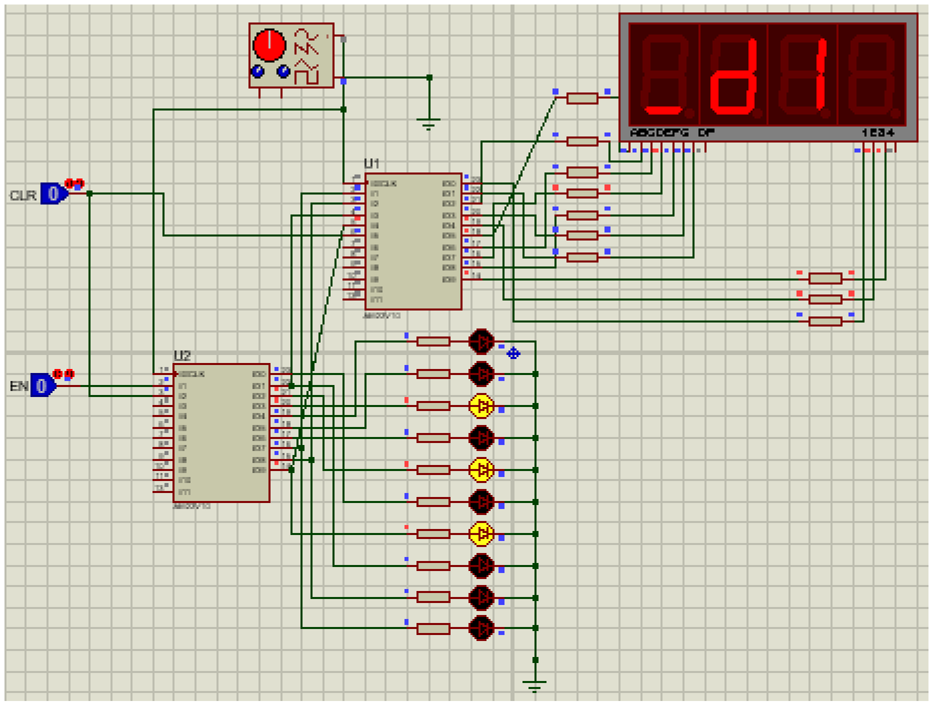
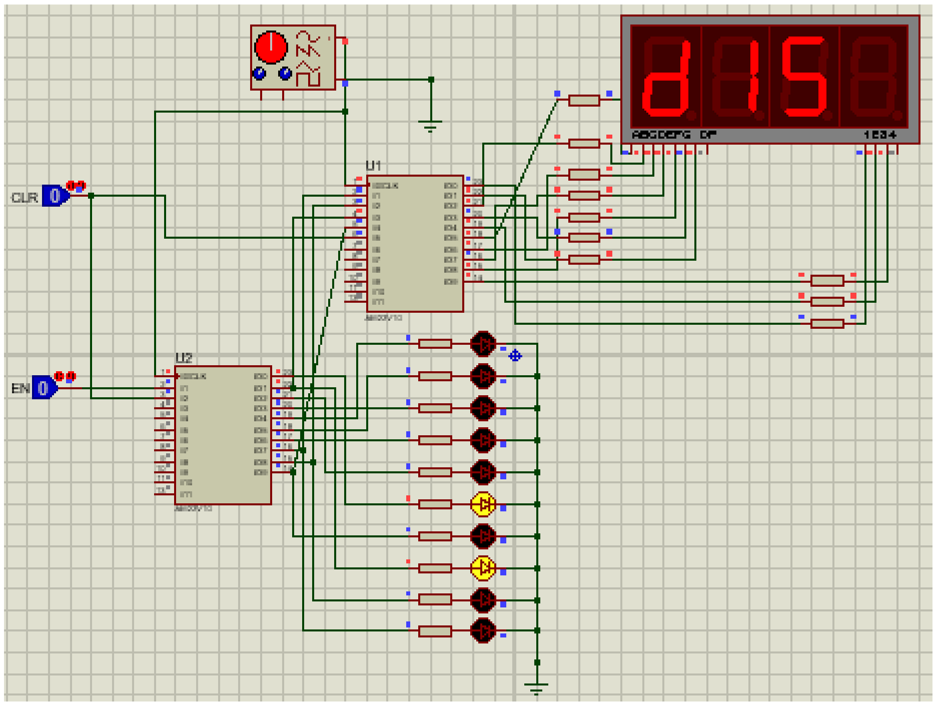


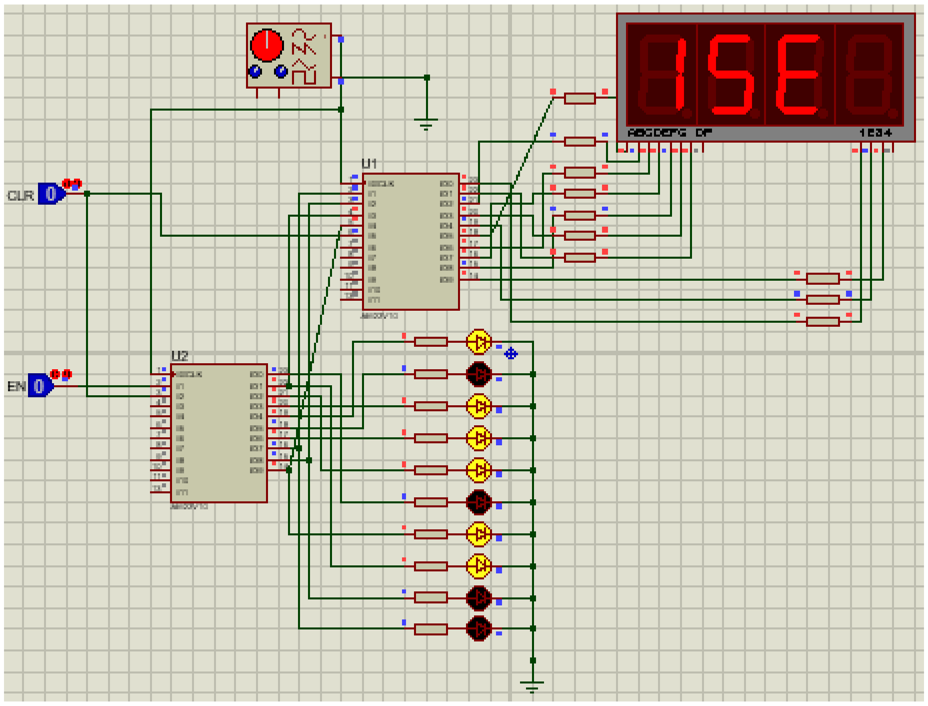
U1
U2
CLR
EN
ABCDEFG DP
1 2 3 4

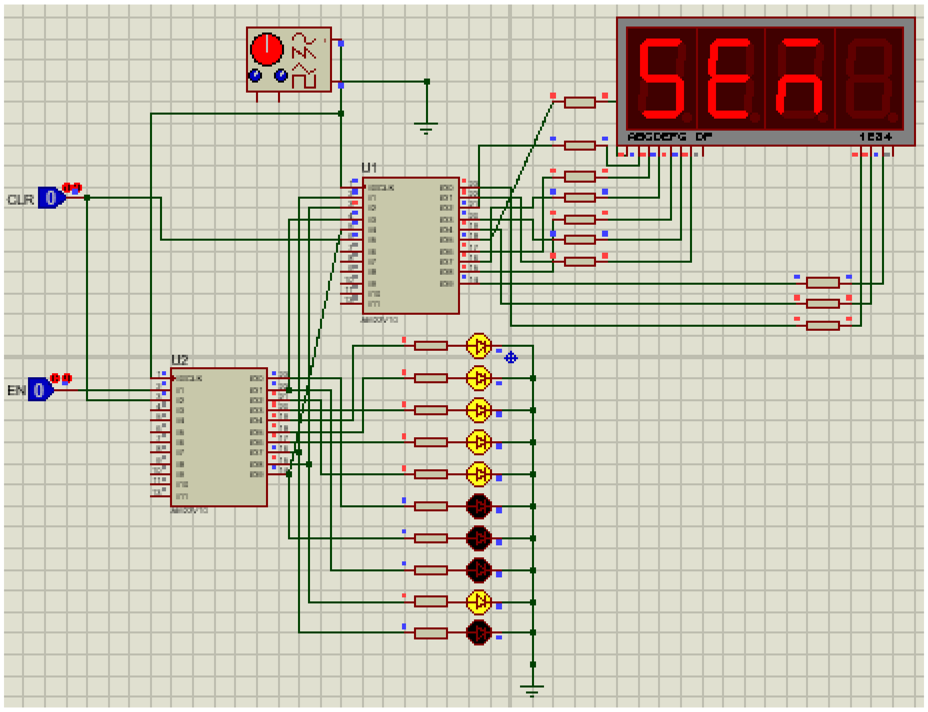
## SEGUNDA MEMORIA

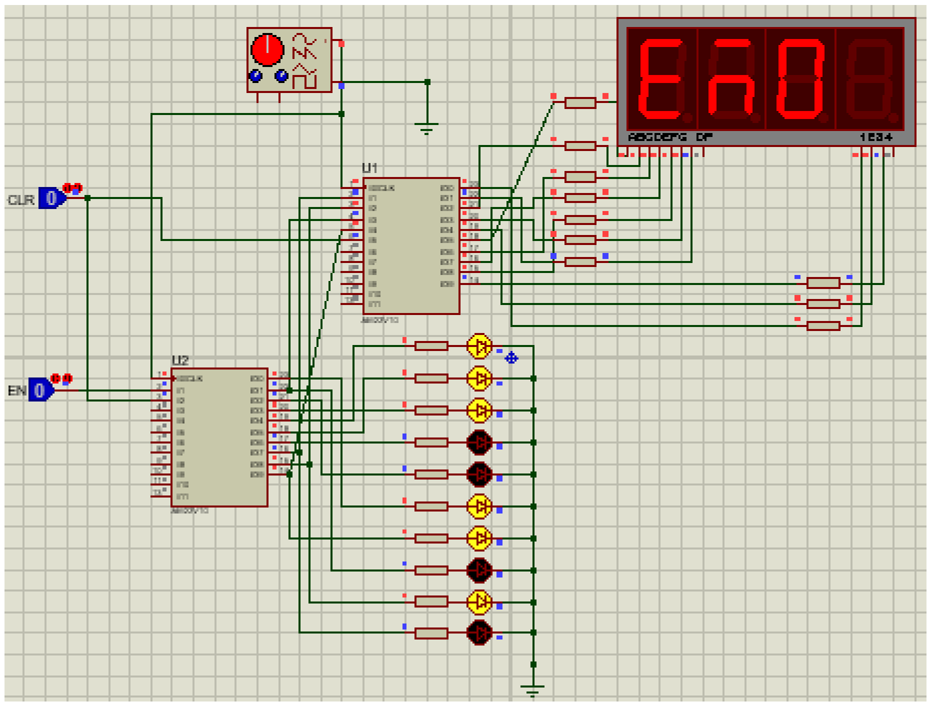
```
                              C22V10

                 __________________________________________
       clk =|  1|                                          |24|* not used
      i(3) =|  2|                                          |23|= anillo(2)
      i(2) =|  3|                                          |22|= s(0)
      i(1) =|  4|                                          |21|= s(5)
      i(0) =|  5|                                          |20|= s(1)
       clr =|  6|                                          |19|= anillo(1)
  not used *|  7|                                          |18|= s(3)
  not used *|  8|                                          |17|= s(4)
  not used *|  9|                                          |16|= s(6)
  not used *| 10|                                          |15|= s(2)
  not used *| 11|                                          |14|= anillo(0)
  not used *| 12|                                          |13|* not used
                 __________________________________________
```

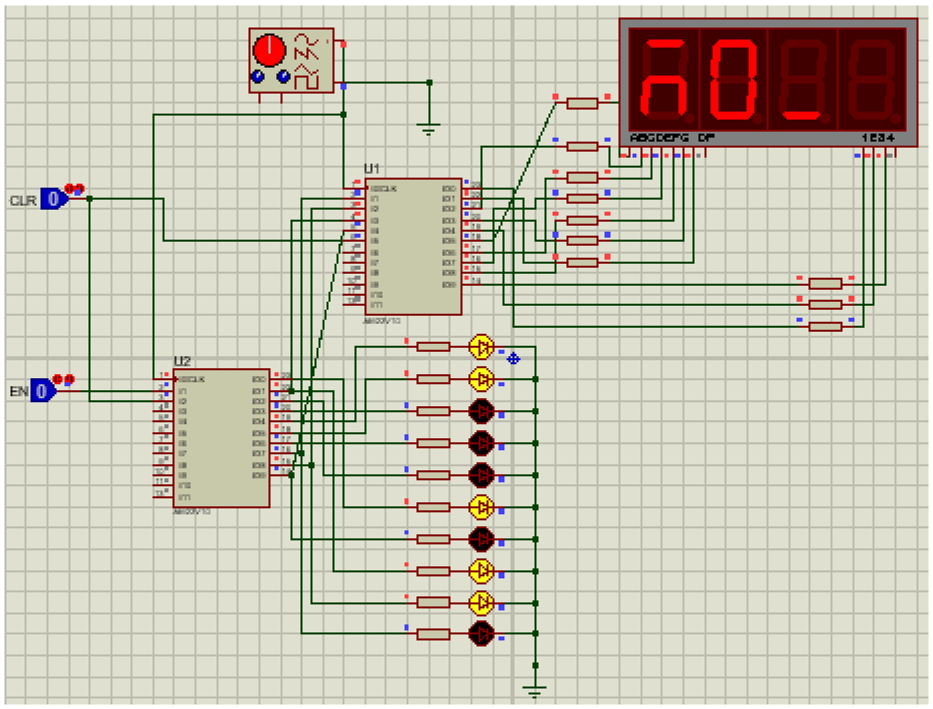


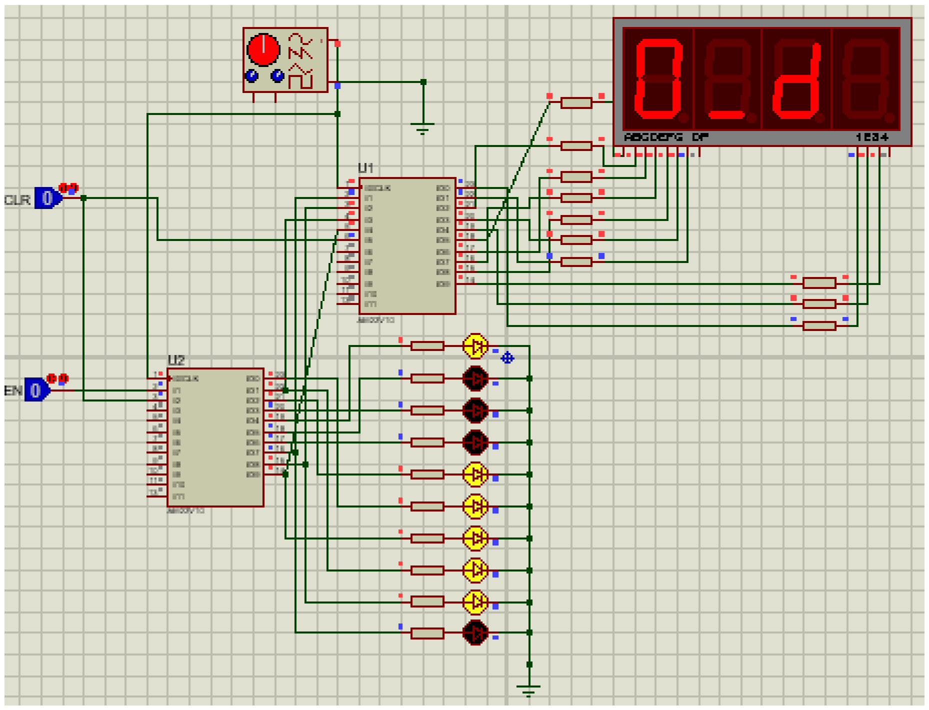
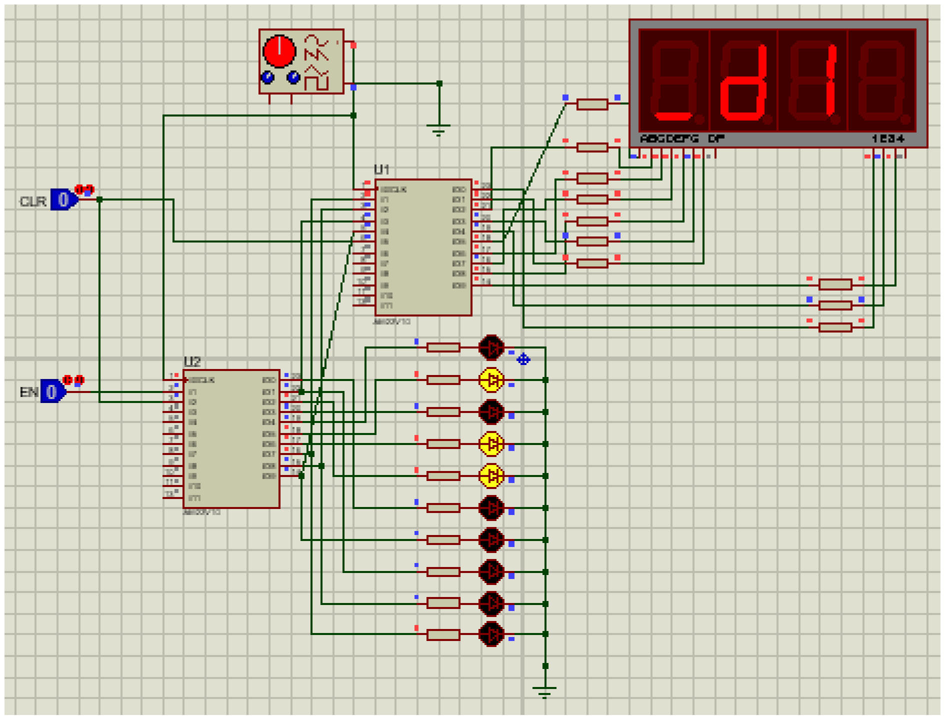

CLR
0
EN
0
U1
U2
ABCDEFG DP
1234

CLR
0
EN
0
U1
U2
ABCDEFG DP
1234

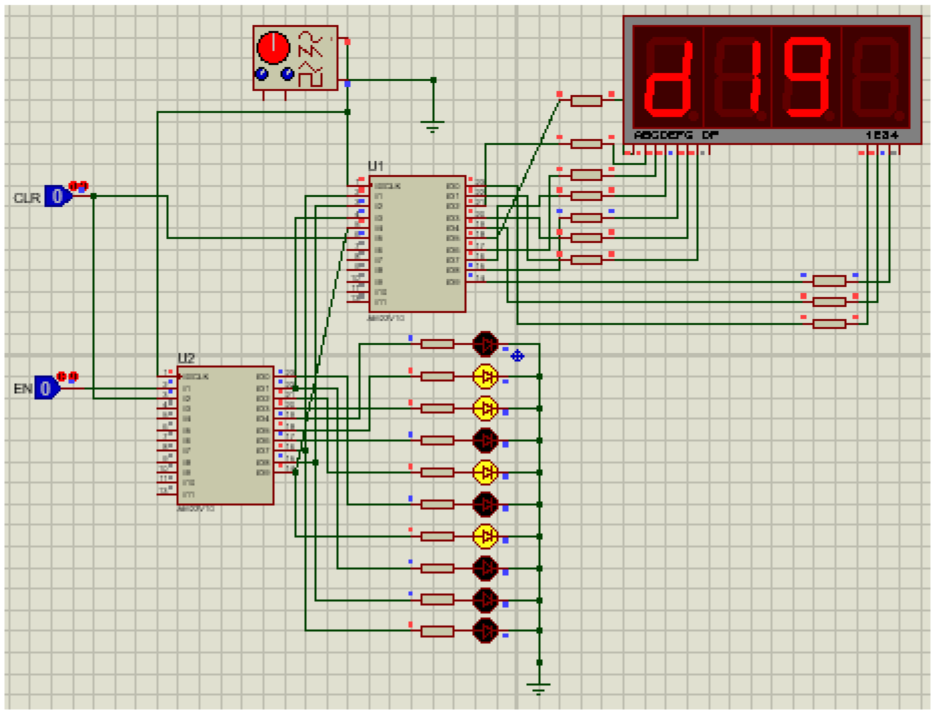

CLR
0
EN
0
U1
U2
ABCDEFG DP
1234


CLR
0
EN
0
U1
U2
ABCDEFG DP
1234

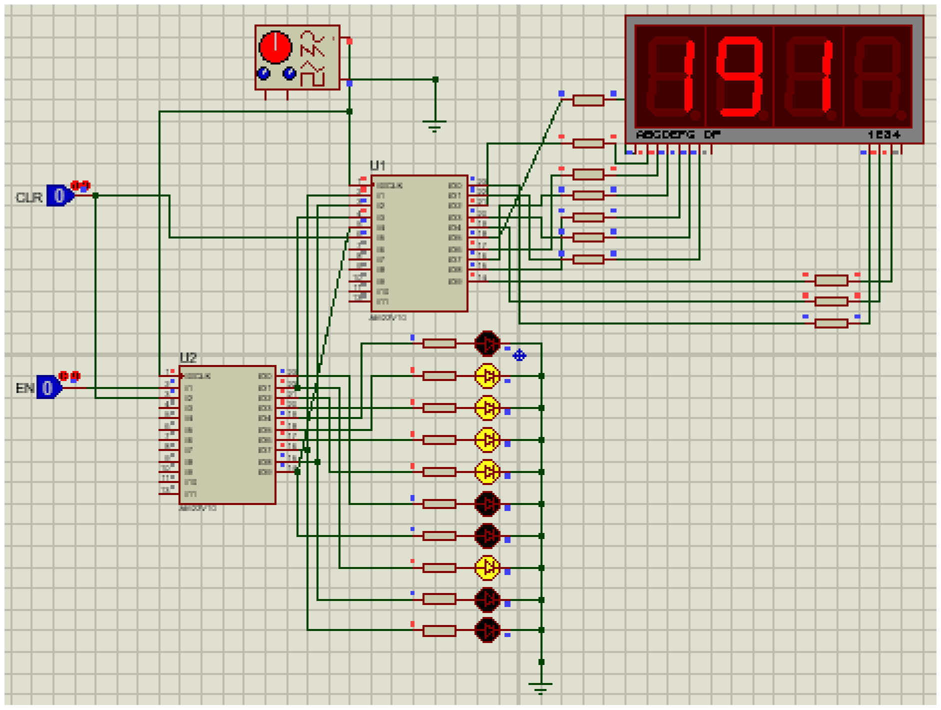

U1
U2
CLR
0
EN
0
ABCDEFG DP
1234


U1
U2
CLR
0
EN
0
ABCDEFG DP
1234

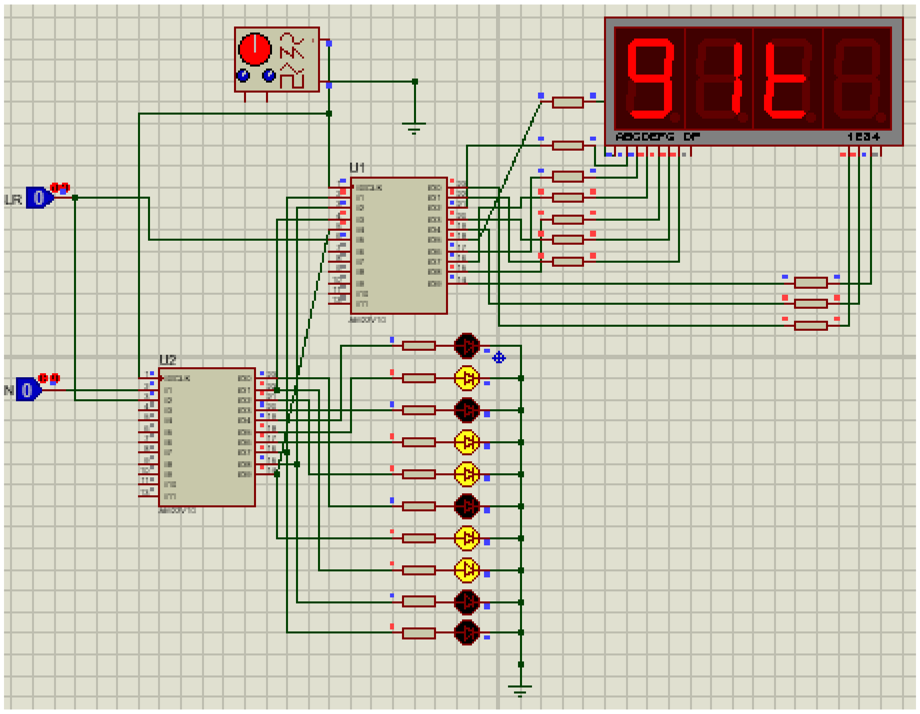

U1
U2
CLR
EN
ABCDEFG DP
1234

U1
U2
CLR
EN
ABCDEFG DP
1234

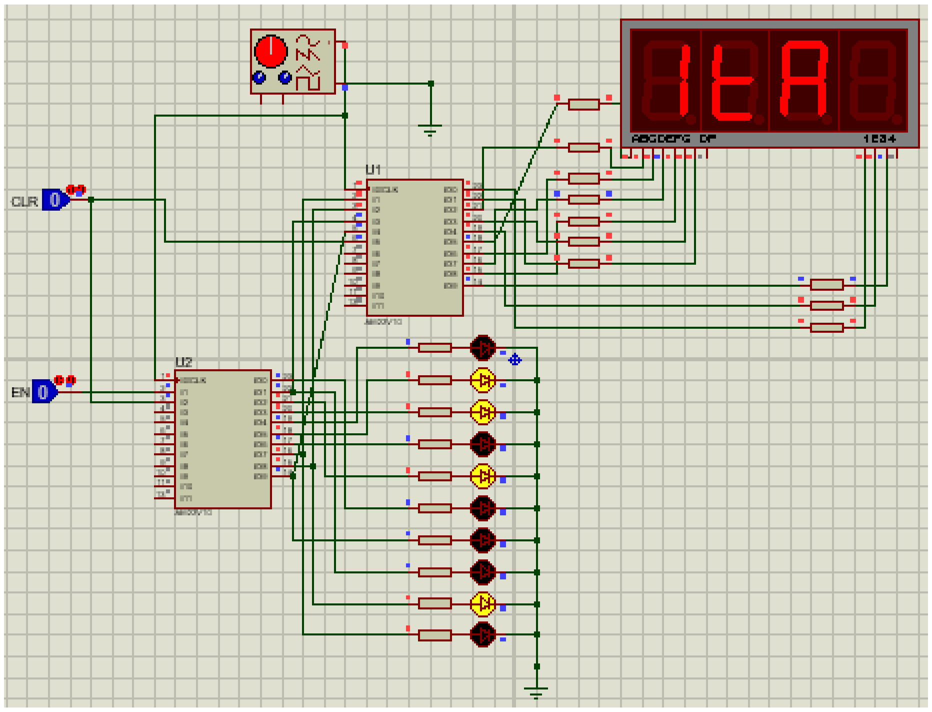


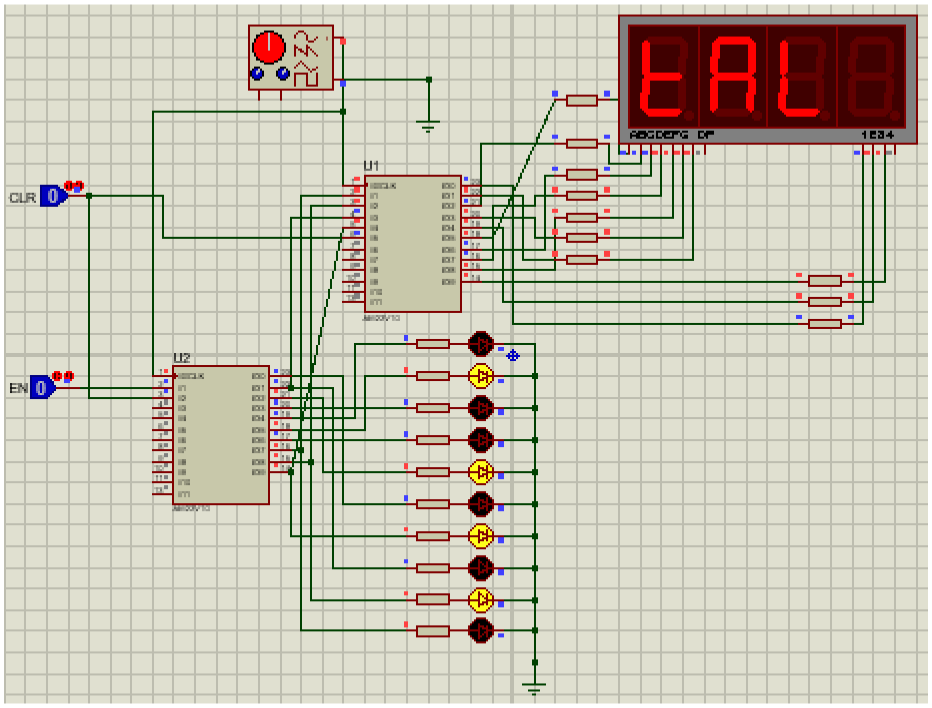
CLR
EN
U1
U2
ABCDEFG DP
1234

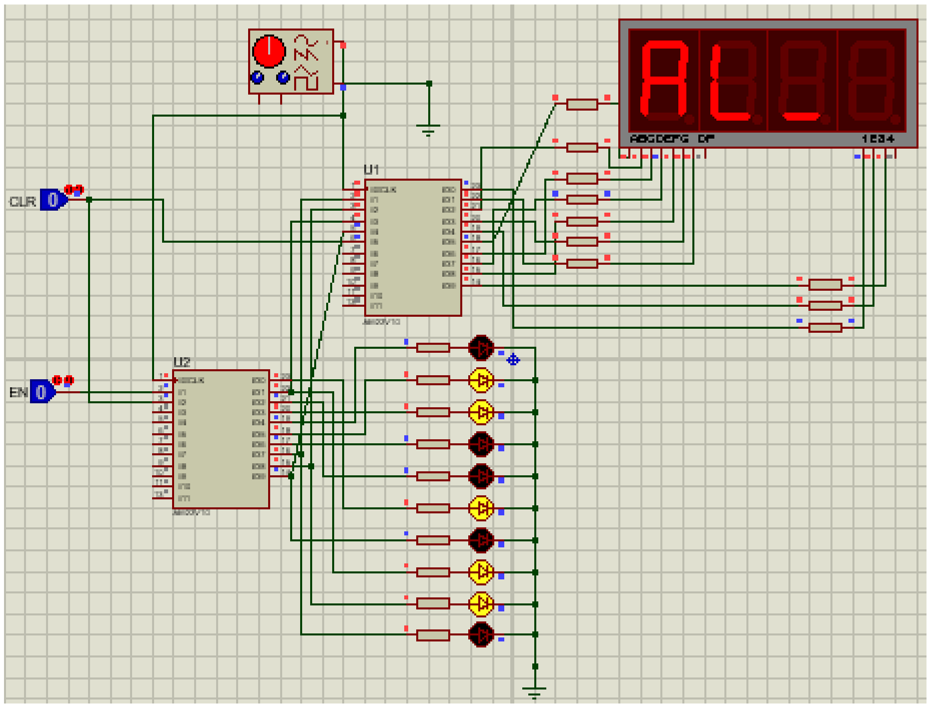


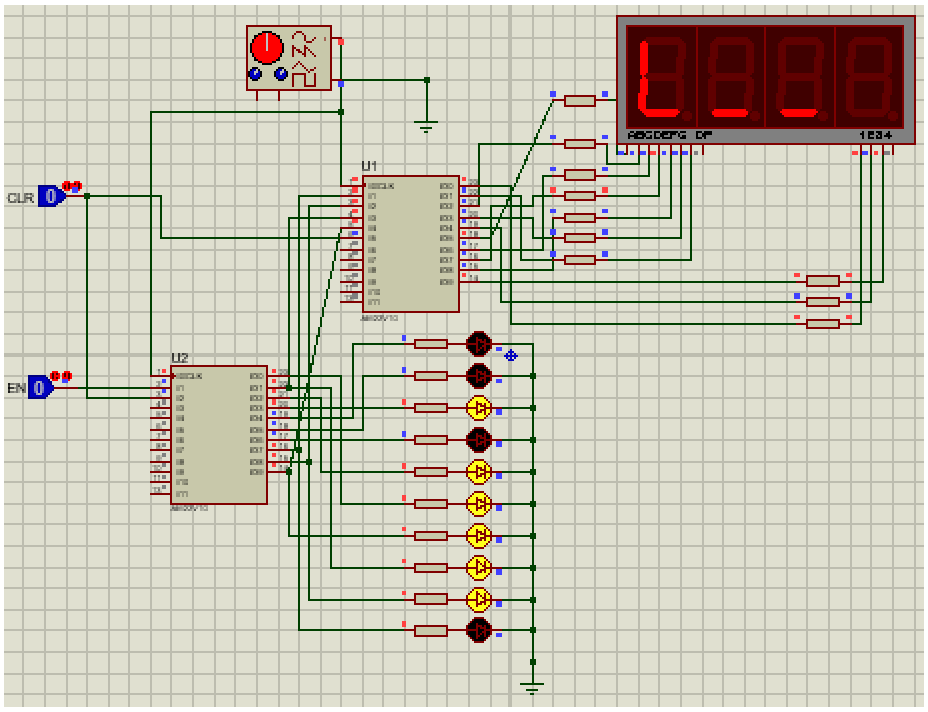
CLR
EN
U1
U2
ABCDEFG DP
1234


LR
N
U1
U2
ABCDEFG DP
1234


CLR
EN
U1
U2
ABCDEFG DP
1234


CLR
EN
U1
U2
ABCDEFG DP
1234


CLR
EN
U1
U2
ABCDEFG DP
1234



## CUESTIONARIO

1. ¿Cuántos dispositivos PLD 22V10 son necesarios para el desarrollo de esta práctica?
2

2. ¿Cuántos dispositivos de la serie 74xx (TTL) ó 40xx (CMOS) hubieras necesitado para el desarrollo de esta práctica?
Aproximadamente 30

3. ¿Cuántos pines de entrada/salida del PLD 22V10 se usan en el diseño?
Para el primero 15, y para el segundo 13

4. ¿Cuántos términos producto ocupan las ecuaciones para cada señal de salida y que porcentaje se usa en total del PLD 22V10?
Para el primero 70, y para el segundo 65

5. ¿Qué puedes concluir de esta práctica?

Las marquesinas pueden llegar a ser mucho más grandes de lo que imaginaba, con un solo PLD.