Martínez
Coronel
Drayan
Yosafat

1. (a, c)
2. (c)
3. (a)
4. (b)
5. (b, d)
6. (d)
7. (a, b)
8. (b)
9. (c)
10. (b)

S	R	Q
0	0	Q
0	1	0
1	0	1
1	1	X

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

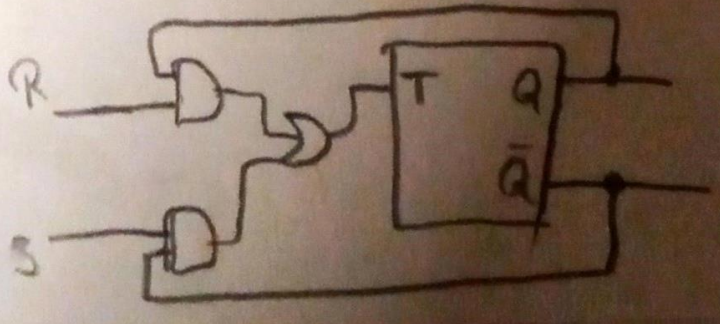
T	Q
0	Q
1	$\bar{Q}$

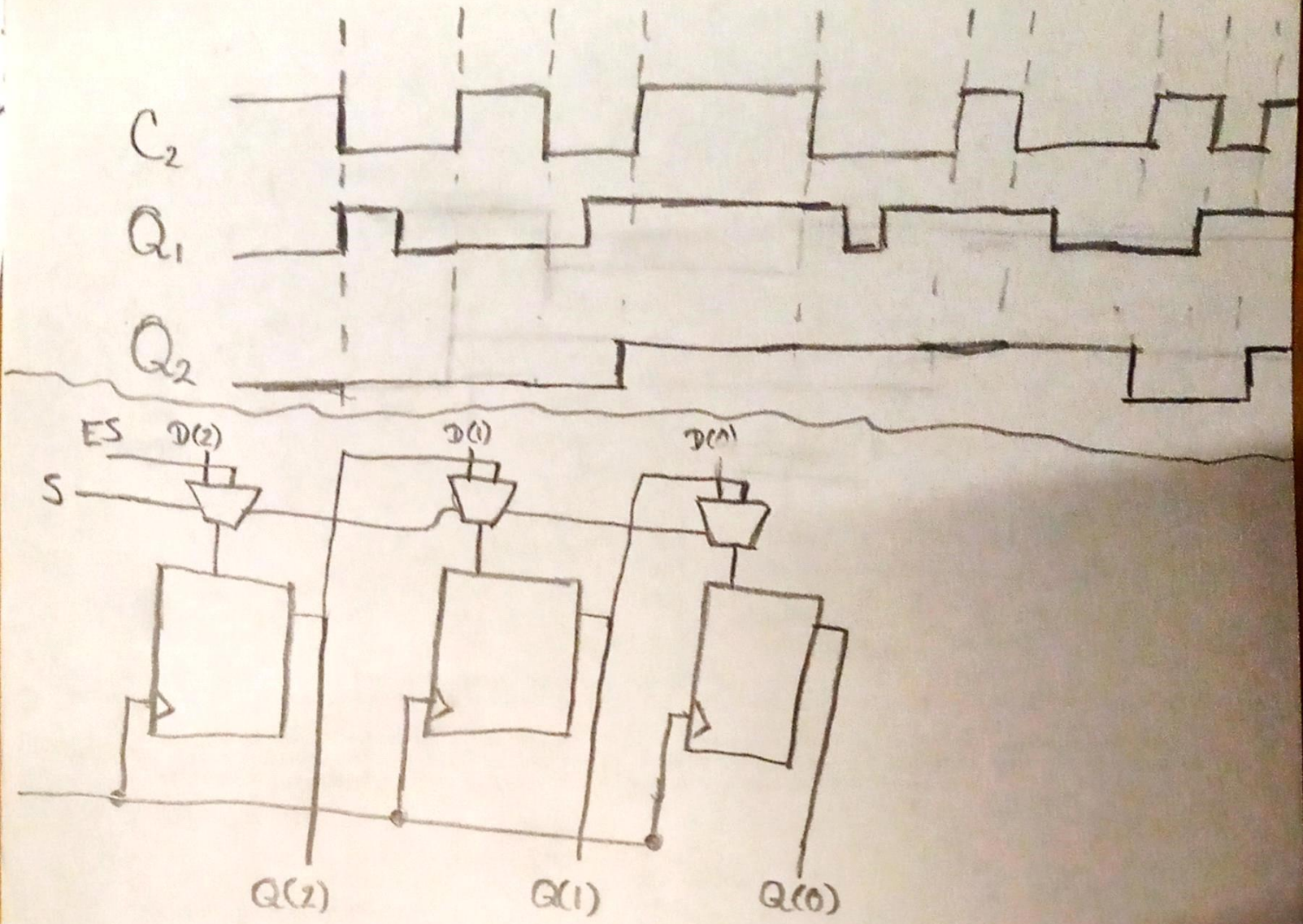
T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

S \ RQ	00	01	11	10
0			1	
1	D		X	X

$T = RQ + S\bar{Q}$






```
architecture Conv of C is
begin
  with code select
  display <= "1111110" when "000",
             "0110000" when "001",
             "1101101" when "010",
             "1111001" when "011",
             "0110011" when "100",
             "1011011" when "101",
             "1011111" when "110",
             "1110000" when others;
end Conv;
```

```
architecture Reg of registro is
signal Q : std_logic_vector (2 downto 0);
begin
  process (CLK, CLR)
  begin
    if (CLR = '1') then
       Q <= "000";
    elseif (rising_edge(CLK)) then
       case OPER is
          when '0' => Q<=D;
          when others =>
                for i in 0 to 1 loop
                   Q(i) <= D(i+1);
                end loop;
                Q(2) <= ES;
       end case;
  end process;

  with Q select
    display <= "1111110" when "000",
               "0110000" when "001",
               "1101101" when "010",
               "1111001" when "011",
               "0110011" when "100",
               "1011011" when "101",
               "1011111" when "110",
               "1110000" when others
end Reg;
```