INSTITUTO POLITÉCNICO NACIONAL

ESCUELA SUPERIOR DE CÓMPUTO

MATERIA

Arquitectura de Computadoras

PROFESOR

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GRUPO

3CV11

Practica 3

ALUMNOS

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FECHA DE ENTREGA

27/03/2021

Codigo VHDL

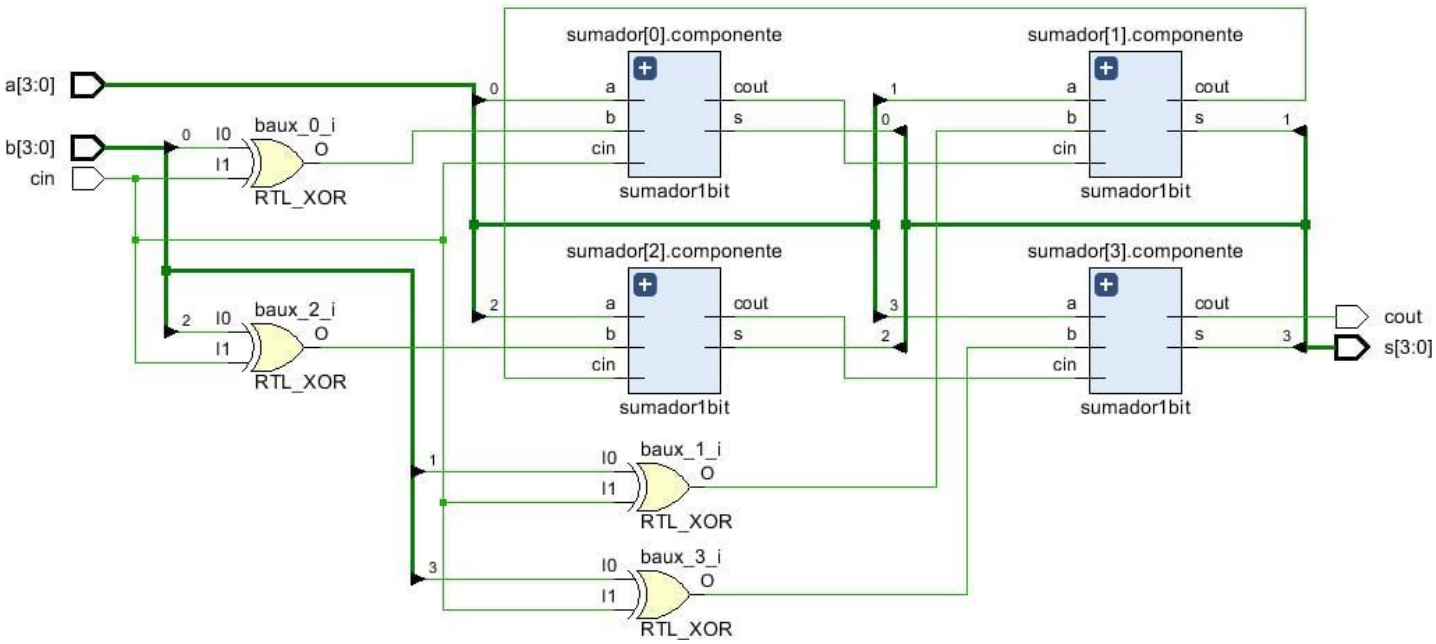
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity sumador4bits is
    Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
           b : in STD_LOGIC_VECTOR (3 downto 0);
           s : out STD_LOGIC_VECTOR (3 downto 0);
           cin : in STD_LOGIC;
           cout : out STD_LOGIC);
end sumador4bits;

architecture Behavioral of sumador4bits is
component sumador1bit is
    Port ( a,b,cin : in STD_LOGIC;
           s,cout : out STD_LOGIC);
end component;

signal acarreos: std_logic_vector (4 downto 0);
signal baux:std_logic_vector (3 downto 0);
begin
acarreos(0)<=cin;

sumador: for i in 0 to 3 generate
    baux(i)<=(b(i) xor cin);
    componente: sumador1bit port map(
    a=>a(i),
    b=>baux(i),
    cin=>acarreos(i),
    s=>s(i),
    cout=>acarreos(i+1)
    );
 end generate;
 cout<=acarreos(4);
```

TEST BENCH

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity tbsumador is
end tbsumador;

architecture Behavioral of tbsumador is
component sumador4bits is
    Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
           b : in STD_LOGIC_VECTOR (3 downto 0);
           s : out STD_LOGIC_VECTOR (3 downto 0);
           cin : in STD_LOGIC;
           cout : out STD_LOGIC);
end component;
signal a,b,s: std_logic_vector(3 downto 0);
signal cin: std_logic;
signal cout: std_logic;
begin

sum4: sumador4bits port map(
    a=>a,
    b=>b,
    s=>s,
    cin=>cin,
    cout=>cout
);

process
begin
    cin<='0';
    a<="0110";
    b<="0111";
    wait for 20ns;
    cin<='0';
    a<="0110";
    b<="1001";
    wait for 20ns;
    cin<='0';
    a<="0100";
    b<="1001";
    wait for 20ns;
    cin<='1';
    a<="1111";
    b<="0001";
    wait for 20ns;
    cin<='0';
```

```
    a<="0011";
    b<="1010";
    wait for 20ns;
    cin<='1';
    a<="1100";
    b<="0101";
    wait for 20ns;
    cin<='1';
    a<="1110";
    b<="1000";
    wait for 20ns;
    cin<='1';
    a<="1010";
    b<="0110";
    wait for 20ns;
    cin<='1';
    a<="1001";
    b<="0100";
    wait;
end process;
end Behavioral;
```

Diagrama RTL



Operación	A	B	S	Cout
Suma	6	7	13	0
Suma	6	9	15	0
Suma	4	9	13	0
Resta	15	1	14	1
Suma	3	10	13	0
Resta	12	5	7	1
Resta	14	8	6	1
Resta	10	6	4	1
Resta	9	4	5	1